The semiconductor roadmap…

- Steps (nb.: each step is ~0.7x, i.e. 2x in density)

*Lithography**	90 nm	65 nm	45 nm	32 nm
Start prod.	2003	2005	2007	2009
λ	193 nm?	193 nm	-	-
*gate length***	50 nm	35 nm	25 ~ 30 nm	-
SRAM:				
cell size	1.0 μm^2	0.57μm^2	0.35 μm^2	-
density	50 Mb	70 Mb	153 Mb	-
tr. #	-	> 0.5 G	> 1G	-
speed	-	3.4 GHz	-	-

* Nominal feature size = DRAM (or minimum metal interconnect) half pitch

** Physical gate (not channel!) length

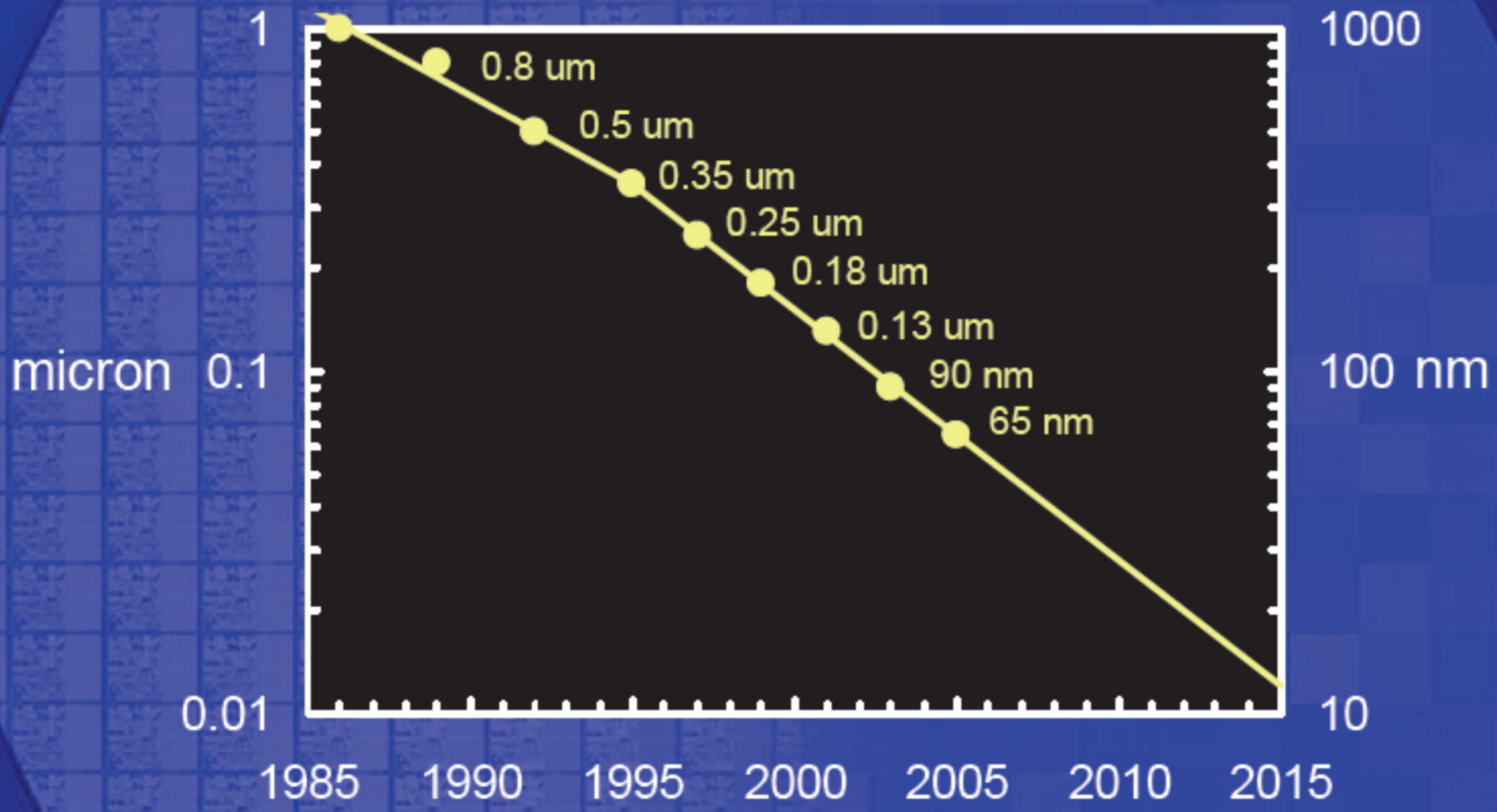
Intel's Logic Technology Evolution

Process Name	P1262	P1264	P1266	P1268
Lithography	90nm	65nm	45nm	32nm
1st Production	2003	2005	2007	2009

Moore's Law continues!

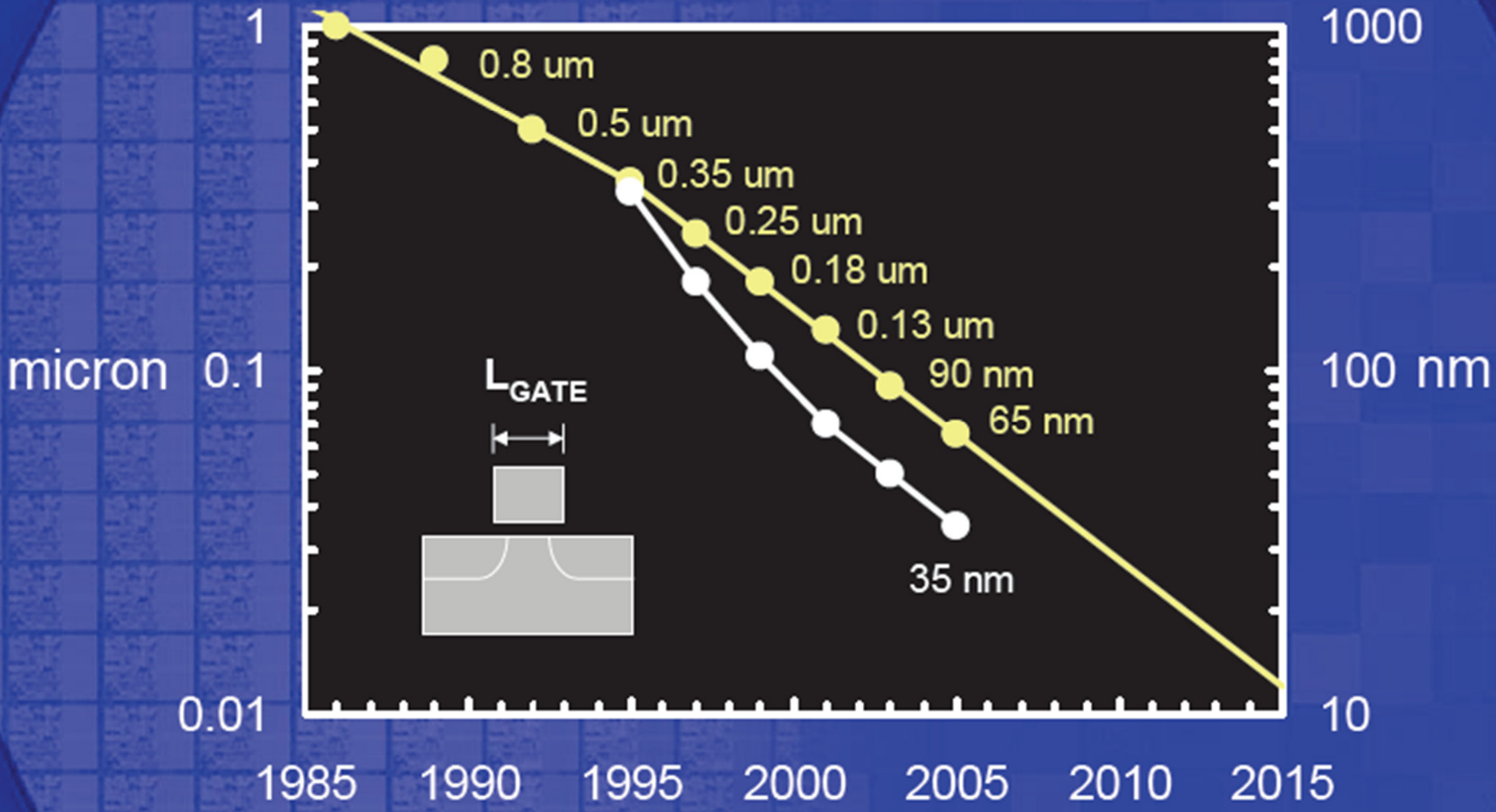
Intel continues to introduce a new technology generation every 2 years

Feature Size Scaling



New technology generations come out every 2 years and provide ~0.7x feature size reduction

Feature Size Scaling

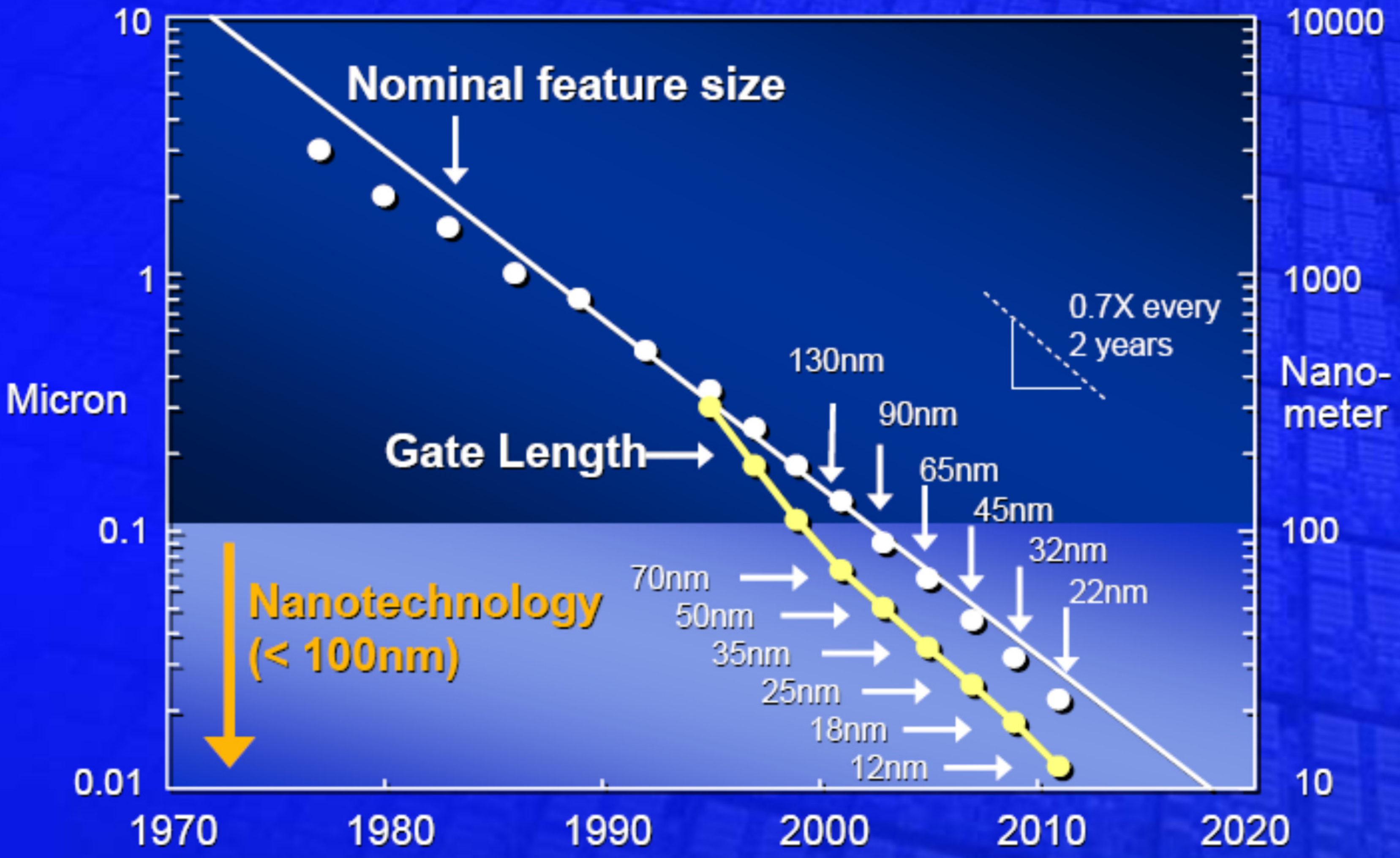


Transistor gate length is smaller than other features for improved performance and reduced power

intel

Intel Developer FORUM

Silicon Technology Reaches Nanoscale



Source: Intel

Continuation of Moore's Law

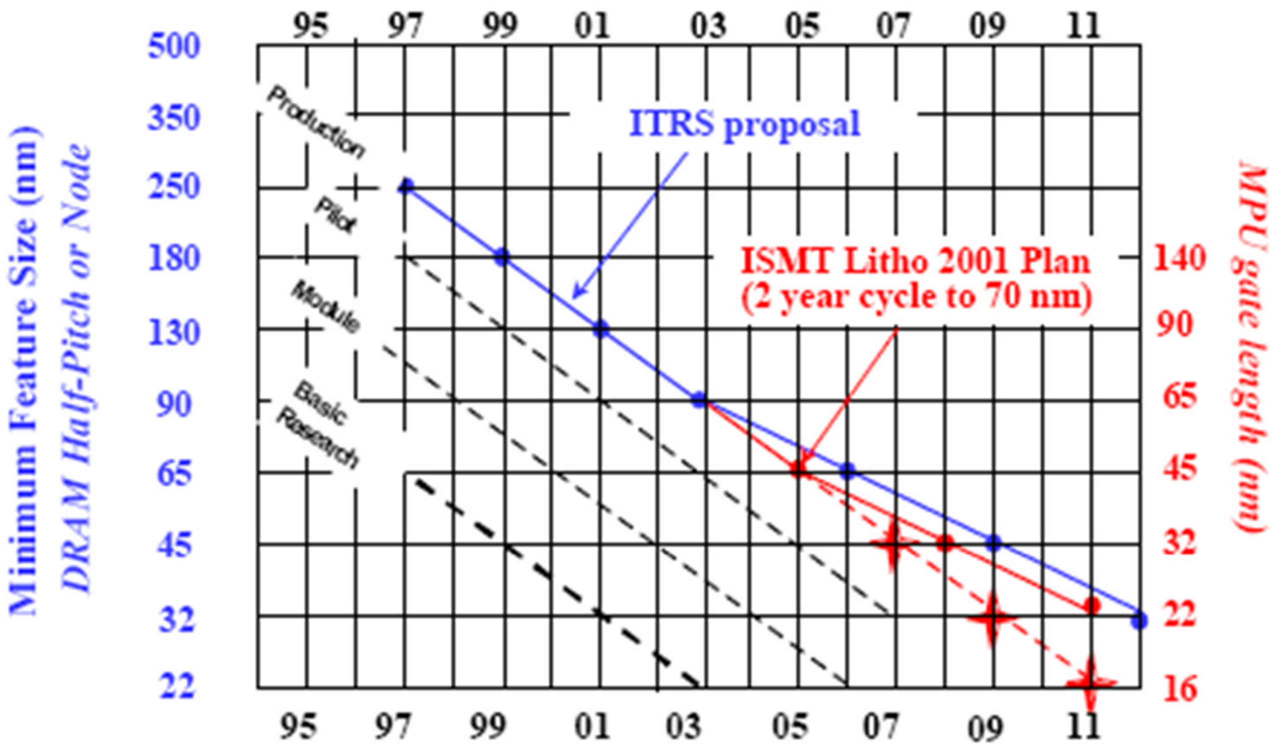
Process Name	P856	P858	Px60	P1262	P1264	P1266	P1268	P1270
1st Production	1997	1999	2001	2003	2005	2007	2009	2011
Process Generation	0.25µm	0.18µm	0.13µm	90 nm	65 nm	45 nm	32 nm	22 nm
Wafer Size (mm)	200	200	200/300	300	300	300	300	300
Inter-connect	Al	Al	Cu	Cu	Cu	Cu	Cu	?
Channel	Si	Si	Si	Strained Si	Strained Si	Strained Si	Strained Si	Strained Si
Gate dielectric	SiO_2	SiO_2	SiO_2	SiO_2	SiO_2	High-k	High-k	High-k
Gate electrode	Poly-silicon	Poly-silicon	Poly-silicon	Poly-silicon	Poly-silicon	Metal	Metal	Metal

Introduction targeted at this time

Subject to change

Intel found a solution for High-k and metal gate

ITRS Roadmap (Moore's law)



Lithography Requirements

Year of Production Technology Node	2001 130nm	2003 90nm	2005 65nm	2007 45nm	2010 32nm	2013 22nm
Half-pitch (nm)	130	90	65	45	32	22
Contacts (nm)	150	100	70	50	35	25
Overlay (nm, mean + 3 sigma)	45	31	23	18	13	9
Gate length (nm, in resist)	90	53	35	25	18	13
Gate length (nm, post-etch)	65	37	25	18	13	9
Gate CD control (nm, 3 sigma, post-etch)	5.3	3.0	2.0	1.5	1.1	0.7

Source : ITRS

[NEOC, summer08]

- TSMC (Taiwan Semiconductor Manufacturing Co. Ltd.):
  - 65 and 90 nm now in full production
  - 45 nm realesed to production (full production in Q2)
  - work in progress on 32 nm process

TMSC steps

- *0.13 μm process*

  - 12” wafer

  - copper metallisation

- *90 nm process*

  - fluoridised silicate glass

  - low K materials

- *65 nm process*

  - gate material: from cobalt silicide to nickel silicide

- *45 nm process*

  - 193 nm immersion (*wet*) photolithography for critical layers

  - extreme low K material (to reduce capacitance between metal layers)

- *32 nm process*

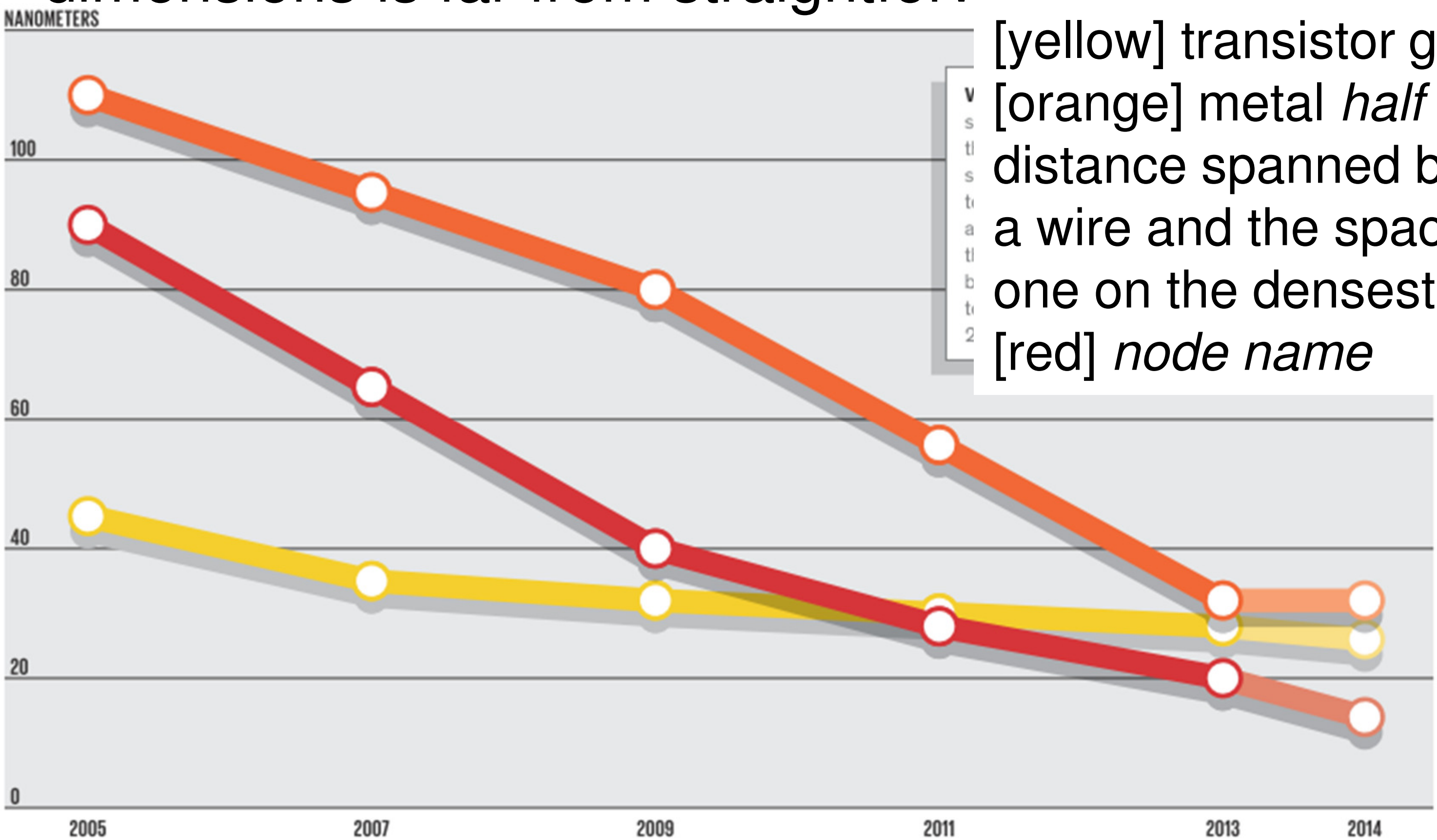
- *22 nm process*
  - expected to enter production in 2012
- *16 nm process*
  - expected to enter production in 2018
  - no way to scale CMOS to 16 nm
- *UE FP7 project DUALLOGIC*:
  Ge PMOS + III-V NMOS on silicon substrate
  - Ge: high mobility (but difficult to make n-channel)
  - III-V: high mobility (but difficult to make p-channel)
  - III-V: e.g., InGaAs
  - susbstrate: 300 mm silicon wafers

part name	year	litho-graph. size [nm]	tran-sistor count [M]	die size [mm^2]	power dissi-pation [W]	at clock freq. [MHz]	core voltage [V]	supply current [A]	power density [W/cm^2]
Intel IA-32 (general purpose CISC; top performance, superscalar, superpipelined, 32/64 bit)									
Pentium	1993	800	3.1	296	15	60	5.0	3	5
PentiumPro	1995	350	5.5	197	28	200	3.3	11	14
Pentium 4	2002	130	42	146	54	2000	1.5	36	37
Pentium 4 560	2004	90	125	112	115	3600	1.385	83	103
Core 2 Extreme	2006	65	291	143	75	2933	1.28	59	52
Sun UltraSPARC (RISC for servers; high performance, eight cores, 32 bit)									
Niagara	2005	90	279	378	63	1200	1.2	52	17
Niagara II	2007	65	503	342	84	1400	1.1	76	25
ARM (general purpose RISC processor; performance-power tradeoff, no FPU, 32 bit)									
XScale	2001	180	6.5	25	0.45	600	1.3	0.35	1.8
dspfactory (dedicated audio processor for digital hearing aids; locally optimized word widths)									
Delta-2	2000	180	0.28	10	0.24m	1.34	1.2	0.2m	2.4m

year	min. half pitch [nm]	metal level	gate oxide thick.[a] [nm]	threshold voltage [mV]	supply voltage [V]	power dissipation[b] [W]	FET curr. drive[c] [A/m]	FET leakage curr.[d] [A/m]	inverter delay[e] [ps]	lithograph. field [mm^2]	wafer diameter [cm]
	semiconductor technology in general										
2002	130	7	1.5		1.1–1.2	2.4–130	900	0.01	7.6	800	30
2004	90	10	1.2	200–500	0.9–1.2	2.2–158	1110	0.05	2.85	704	30
2007	65	11	1.1	165–524	0.8–1.2	3.0–189	1200	0.20	1.92	858	30
2010	45	12	0.7	151–502	0.7–1.1	3.0–198	2050	0.28	1.20	858	30
2013	32	13	0.6	167–483	0.6–1.0	3.0–198	2220	0.29	0.75	858	45
2016	22	13	0.5	195–487	0.5–1.0	3.0–198	2713	0.11	0.45	858	45
2019	16	14	0.5	205–488	0.5–1.0	3.0–198	2744	0.11	0.30	858	45

[Spectrum, Nov. 2013]

- Industry is now delivering integrated circuits with transistors that are made using 20- or 22-nanometer manufacturing process (with 193 nm laser light)
- But the relationship between node names and chip dimensions is far from straightforward



[yellow] transistor gate *length*
[orange] metal *half pitch* (half the distance spanned by the width of a wire and the space to the next one on the densest metal layer
[red] *node name*