Analog and Mixed-Signal Products

Analog Applications Journal

Fourth Quarter, 2003

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Introduction

Analog Applications Journal is a collection of analog application articles designed to give readers a basic understanding of TI products and to provide simple but practical examples for typical applications. Written not only for design engineers but also for engineering managers, technicians, system designers and marketing and sales personnel, the book emphasizes general application concepts over lengthy mathematical analyses.

These applications are not intended as "how-to" instructions for specific circuits but as examples of how devices could be used to solve specific design requirements. Readers will find tutorial information as well as practical engineering solutions on components from the following categories:

- Data Acquisition
- Power Management
- Amplifiers: Op Amps

Where applicable, readers will also find software routines and program structures. Finally, *Analog Applications Journal* includes helpful hints and rules of thumb to guide readers in preparing for their design.

ADS82x ADC with non-uniform sampling clock

By Hui-Qing Liu (Email: liu_hui-qing@ti.com)
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Introduction

The Texas Instruments (TI) high-speed analog-to-digital converter (ADC) ADS82x family includes ADS825/822, ADS826/823, and ADS828. These ADCs have 10-bit resolution with a maximum sampling speed of 40, 60, and 75 MHz, respectively. They are widely used in communications, video digitizing, test equipment, CCD imaging, and medical ultrasound imaging. In some applications the ADCs are driven by a continuous sampling clock with constant frequency. However, in other applications such as medical ultrasound imaging or where the ADCs are parallel with interleaved configuration, they must operate with a sampling clock that has variable frequency, phase, or duty cycle. In other words, these ADCs must operate with a non-uniform sampling clock. Can TI's ADS82x handle this? A lab bench test has shown good results, and the answer is *yes*. This article presents the measurement system and fast Fourier transform (FFT) analysis method used along with the test results for only the ADS826 EVM. However, these test results are applicable to all other ADCs in the ADS82x family, since these ADCs all have pipeline architecture and are designed with the same basic features, such as 10-bit resolution, internal or external reference, single-ended or differential analog input, input range selection, single 5-V power supply, power-down mode, low power dissipation, three-state output, and CMOS- or TTL-output compatibility.

Figure 1. ADS82x bench test system

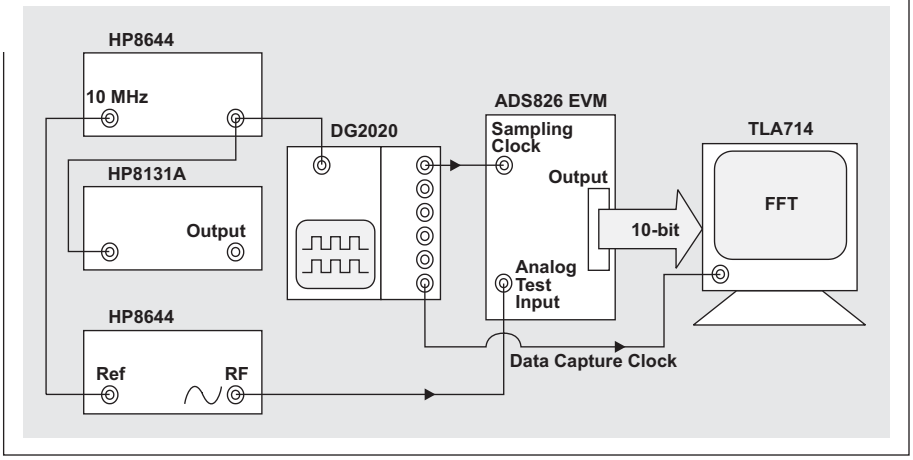
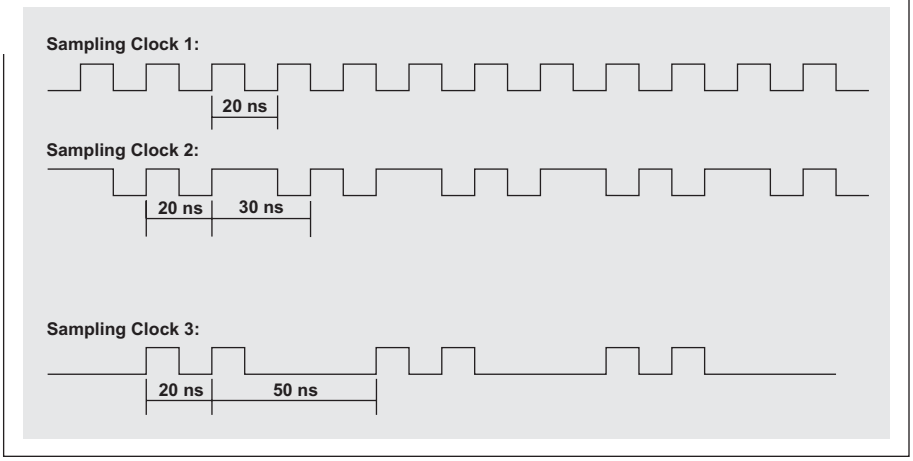


Figure 2. Pattern clocks for ADS826 test



Test system

The ADS826 bench test system includes a pulse generator (HP8131A), data generator (DG2020), waveform generator (HP8644), and Tektronix logic analyzer (TLA714) (see Figure 1). This system is used to generate an analog signal, pattern clock, and data capture clock. The analog signal, a sine wave that can be varied in frequency and amplitude, is an input test signal to the ADS826; and the pattern clock, which can be varied in frequency, phase, or duty cycle, is the sampling clock to the ADS826. The data capture clock can be flexible with a proper frequency and duty cycle for the TLA714 to capture data from the ADS826 EVM and perform FFT analysis. The clock source is phase locked with the test signal source by the 10-MHz reference output of the HP8644, so all the signals generated from the system are synchronized. The HP8131A is used to calibrate DG2020.

Pattern clocks

Three different pattern clocks, plotted in Figure 2, are generated from this system. They are used to test the non-uniform sampling performance of

the ADS826. Sampling Clock 1 (Case 1) is a uniform clock with a frequency of 50 MHz and a duty cycle of 50%. Sampling Clock 2 (Case 2) is a non-uniform clock with frequency (varied cycle by cycle) alternating from 50 MHz with a 50% duty cycle to 33.3 MHz with a 66.7% duty cycle. Sampling Clock 3 (Case 3) is a non-uniform clock with frequency varying (cycle by cycle) from 50 MHz with a 50% duty cycle to 20 MHz with a 20% duty cycle. These clocks are simulated from real applications.

ADS826 input/output configuration

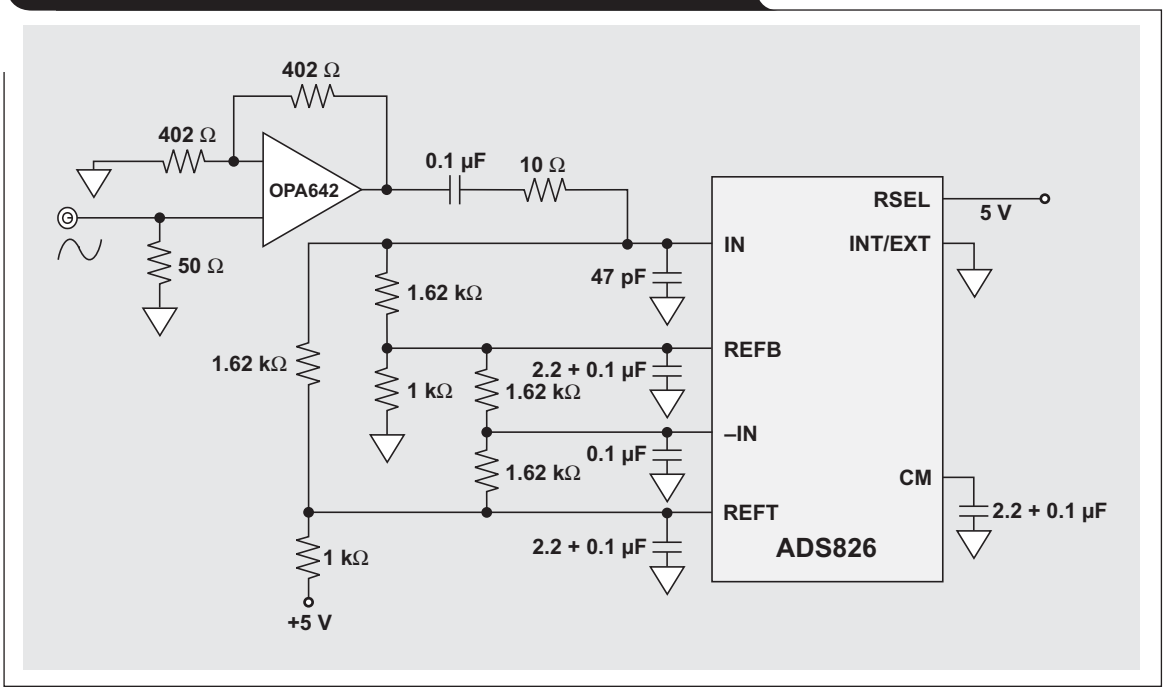
The single-ended analog input circuit used in this test is shown in Figure 3. Here an OPA642 with an inverting gain of 2 is used. This circuit mainly provides two conditions for the ADS826. One is an ac-coupled signal path with a power amplifier with proper gain and driving capability; another is the common-mode dc voltage for the ADS826 analog input bias. The ADS826 is configured with an internal reference and a full-scale input range of 2 V_{p-p}. The common-mode pin (CM) is not used here except for bypassing. Based on the configuration, a 2-V_{p-p} analog sine wave is applied to +IN, and a 2.35-V common-mode dc voltage is added to both +IN and –IN of the ADS826 analog input. This common-mode voltage is generated by REFT, REFB, and an external 5-V power supply through a balanced resistor network. The input clock of ADS826 from DG2020 is one of the three sampling clocks mentioned earlier. The digital output of the ADS826 is connected to the TLA714 through a data bus driver such as TI's SN74x family. The digital configuration of ADS826 is straightforward and is therefore not shown in Figure 3. Details about the ADS826 digital output circuit can be found in Reference 1.

Data measurement and analysis

A TLA714 is used to collect the output data from the ADS826, and the performance of the device is evaluated using FFT analysis. For this approach, the sampling clock of the ADS826 and the input clock of the TLA714 need to be synchronized with the analog input test signal. When the signal is synchronized, the data is ready to be measured. In the beginning, the analog sine wave is sampled by the ADS826 at the rising edge of the sampling clock, and the sample is converted into digital form in the pipeline stage. Five sampling clocks later, a digital number (straight offset binary code) of the sample is output to the data bus of the ADS826 with additional small-signal propagation. The digital data is sent to the data bus by the ADS826 at the rising edge of the input sampling clock. It stays on the bus for one clock period and is then updated at the next rising edge of the input sampling clock by new sample data. When the data is valid on the data bus, it is captured by the logic analyzer with a synchronized clock. The data is then processed and analyzed using FFT analysis.

The three different sampling cases mentioned earlier are evaluated here. In Case 1 the sampling clock frequency of ADS826 is constant at 50 MHz; in Case 2 the sampling clock frequency of ADS826 is not constant and is regularly varied 20 ns or 30 ns on a cycle-by-cycle basis; and in Case 3 the sampling clock period of the ADS826 is regularly varied by 20 ns or 50 ns. Sampling Clocks 2 and 3 are non-uniform sampling clocks, and their phases change with time. This is clearly demonstrated by Sampling Clock 3, where the clock phase is delayed for 30 ns after each two 50-MHz clock cycles. Such sampling phase variation is apparent

Figure 3. Single-ended input circuit for ADS826 bench test



from the output data of the ADS826. In Case 1, the ADS826 samples the analog sine wave and constantly outputs the digitized samples at 50 MSPS. In Cases 2 and 3, the analog sine wave is sampled by the ADS826 at variable speed so that the digitized samples are sent out in non-uniform time intervals. This is shown in Figures 4–6. Further analysis of the non-uniform sampling performance of the ADS826 is presented later under "Test results."

Does the ADS826 operate as well with a non-uniform sampling clock as it

Figure 4. Non-uniform sampling time intervals

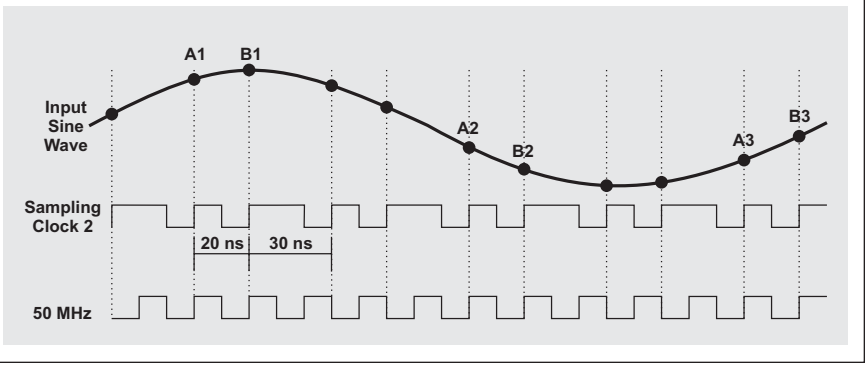


Figure 5. ADS826 non-uniform sampling performance analysis for Case 2

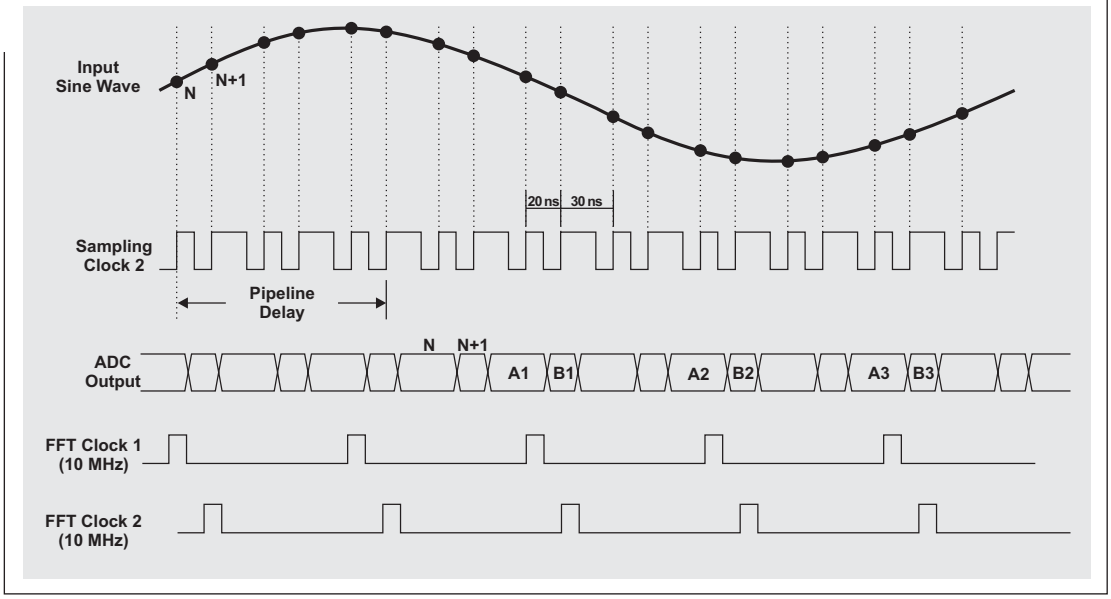
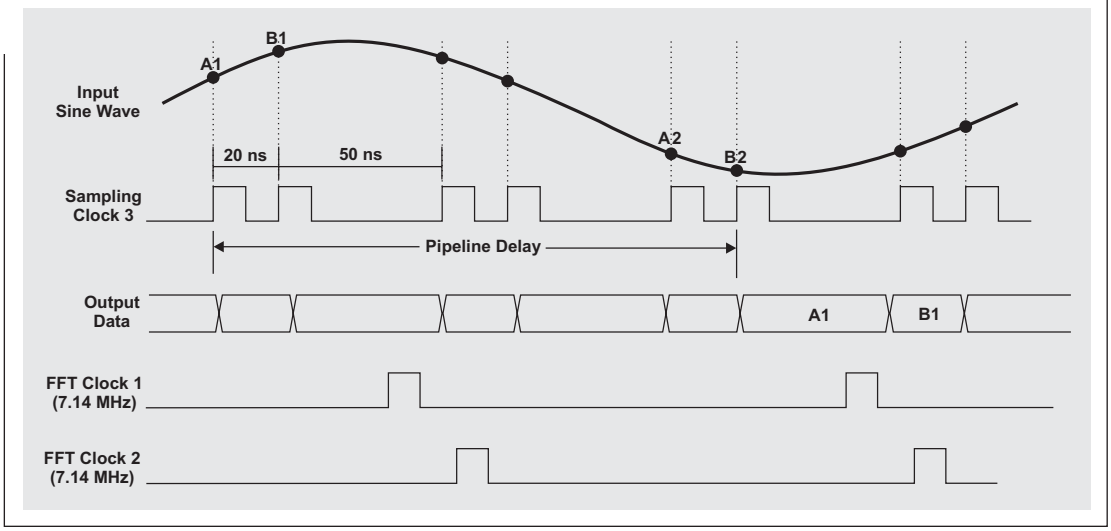


Figure 6. ADS826 non-uniform sampling performance analysis for Case 3

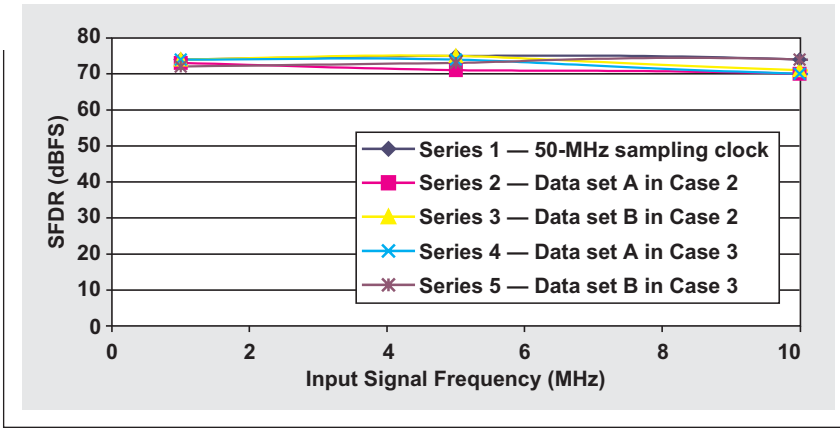


does with a uniform sampling clock? Yes, and this can be explained by the downsampling technique and the FFT analysis. In FFT analysis, the sample size is kept at 4096; and the FFT sampling frequency is kept more than five times higher than the signal frequency for all three cases. In Case 1 with Sampling Clock 1, the output data of the ADS826 can be used directly as the FFT input because of the uniform samples; and the FFT result is the specification in the data sheet. In Cases 2 and 3 with a non-uniform sampling clock, the output data of the ADS826 cannot be used directly as the FFT input due to non-uniform samples. To perform the FFT analysis for Cases 2 and 3, we need to find a set of uniform samples from non-uniform ADC sampling data. The implementation of this idea is shown in Figure 4, where the ADS826 samples an analog sine wave at the rising edge of Sampling Clock 2 and the sample locations on the sine wave have non-uniform time intervals. With FFT downsampling techniques, however, these locations can be classified into uniform time-interval sets. For example, by using a 50-MHz clock as a uniform time reference, we can find data set A (A1, A2, A3...) and data set B (B1, B2, B3...) in which the data is uniformly spaced. Furthermore, data set A results from fast-sampling Clock 2 (50 MHz), and data set B results from slow-sampling Clock 2 (33.3 MHz). The data in each set is uniformly time-spaced by the 10-MSPS FFT sampling frequency, which downsamples the original data. This frequency can be used as a clock frequency of the logic analyzer that is used to extract data set A or B from the data bus of the ADS826.

The completed data acquisition from the ADS826 with a non-uniform sampling clock is shown in Figure 5, where sample N on the sine wave is collected by the ADS826 at the rising edge of the input clock and is output after a period of five input clocks. The input clock consists of fast and slow clocks, while the ADS826 output data consists of long and short periods. Because of the five-clock delay, sample N from the fast input clock appears on the output data bus for a long period, and sample N+1 from the slow input clock appears on the output data bus for a short period. For FFT analysis, FFT Clock 1 (10 MHz) is used to capture data set A, while FFT Clock 2 (10 MHz with a 20-ns clock delay) is used to capture data set B. The output results of data sets A and B represent the dynamic performance of the ADS826 with non-uniform Sampling Clock 2, as shown later under "Test results."

The same principle is applied in Case 3, which is shown in Figure 6. In this case the frequency of FFT Clocks 1 and 2 is 7.14 MHz. With a different sampling clock pattern, the downsampling clock frequency for FFT will vary and may be difficult to determine. The test results show that the ADS826 functions well with a non-uniform sampling clock as long as the clock high and low pulse width is at least half the period of the highest sampling clock specified in the data sheet; for example, a pulse width of at least 8.3 ns for the ADS826 (maximum speed is 60 MHz). The sampling clock speed also has to meet the minimum limit in the data sheet.

Figure 7. SFDR of ADS826 with uniform and non-uniform sampling clocks



Test results

Input analog signal frequencies of up to 30 MHz for all three cases were tested, and the results are shown in Table 1 and Figure 7. Table 1 shows that there is no change in the signal-to-noise ratio (SNR) whether the ADS826 is driven by a uniform or non-uniform sampling clock. Figure 7 shows that there is also no significant difference in spurious-free dynamic range (SFDR) performance between uniform and non-uniform sampling. In addition, for

Table 1. SNR (dBFS) of ADS826

	SAMPLING CLOCK (MHz)	FFT CLOCK (MHz)	SNR (dBFS)			
			1-MHz Signal Frequency	5-MHz Signal Frequency	10-MHz Signal Frequency	30-MHz Signal Frequency
Case 1	50 (uniform)	50	60	60	60	58
Case 2	50 and 33.3 mixed (non-uniform)	10 (FFT Clock 1)	60	60	60	58
	50 and 33.3 mixed (non-uniform)	10 (FFT Clock 2)	60	60	60	58
Case 3	50 and 20 mixed (non-uniform)	7.14 (FFT Clock 1)	60	60	60	58
	50 and 20 mixed (non-uniform)	7.14 (FFT Clock 2)	60	60	60	58

non-uniform sampling, the SFDR increases when the sampling clock or input signal amplitude decreases.

The FFT test result is shown in Figures 8–10. Figure 8 shows the FFT output of Case 1 and the performance of ADS826 with a 50-MHz sampling clock and a 1-MHz input sine wave at maximum amplitude. The SNR is 60 dBFS, and the SFDR is 74 dBFS. The FFT output of Case 2 is shown in Figure 9, in which the non-uniform ADC samples are downsampled by a 10-MHz FFT clock. Figure 9a shows the FFT output of data set A, and Figure 9b shows the FFT output of data set B. The SNR is 60 dBFS for both data sets A and B; the SFDR is 73 dBFS for data set A and 74 dBFS for data set B. The FFT output of Case 3 is shown in Figure 10, in which the non-uniform ADC samples are downsampled by a 7.143-MHz FFT clock. The SNR is 60 dBFS for both data sets A and B; the SFDR is 74 dBFS for data set A and 72 dBFS for data set B.

Conclusion

The test results presented in this article strongly support non-uniform sampling applications of the ADS82x family. The test results show that the same SNR is achieved with both uniform and non-uniform sampling using the ADS826. Good SFDR is also achieved with both uniform and non-uniform sampling. The test data and analysis conclude that the ADS826 functions well with a non-uniform sampling clock as long as the clock high and low pulse width is at least half the period of the highest sampling clock specified in the data sheet. The test result proves that the ADS82x family has a very stable and solid SNR of 10 bits of resolution in both uniform and non-uniform high-speed sampling and converting operations, making it appropriate for wide use in future applications.

Figure 8. FFT output with 50-MHz uniform sampling (Case 1)

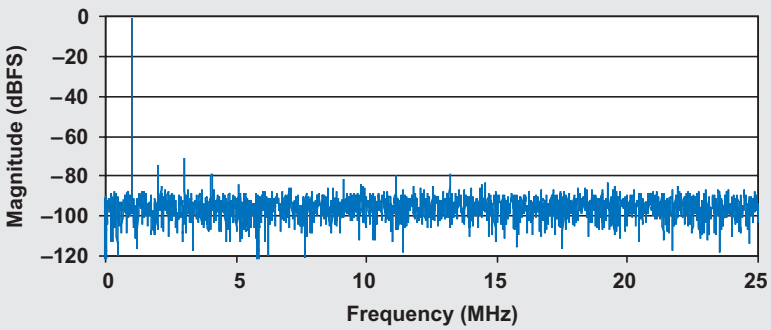


Figure 9. Case 2 FFT outputs with 10-MHz downsampling frequency

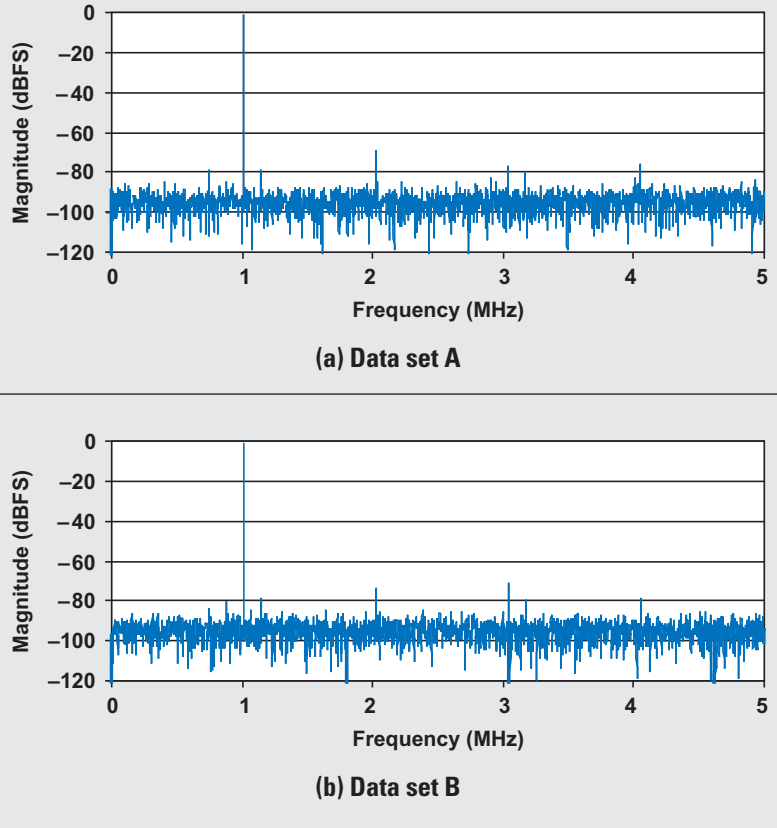
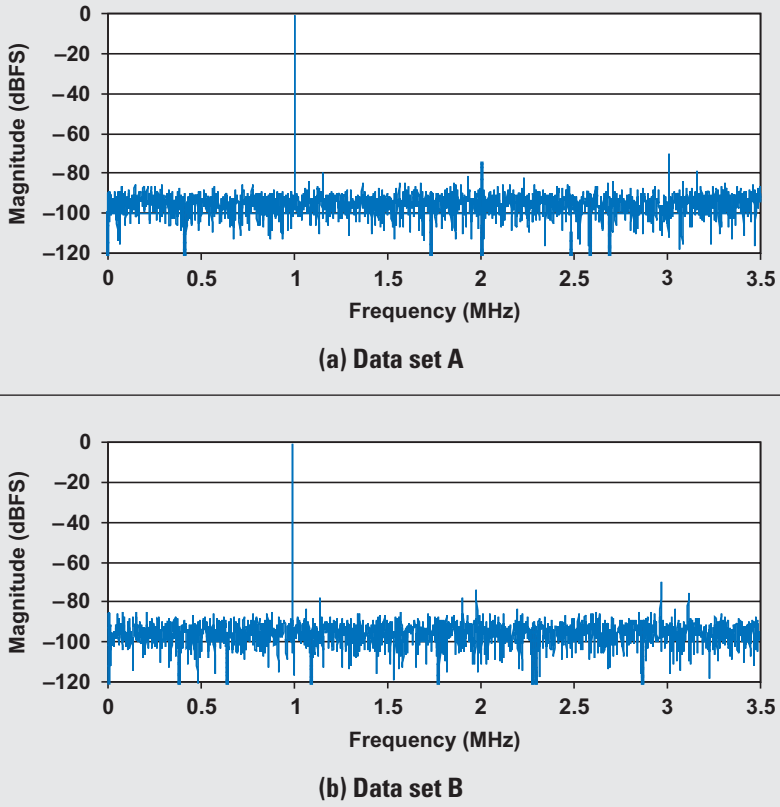


Figure 10. Case 3 FFT outputs with 7.14-MHz downsampling frequency



References

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Document Title	TI Lit. #
1. "DEM-ADS82xE Evaluation Fixture," User Guide	sbau036
2. "10-Bit, 60MHz Sampling Analog-to-Digital Converter," Data Sheet	sbas070
3. Alan V. Oppenheim and Ronald W. Schafer, *Discrete-Time Signal Processing* (Prentice-Hall, Inc., 1989).	—

Acknowledgments

Special thanks go to Bryan McKay and Rosie Loaiza for their support on the test board and to Stephan Baier for his article review.

Related Web sites

analog.ti.com

www.ti.com/sc/device/*partnumber*

Replace *partnumber* with ADS822, ADS823, ADS825, ADS826, ADS828 or OPA642

Calculating noise figure and third-order intercept in ADCs

By James Karki (Email: j-karki@ti.com)
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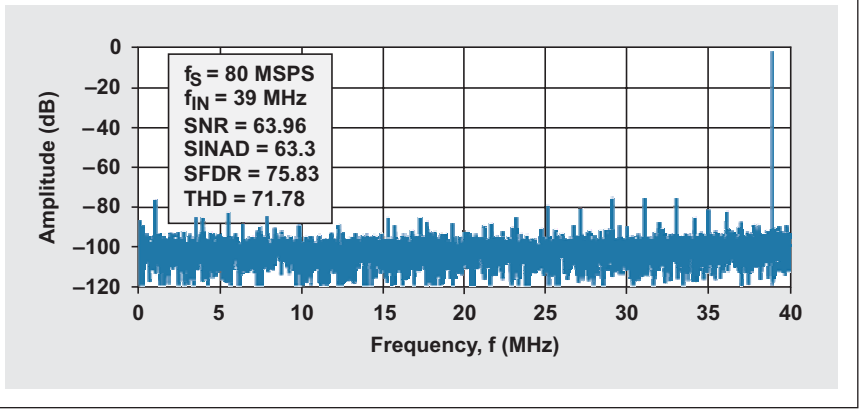
Introduction

Noise figure (NF) and the third-order intercept point (IP_3) are used in radio receiver link budget analysis as a means to quantify the effects of device noise and nonlinearity on the sensitivity of the radio. Analog-to-digital converters (ADCs) are used in radio receivers to convert the signal from the analog domain to the digital domain. NF and IP_3 typically are not specified for the device, but equivalent parameters are given whereby they can be calculated.

ADCs specify signal-to-noise ratio (SNR) and two-tone, third-order intermodulation distortion (IMD_3) under certain input signal and clocking conditions. With this information, NF and IP_3 can be calculated.

In general, a low NF and high IP_3 are desired. The actual values required to meet the design goals depend on the architecture of the system.

Figure 1. ADS5410 FFT or spectral plot from Reference 1



Review of noise figure

Noise figure (NF) is the decibel equivalent of noise factor (F): NF (dB) = 10log(F).

Noise factor of a device is the power ratio of the SNR at the input (SNR_I) divided by the SNR at the output (SNR_O):

$$F = \frac{SNR_I}{SNR_O}. \quad (1)$$

The output signal (S_O) is equal to the input signal (S_I) times the gain: $S_O = S_I \times G$. The output noise is equal to the noise delivered to the input (N_I) from the source plus the input noise of the device (N_A) times the gain: $N_O = (N_I + N_A) \times G$. Substituting into Equation 1 and simplifying, we get

$$F = \frac{SNR_I}{SNR_O} = \left[\frac{\frac{S_I}{N_I}}{\frac{G \times S_I}{G \times (N_I + N_A)}}\right] = 1 + \frac{N_A}{N_I}. \quad (2)$$

Assuming that the input is terminated in the same impedance as the source, $N_I = kT$ = –174 dBm/Hz, where k is Boltzman's constant and T = 300 Kelvin). Once we find the input noise spectral density of the device, it is a simple matter to plug it into Equation 2 and calculate F.

NF in ADCs

There are a couple of ways to go about calculating the input noise spectral density of an ADC, but using the SNR specification is easy.

To measure SNR, a low-noise signal is input to the ADC, and the output is examined by taking a fast Fourier transform (FFT) or spectral plot. Figure 1 shows such a plot from Reference 1. The ratio of the signal to the noise integrated over half the sampling frequency ($f_S/2$) is the SNR. Since the noise of the ADC is—to first-order approximation—independent of signal level, the higher the input level the better the SNR, up to a point. As the signal approaches full scale (FS), spurious behavior begins to degrade the SNR. An input signal level 1 dB below full-scale input (–1 dBFS) seems to give good results and is commonly used.

To find the input noise spectral density, we divide the signal level by the SNR divided by half the sampling frequency (since SNR is calculated by dividing the signal by the noise integrated over $f_S/2$):

N_A (dBm/Hz) = –1 dBFS (dBm) + SNR (dBc) – $f_S/2$ (dBHz).

An ADC is a voltage-driven device, so we must choose an input resistance to find the signal power with the formula $P = V^2/R$. Assuming that FS = $2V_{p-p}$ and R = 50 Ω, the full-scale input is +10 dBm.

As an example of how to calculate, consider the following for the ADS5410, a 12-bit ADC. Given that f_S = 80 MSPS, R_{IN} = 50 Ω, FS = $2V_{p-p}$, and SNR = 63.96, then

N_A (dBm/Hz) = +9 dBm – 63.96 dBc – 76.02 dBHz
= –130.98 dBm/Hz.

To use Equation 2, we need to use the linear equivalents of N_I and N_A:

$$F = 1 + 10E\left(\frac{-130.98 + 174}{10}\right) = 20045,$$

or NF (dB) = 43.02 dB.

Looking at the result, we see that adding the 1 in Equation 2 makes very little difference since the noise figure is so high. Therefore, using

$$NF\ (dB) = N_A\ (dBm/Hz) - N_I\ (dBm/Hz)$$

introduces little error.

It is common practice to use a transformer or a fully differential op amp to drive high-performance ADCs differentially. This gives us the opportunity to use higher ADC input resistance. If NF is calculated based on 50 Ω, it is reduced by $\log_{10}$(impedance ratio).

For example, if we use a 1:4 impedance ratio (1:2 turns ratio) transformer, the input resistance is 200 Ω to match to a 50-Ω drive amplifier. The NF is reduced by $10 \times \log_{10}(200/50) = 6$ dB. Or, if we use a 1:16 impedance ratio transformer with 800-Ω input resistance, NF is 12 dB lower.

Review of third-order intercept point (IP_3)

Due to nonlinearity in the transfer function of all electronics, distortion is generated. With reference to the formula of a straight line, y = b + mx, nonlinearity is any deviation that the output (y) may have from a constant multiple (m) of the input (x) plus any constant offset (b).

Expanding the nonlinear transfer functions of basic transistor circuits into a power series is a typical way to quantify distortion products (see Reference 2). For example, transistors typically have an exponential transfer function (i.e., collector current vs. base emitter voltage), $y = e^x$, where x is the input and y is the output. Expanding e^x into a power series around x = 0 results in

$$e^x = 1 + x + \frac{x^2}{2} + \frac{x^3}{6} + \frac{x^4}{24} + \frac{x^5}{120} + \cdots + \frac{x^n}{n!}.$$

Figure 2 shows the function $y = e^x$ along with estimates that use progressively more terms of the power series.

The farther x is from 0, the more terms are required to estimate the value of e^x properly. If $x < 0.25$, the linear term 1 + x provides a close estimate of the actual function, and the circuit is linear. As x becomes larger, progressively more terms (quadratic, cubic, and higher-order distortion terms) are required to estimate e^x properly.

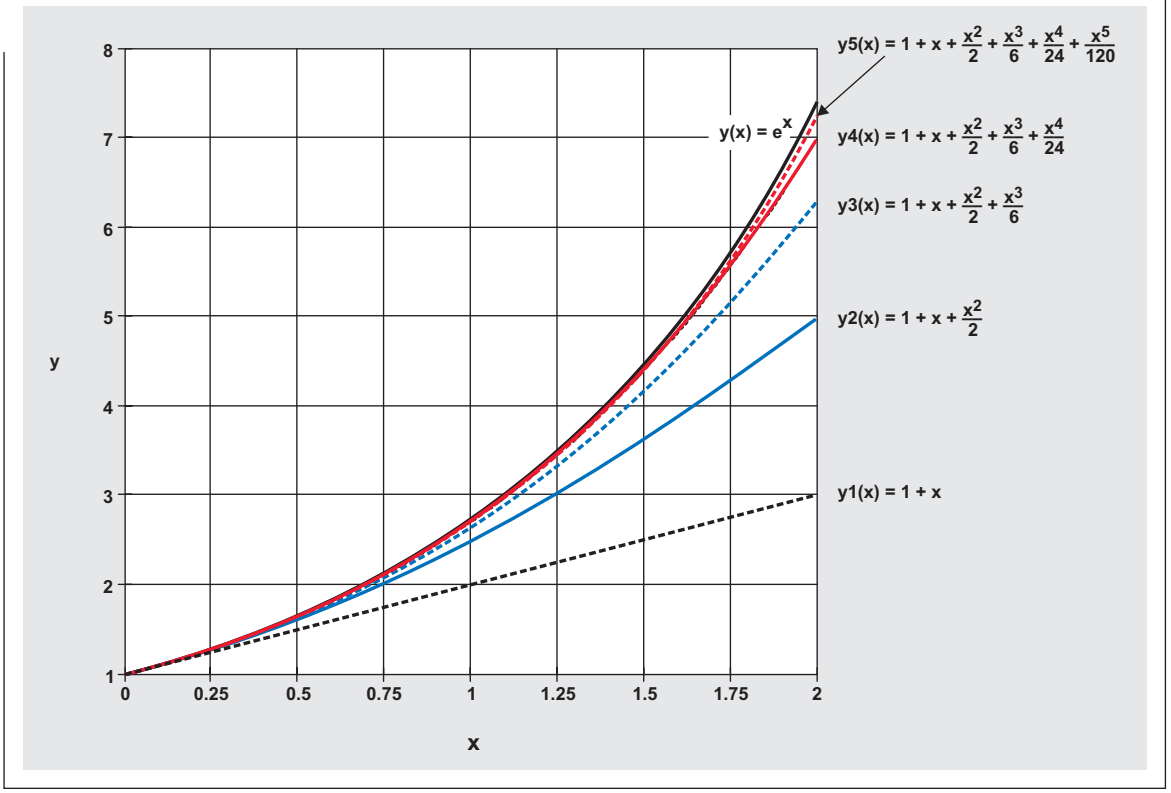
If the input to this circuit is a sinusoid—i.e., $x = A\sin(\omega t)$—then the output

$$y = K_0 + K_1 A\sin(\omega t) + K_2 A^2\sin^2(\omega t) + K_3 A^3\sin^3(\omega t) + \cdots,$$

where K_0, K_1, etc. are constant scaling factors. Using the trigonometric identities

$$\sin^2(\omega t) = \frac{1 - \cos(2\omega t)}{2} \text{ and}$$

Figure 2. Function $y = e^x$ and its power series estimates



$$\sin^3(\omega t) = \frac{3\sin(\omega t) - \sin(3\omega t)}{4}$$

shows that the quadratic and cubic terms give rise to second- and third-order harmonic distortion (HD_2 and HD_3, respectively). Similarly, higher-order terms give rise to higher-order harmonic distortion.

If the input is comprised of two tones—i.e., $x = A_1\sin(\omega_1 t) + A_2\sin(\omega_2 t)$—then the output

$$\begin{aligned} y = {} & K_0 \\ & + K_1[A_1\sin(\omega_1 t) + A_2\sin(\omega_2 t)] \\ & + K_2[A_1\sin(\omega_1 t) + A_2\sin(\omega_2 t)]^2 \\ & + K_3[A_1\sin(\omega_1 t) + A_2\sin(\omega_2 t)]^3 \\ & + \cdots, \end{aligned}$$

where K_0, K_1, etc. are constant scaling factors.

Expanding the third term, we get

$$\begin{aligned} & K_2[A_1\sin(\omega_1 t) + A_2\sin(\omega_2 t)]^2 \\ = {} & K_2[A_1^2\sin^2(\omega_1 t) + 2A_1A_2\sin(\omega_1 t)\sin(\omega_2 t) + A_2^2\sin^2(\omega_2 t)]. \end{aligned}$$

Using the trigonometric identities

$$\sin^2(\omega t) = \frac{1 - \cos(2\omega t)}{2} \text{ and}$$

$$\sin(\omega_1 t)\sin(\omega_2 t) = \frac{\cos(\omega_1 t - \omega_2 t) - \cos(\omega_1 t + \omega_2 t)}{2}$$

shows that the quadratic terms give rise to HD_2 and second-order intermodulation distortion (IMD_2).

Expanding the fourth term, we get

$$\begin{aligned} & K_3[A_1\sin(\omega_1 t) + A_2\sin(\omega_2 t)]^3 \\ = {} & K_3[A_1^3\sin^3(\omega_1 t) + 3A_1A_2\sin^2(\omega_1 t)\sin(\omega_2 t) \\ & + 3A_1A_2\sin(\omega_1 t)\sin^2(\omega_2 t) + A_2^3\sin^3(\omega_2 t)]. \end{aligned}$$

Using the trigonometric identities

$$\sin^3(\omega t) = \frac{3\sin(\omega t) - \sin(3\omega t)}{4} \text{ and}$$

$$\sin^2(\omega_1 t)\sin(\omega_2 t) = \frac{2\sin(\omega_2 t) - \sin(2\omega_1 t + \omega_2 t) - \sin(2\omega_2 t + \omega_1 t)}{4}$$

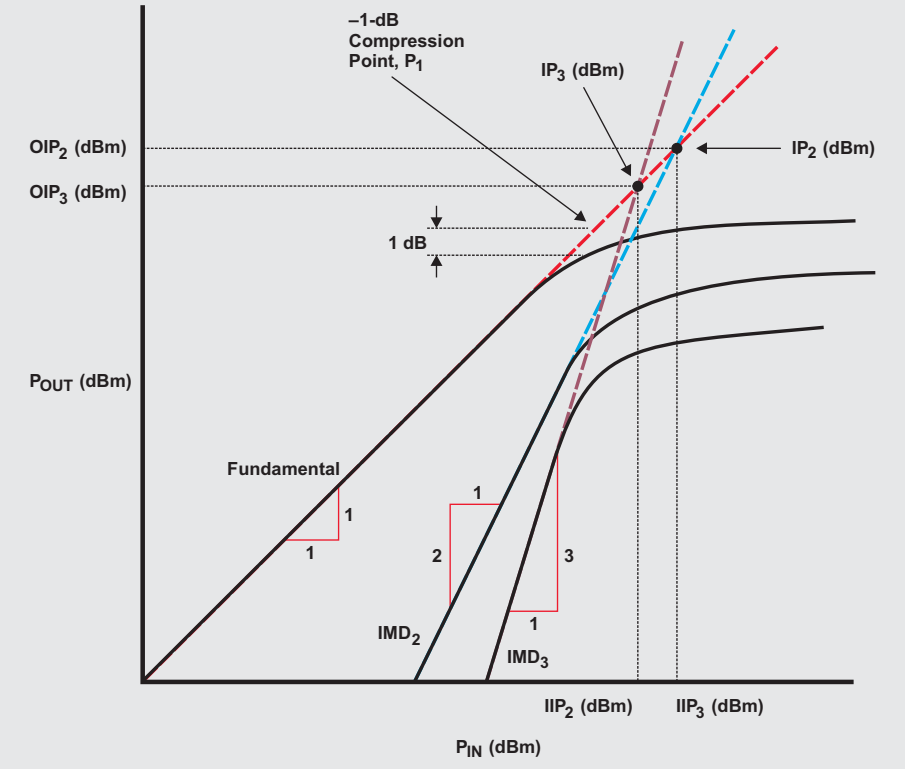
shows that the cubic terms give rise to HD_3 and third-order intermodulation distortion (IMD_3). Similarly, higher-order terms give rise to higher-order harmonic and intermodulation distortion.

Table 1 shows the frequencies of the distortion products that will be generated due to second- and third-order nonlinearity, given a two-tone input at frequencies f_1 and f_2.

Table 1. Distortion product frequencies due to second- and third-order nonlinearity

SECOND-ORDER FREQUENCIES		THIRD-ORDER FREQUENCIES	
$2f_1$	$2f_2$	$3f_1$	$3f_2$
$f_1 - f_2$	$f_1 + f_2$	$2f_1 - f_2$	$2f_2 - f_1$
		$2f_1 + f_2$	$2f_2 + f_1$

Figure 3. Input and output two-tone and intermodulation distortion



So now the question arises: Why is all this important? The answer is that radio specifications for GSM, CDMA2000, WCDMA, and the like all call for sensitivity requirements to be met with two interfering signals spaced in the frequency domain such that their third-order intermodulation product will fall on top of the signal of interest. The third-order intermodulation point is used to quantify how much distortion is generated. Referring this to the antenna input provides an easy method to determine whether or not the spec can be met.

If the input and output power of two tones applied to a device and their intermodulation products are graphed on a log-log scale as shown in Figure 3, the fundamental tones have a slope of 1, the second-order product has a slope of 2, and the third-order products have a slope of 3. The

device will go into compression before the lines intersect. The point where the output power is reduced by 1 dB from what is expected is called the 1-dB compression point (P_1). By extending the lines, the second- and third-order intercept points (IP_2 and IP_3, respectively) can be found. If they are referred to the input, they are called input intercept points (IIP_2, IIP_3); and if they are referred to the output, they are called output intercept points (OIP_2, OIP_3).

Since we are interested in intermodulation distortion relative to the carriers, why should we concern ourselves with some fictitious point that the amplifier will never reach? The answer is that there is a mathematical relationship between the two. Given the intercept point, we can calculate the intermodulation product for any input/output power.

Given that the slopes are known, equations for slopes L_1 and L_3 are written as shown in Figure 4.

Subtracting two arbitrary points on each line and rearranging gives us

$$y_2 - y_3 = x_2 - x_3 \quad \Rightarrow y_2 = y_3 + x_2 - x_3 \text{ for L1, and}$$
$$y_1 - y_3 = 3x_2 - 3x_3 \Rightarrow y_1 = y_3 + 3x_2 - 3x_3 \text{ for L3.}$$

Subtracting again results in

$$\begin{array}{l} y_2 = y_3 + x_2 - x_3 \\ \underline{-(y_1 = y_3 + 3x_2 - 3x_3)} \\ y_2 - y_1 = 2(x_3 - x_2). \end{array}$$

$\uparrow$ $\uparrow$ $\nwarrow$

IMD_3 (dBc) IIP_3 (dBm) P_{IN}

From this it is seen that

$$IIP_3\,(\text{dBm}) = P_{IN}\,(\text{dBm}) - \frac{IMD_3\,(\text{dBc})}{2}. \qquad (3)$$

Once we find IMD_3 and know the input power, it is a simple matter to plug them into Equation 3 and calculate IIP_3.

Figure 4. Straight-line relationship between IMD_3 and the fundamental

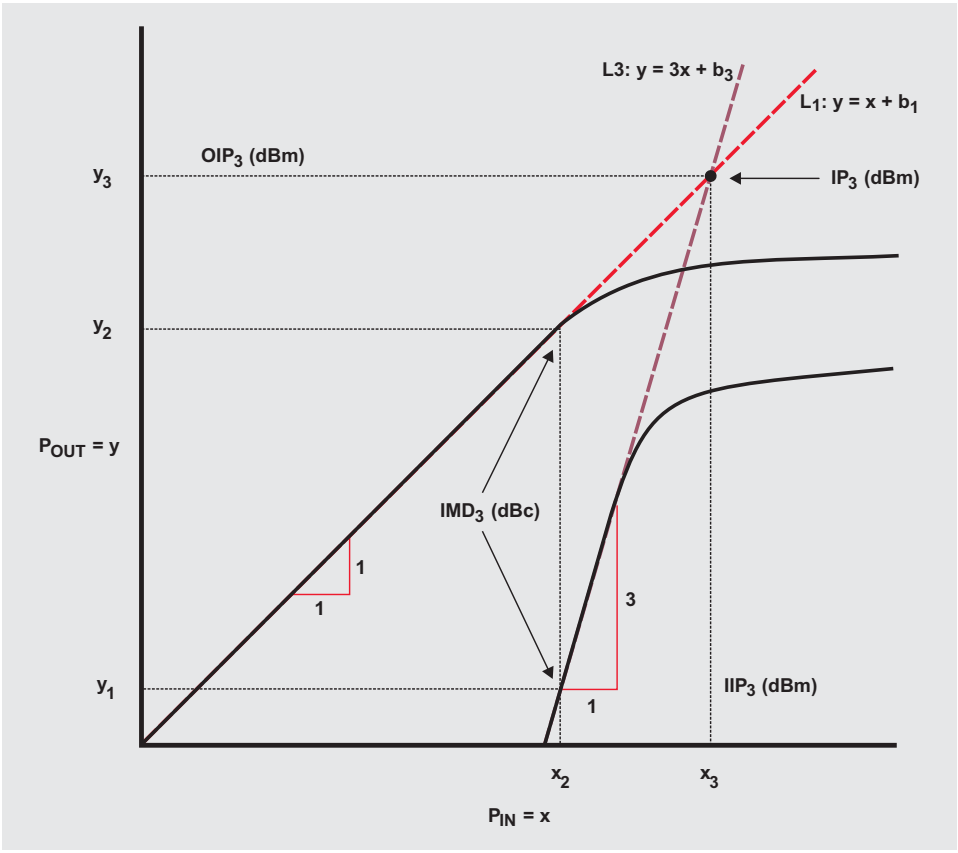
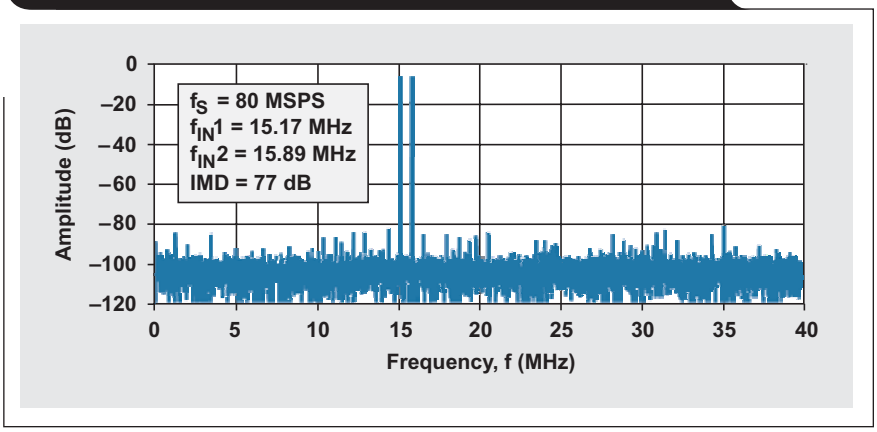


Figure 5. Two-tone FFT or spectral plot from Reference 1



IP_3 in ADCs

In ADC testing, two tones are applied to the ADC, and the output is examined by taking an FFT or spectral plot to find the two-tone IMD_3. Figure 5 shows such a plot from Reference 1. The ratio of each of the tones to the IMD_3 product(s) is the two-tone IMD_3 in dBc. IMD_3 depends on signal level. Too high a signal level results in excessive distortion, and too low a signal level makes distortion hard to detect in the presence of noise and other spurious components. An input signal level 7 dB below full-scale input (–7 dBFS) seems to give good results and is commonly used.

Since an ADC is a voltage-driven device, we must choose an input resistance to find the signal power with the formula $P = V^2/R$. Assuming that FS = $2V_{p-p}$ and R = 50 Ω, the full-scale input is +10 dBm. With the input power and the IMD_3, Equation 3 is used to find IIP_3.

As an example of how to calculate, consider the following for the ADS5410, a 12-bit ADC. Given that FS = $2V_{p-p}$, R_{IN} = 50 Ω, and IMD_3 = 77 dBc, then

$$IIP_3 = 3\ \text{dBm} - \frac{-77\ \text{dBc}}{2} = 41.5\ \text{dBm}.$$

As mentioned earlier, it is common practice to use a transformer or a fully differential op amp to drive high-performance ADCs differentially. If 50 Ω is originally used as shown in the example, then the IIP_3 is reduced by $10 \times \log_{10}$(impedance ratio).

For example, if we use a 1:4 impedance ratio (1:2 turns ratio) transformer, the input resistance is 200 Ω to match to a 50-Ω drive amplifier. The IIP_3 is reduced by $10 \times \log_{10}(200/50) = 6$ dB. Or, if we use a 1:16 impedance ratio transformer with 800-Ω input resistance, IIP_3 is 12 dB lower.

Conclusion

We have examined typical ADC noise and distortion specifications to see how they relate to NF and IP_3. It is seen that the required information to calculate NF and IP_3 is contained in a typical ADC data sheet.

A key point to remember is that an ADC is a voltage-driven device, whereas NF and IP_3 are associated with power. Thus, in order for the calculations to proceed, an impedance is imposed on the ADC input to find the corresponding power levels.

References

For more information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/*litnumber* and replace *"litnumber"* with the **TI Lit. #** for the materials listed below.

Document Title **TI Lit. #**

1. "12-Bit, 80 MSPS CommsADC™ Analog-to-Digital Converter," Data Sheet, p. 7 . . . . . .slas346
2. Piet Wambacq and Willy Sansen, *Distortion Analysis of Analog Integrated Circuits* (Kluwer Academic Publishers, 1998).

Related Web sites

analog.ti.com
www.ti.com/sc/device/ADS5410

Evaluation criteria for ADSL analog front end

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Introduction

The latest ADSL standard proposed by the International Telecommunication Union (ITU), with the draft recommendation G.992.3-ADSL2, is the next evolution for second-generation ADSL. A summary of the first-generation ADSL evaluation and design criteria is helpful in understanding first-generation ADSL in the mass market and in designing the specifications for second-generation ADSL.

The AFE1302 customer premise equipment (CPE) modem is one practical ADSL analog front end (AFE) design and evaluation example. In this design, an AFE1302 chip and AFE reference design printed circuit board are used for the ADSL CPE modem and CPE PCI card. The maximum reach of the CPE modem is an 18,000-ft (5.5-km) loop with a downstream net bit rate of 928 Kbps and an upstream rate of 416 Kbps.

The maximum transmitted power is defined by ITU G.992 power spectral density (PSD) mask requirements. The crosstalk from coexisting ADSL and ISDN lines can be minimized by limiting the maximum strength of the transmitted ADSL signal power over the twisted-pair long wires. In addition, Electromagnetic Compatibility Society legislation requires that the ADSL transmission system not interfere with AM/FM radio reception. These two requirements place a PSD limit on the strength of the transmitted ADSL signal power.

This article discusses some evaluation and design considerations for addressing transmitted data speed, telephone twisted-pair loop attenuation, the hybrid circuit, and the multitone power ratio (MTPR).

Transmitted data speed and the total signal-to-noise ratio

Transmitted data speed is the first consideration for ADSL CPE modem design and evaluation. The transmitted data speed is a function of the total signal-to-noise ratio (SNR). The total SNR is the telephone loop SNR plus the modem receive path SNR.

The discrete multitone (DMT) modulation was standardized for the ADSL system by the telecommunication standardization sector of the ITU. For DMT-based ADSL, each subcarrier or tone is spaced at 4.312-kHz intervals. The subcarrier assignment is defined by ITU standard G.992. For example, the subcarrier assignment in G.992.1 annex A can be used for frequency division multiplexing to separate upstream and downstream signals. The subcarriers 31–255 (ITU G.992.1), or subcarriers 31–127 (ITU G.992.2), are reserved for downstream. The subcarriers 0–30—e.g., a maximum total of 31 subcarriers—may be assigned for upstream. The lowest-frequency subcarriers may be set to zero to allow for voice on the same line, such as in plain old telephone service (POTS).

The lowest-frequency subcarrier used for upstream is determined by the POTS/ADSL splitting filter. The number of upstream and downstream subcarriers is determined by the receive and transmit filters. The actual number of subcarriers employed to modulate data may be less than the maximum and is determined during the initialization sequence. The transmitter designates a subset of the maximum available subcarriers for a connection during the channel analysis phase.

The process of ADSL DMT modulation actually modulates each subcarrier as $2^{b(i)}$ quadrature amplitude modulation (QAM). The superscript b(i) denotes the number of bits in the i*th* subcarrier. Subcarriers with a lower SNR will be assigned fewer bits to do a small-number QAM constellation. Subcarriers with a higher SNR will be assigned more bits to create a large-number QAM constellation. Suppose that the i*th* subcarrier is assigned 8 bits; then the size of the carrier QAM constellation is $2^8 = 256$ QAM.

The bits are determined by the SNR measured during the channel analysis initialization procedure. The initialization of the CPE modem is performed in five steps: Handshake procedures, channel discovery, transceiver training, channel analysis, and exchange.

During the exchange phase, each receiver communicates to its far-end transmitter the number of bits and relative power levels used on each DMT tone or subcarrier, as well as the final data rate information. After the successful initialization sequence, the transceivers can start communication with actual data.

The channel analysis phase is used to measure the channel characteristics for both directions of transmission. In other words, it measures the channel transfer function versus the frequency response characteristic. The downstream channel characteristics are measured at the CPE side, and the upstream channel characteristics are measured at the central office (CO) side.

During the channel analysis phase, the receiver estimates the transmitted channel gain of each subcarrier in preparation for computing the total SNR for each subcarrier. Then each subcarrier is assigned the number of bits it will carry. The sum of all the bits assigned to all of the subcarriers within the transmitting period (per DMT symbol) determines the transmitted data speed.

The number of bits assigned per subcarrier can be calculated by

$$b(i) = \log_2[1 + snr(i) \times g/\gamma \times m]. \quad (1)$$

Further, $2^{b(i)} - 1 = snr(i) \times g/\gamma \times m$, and

$10\log_{10}[2^{b(i)} - 1]$
$= 10\log_{10}[snr(i)] + 10\log_{10}(g) - 10\log_{10}(\gamma) - 10\log_{10}(m)$.

Only if $2^{b(i)} >> 1$ is the following equation true:

$10\log_{10}[2^{b(i)}] = SNR\ (dB) + G\ (dB) - \Gamma\ (dB) - M\ (dB)$.

Therefore,

$b(i) = [SNR\ (dB) + G\ (dB) - \Gamma\ (dB) - M\ (dB)]/3\ dB\ (bits)$. **(2)**

Variable definitions for the preceding equations are as follows:

- b(i) is the number of bits in the *ith* subcarrier.
- i is the subcarrier index from 0 to N – 1; N is the total usable subcarrier number; and the maximum N = 256.
- snr(i) is the SNR per subcarrier; it is a real value that represents the ratio between the received signal power and the received noise power for that subcarrier. SNR (dB) = $10\log_{10}[snr(i)]$.
- γ or Γ is a constant determined by the required bit error rate (BER). For example, $\gamma = 9.55$ and $\Gamma = 10\log_{10}(\gamma) = 9.8$ (dB) for BER $\leq 10^{-7}$.
- g or G = $10\log_{10}(g)$ (dB) is a gain provided by Reed-Solomon error correction coding to make the system robust against impulsive noise bursts.
- m or M = $10\log_{10}(m)$ (dB) is the margin to represent the amount of increased noise relative to the noise power that the system is designed to tolerate and still meet the target BER of $10 \times e^{-7}$, accounting for all coding (trellis coding and Reed-Solomon forward error correction) gains included in the design. This margin can prevent too many bits from swapping if the SNR changes. Normally M = 6 dB is used to prevent online swapping.

G (dB), Γ (dB), and M (dB) are constants. One bit is added to the assigned b(i) if SNR (dB) increases 3 dB in the subcarrier channel; this is the "one-bit-per-3-dB" rule.

Assuming that G (dB) = 2 dB, Γ (dB) = 9.8 dB, and M (dB) = 6 dB, a typical b(i) and SNR (dB) versus the tone number is shown in Figure 1.

The transmitted data speed can be calculated by

$$C = [\Sigma b(i)]/t \text{ for } i = 0 \text{ to } N - 1,$$

where C is the transmitted data speed and t is the transmission period.

Example 1: If the gain of trellis and Reed-Solomon coding is not included, the attainable net rate or the maximum data rate is

$$C = \{\Sigma[SNR\ (dB) - \Gamma\ (dB) - M\ (dB)]/3\ dB\}/t\ (bps)$$

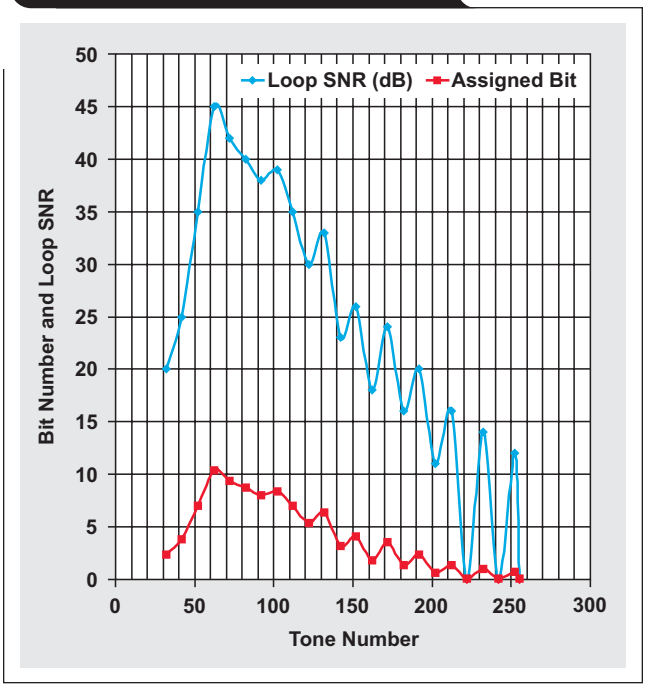
for i = 0 to NSC – 1, where NSC is the number of subcarriers.

Example 2: Additionally, if M = 6 dB and G = 6 dB, the attainable net rate can be simplified as follows:

$$C = \{\Sigma[SNR(i) - \Gamma]/3\ dB\}/t\ (bps)$$

for i = 0 to NSC – 1. For the duration of a DMT symbol, t = 250 µs. The data symbol rate (4000 data symbols/second) is the net average rate at which symbols carrying data frames are transmitted. However, in order to insert the synchronization symbol, the symbol rate is defined as the rate at which all symbols, including the synchronization symbol, are transmitted; that is, (69/68) × 4000 = 4058.8 symbols/second.

Figure 1. Bit assignment and loop SNR relationship



From the equation given earlier, the transmitted data speed is determined by the total SNR. The modem RX path noise is not covered in this article. The transmitted DMT signal power and loop noise are specified in the recommended ITU G.992 as follows:

- For G.992.1, the downstream PSD is –40 dBm/Hz, from 25.875 to 1104 kHz, for a total transmission power not greater than 20.4 dBm if all subcarriers are used.
- For G.992.2, the downstream PSD is –40 dBm/Hz, from 25.875 to 552 kHz, for a total transmission power not greater than 16.2 dBm if all subcarriers are used.
- The upstream normal transmit PSD, for the channel analysis signal (R-REVERB1) and all subsequent upstream signals, is –38 dBm/Hz, which is equivalent to –1.65-dBm total transmit power in any 4.3125-kHz subcarrier. The maximum transmit PSD should be no higher than –37 dBM/Hz, for an aggregate transmit power not greater than 12.5 dBm if all subcarriers are used.
- The telephone loop noise is assumed to be 31.62 nV/$\sqrt{Hz}$, or –140 dBm/Hz. It is specified as the quiet line noise PSD N(f) for a particular subcarrier in G.992.3-ADSL2; and it is the rms level of the noise present on the telephone line when no ADSL signals are present on the line.

A practical evaluation result of the transmission channel capacity is the net data speed for the AFE1302 CPE

modem. The evaluation is based on using the subcarriers 36–127 for downstream with a total transmission power of less than 15.99 dBm during the training phase and less than 6.06 dBm during the SHOWTIME state. The SHOWTIME state is the normal operation state after all initialization and training are completed. Taking into account all noise contributions, the loop noise test results referred to the telephone line are less than –148 dBm/Hz over receiver bandwidth for the AFE1302 CPE modem. The tested downstream net bit rate can reach 928 Kbps with an 18,000-ft (5.5-km) loop. For the test environments, the loop simulator NSA400 is set as a 26-AWG twisted-pair telephone wire without a bridged tap, the noise margin is 6 dB, and the interleave depth is 16 with no trellis coding.

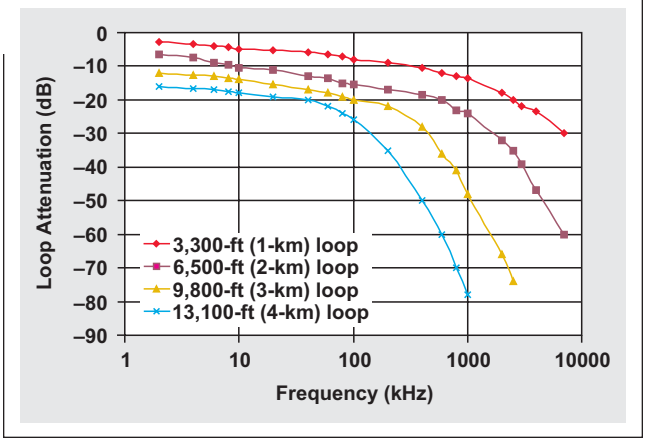
Twisted-pair telephone-loop attenuation

The reach of an ADSL system is the distance over telephone lines that it can transmit and receive information. Reach is the key performance parameter for ADSL and is limited by twisted-pair telephone-loop attenuation.

Telephone-loop attenuation is defined as the difference between the total maximum transmitted power at one end of the telephone line and the total received power at the other end of the line. Loop attenuation is mainly dictated by wire diameters, loop length, and the transmitted signal frequency. The most frequently used telephone twisted-wire diameters are 0.4 mm for 26-AWG wire and 0.5 mm for 24-AWG wire. The typical loop length varies from 6,000 to 18,000 ft (1.8 to 5.5 km) in North America, Europe, and Asia. ADSL signals cover the bandwidth of 25.875 kHz to 1104 kHz as specified in ITU G.992.

According to POTS application statistics, the typical voice signal loss through a telephone loop is 3 to 6 dB per mile (1.6 km) within the voice bandwidth of 300 Hz to 4 kHz. Because ADSL signal frequency is much higher than the POTS signal, and because line attenuation increases as signal frequency increases, the loop attenuation is greater within the ADSL signal bandwidth.

Figure 2. A 24-AWG twisted-pair telephone-loop attenuation vs. frequency



The transfer function of a twisted-pair telephone loop is dominated by the skin effect: High-frequency currents tend to flow only in the outer portion, or skin, of the conductor, resulting in an increase of the attenuation at higher frequencies. In the case of a twisted-pair loop, the attenuation is a function approximately proportional to $f^{1/4}$ for frequencies below 350 kHz, and approximately proportional to $f^{1/2}$ for frequencies above 350 kHz.

The experimental data in Figure 2 shows that the loop attenuation increases from around 5 dB per 3300 ft (1 km) at 10 kHz to over 15 dB per 3300 ft (1 km) at 1 MHz. This means that a 13,100-ft (4-km), 24-AWG twisted-pair telephone loop has an attenuation of over 20 dB at 100 kHz, and over 70 dB at 1 MHz. Over the ADSL signal bandwidth, the twisted-pair loop attenuation varies by more than 50 dB.

During channel analysis, the CO-side receiver calculates the average loop attenuation. Based on the channel analysis signal (R-REVERB1) using subcarriers 7–18, the average upstream loop attenuation is calculated as the difference between the total transmitted power at the CPE side and the total received power measured at the CO side. In G.992.3-ADSL2, for a given loop length, the loop attenuation is defined as

$$\text{LATN (dB)} = 10 \times \log[\Sigma|H(f)|^2/\text{NSC}]$$

for i = 0 to NSC – 1. Variables for this equation are defined as follows:

- NSC is the number of subcarriers.
- H(f) is the channel characteristic function per subcarrier.
- LATN is the difference in decibels between the power received at the near end and that transmitted from the far end over all subcarriers; its dynamic range is from 0 to 102.2 dB.

For example, assume that LATN = 58.2 dB, N = –140 dBm/Hz, G = M = 6 dB, the transmitted signal power is –30 dBm/Hz, and the received signal power is S = –88.2 dBm/Hz for a particular subcarrier. With Equation 2, b(i) can be calculated as 14 bits, which means that 14 bits of data can be assigned on that subcarrier. But if LATN increases to 88.2 dB for a longer loop, then b(i) is only 4 bits because of the one-bit-per-3-dB rule.

A longer-reach loop and a higher subcarrier frequency result in greater loop attenuation, which means that fewer data bits can be assigned to subcarriers, and lower data speed can be achieved.

Hybrid circuit

The ADSL hybrid circuit is a three-port network used to pass the transmit signal from the AFE transmission port to the telephone-loop port and to pass the receive signal from the telephone loop port to the AFE receive port. The ADSL hybrid circuit is also used to eliminate the transmit signal from the receive signal in the receive path. It allows full-duplex transceiver operation in a twisted-pair telephone loop. ADSL hybrid echo return loss is the amount of attenuation between the transmitted signal power and the reflected echo power in the receive path, normally

expressed in decibels. It is a key target of evaluation and design for an ADSL AFE. The higher the echo return loss, the less of the transmitted signal power gets into the receive path.

$$H_{echo} = 10 \times |\log(P_{echo}/P_{tx})|,$$

where H_{echo} is the hybrid echo return loss, P_{tx} is the transmitted signal power, and P_{echo} is the portion of transmitted power that enters the receive channel (also called the reflected echo power in the receive path).

The actual twisted-pair loop impedance Z(f) is the frequency function of the telephone line. The magnitude of the twisted-pair impedance is about 600 Ω for the POTS bandwidth; but for the ADSL signal bandwidth, it is about 100 Ω without bridged taps and varies from 60 to 100 Ω with bridged taps.

The hybrid circuit used in the AFE1302 CPE modem is purely resistive and basically an electrical bridge circuit. When the differential drive resistive network becomes balanced, the amount of hybrid echo is minimized.

In a DMT-based ADSL system, the ADSL hybrid circuit and the receive path filter are the critical factors for receiver performance. The transmit path signal and noise power need to be sharply attenuated by the hybrid echo path and receive filter. They can significantly improve CPE modem reach and downstream data speed.

For the typical value of 100-Ω equivalent twisted-pair loop impedance, a total 40-dB attenuation of a hybrid circuit and receive high-pass filter is the minimum evaluation and design requirement. A 20-dB return loss can be easily achieved through the hybrid circuit. The hybrid plus the third-order, LC RX filter on-board can provide a total echo loss of more than 40 dB. That is, the hybrid circuit can attenuate the transmitted power and noise by 40 dB (see Figure 3).

The multitone power ratio

The multitone power ratio (MTPR) is an important feature in the evaluation and design of DMT-based ADSL systems. Better MTPR performance in both the transmission and receive paths results higher data rates in the ADSL system.

The MTPR is the ratio of the power in one subcarrier to the noise power in another selected empty subcarrier. There are no data bits assigned to the selected empty subcarrier in a DMT modulation. The MTPR indicates the degree to which a subcarrier QAM signal is corrupted by distortion from all other subcarrier QAM signals.

The measurement and evaluation for this kind of corruption are different from that for traditional single-tone distortion. Signal-to-noise and distortion ratio (SINAD), spurious-free dynamic range (SFDR), single-tone harmonic distortion, two-tone intermodulation distortion (IMD), third-order intercept point (IP_3), and total harmonic distortion (THD) are used only for expressing single- or two-tone signal integrity and spectral properties.

The MTPR, on the other hand, indicates how the tested device—such as line driver, receiver, line transformer, TX filter, RX filter, or DAC/ADC—responds to the discrete multitone signal, which is not 1 or 2 tones but may be up to 255 or more.

One of the design tasks for the ADSL CPE modem is to maintain the fidelity of the discrete multitone signal. All the analog components used on the modem—such as line transformer, common-mode choke, hybrid circuit, TX filter, RX filter, and line driver and receiver—must be designed so that they cause minimal corruption of the discrete multitone signal.

For any subcarrier, the minimum transmitter MTPR shall be at least 38 dB as specified in G.992, and at least 44 dB as recommended by G.992.3.

Figure 3. Hybrid echo return loss plus RX filter attenuation vs. frequency

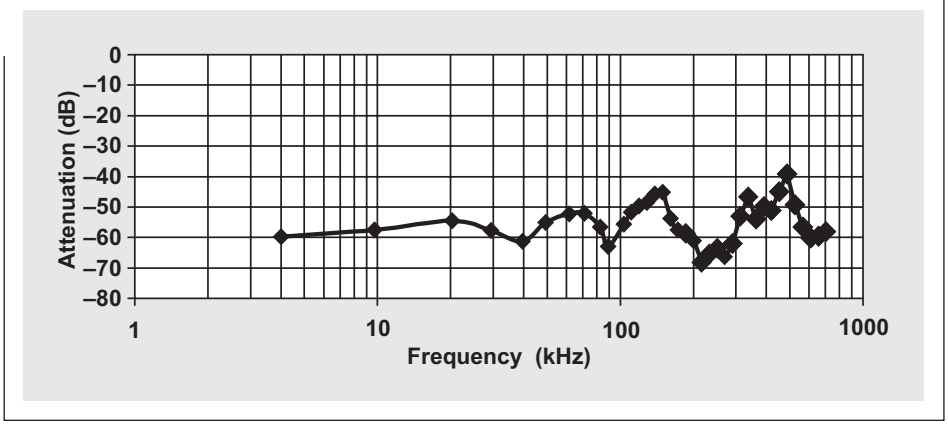
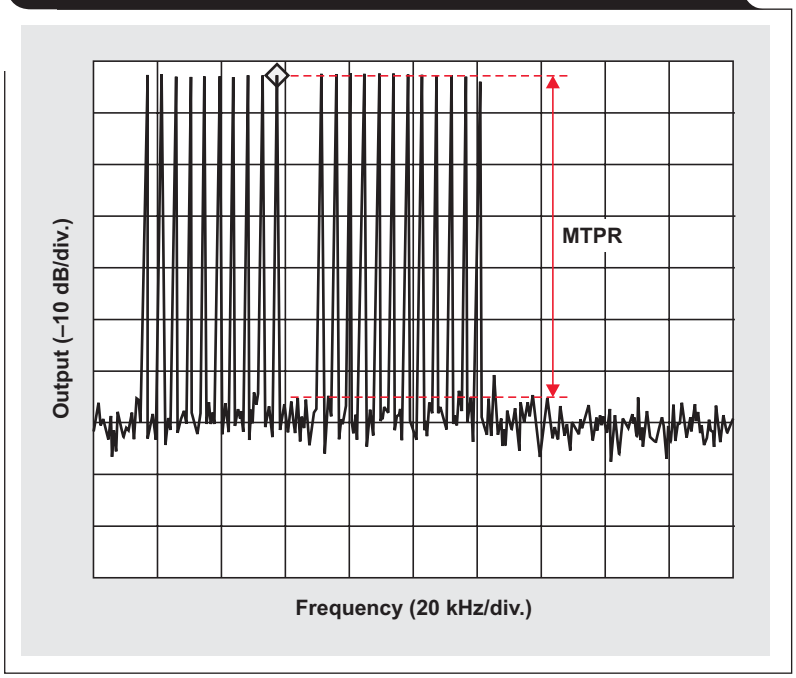


Figure 4. Transmitter path MTPR performance of AFE1302



The MTPR of a tested device can be measured as the dynamic range from peak power in a subcarrier to the peak distortion in an empty tone. For example, a test result shows that an MTPR of 65.82 dB can be achieved in the AFE1302 CPE modem transmission path. The test tool is National Instruments PXI-1002 arbitrary waveform generator 5411.

The transmitter path is defined as the path from the DSP interface TX output to the twisted-pair telephone line interface with 100-Ω impedance (see Figure 4). The transmitted multitone signal is from tones 6–29 and with notch tones 16 and 17. The internal AFE1302's TX programmable gain amplifier gain is 0 dB, and the external TX line driver gain is 15 dB. The tested result of the MTPR is 65.82 dB.

Summary

This article has discussed some evaluation and design considerations for an ADSL AFE. The most critical evaluation criterion is an ADSL transceiver data speed that is limited by the total SNR. The second issue is frequency variation of telephone-loop attenuation and its impact on reach. This article further pointed out that the improvement on hybrid echo return loss significantly increases the received data speed and the reach. The MTPR, a kind of corruption that differs from the traditional single-tone distortion, is another important criterion for designing and evaluating an ADSL AFE.

References

For more information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/*litnumber* and replace *"litnumber"* with the **TI Lit. #** for the materials listed below.

Document Title	**TI Lit. #**
1. "ITU-T Draft Recommendation G.992.3-ADSL2," International Telecommunication Union, Geneva, Switzerland, April 29–May 10, 2002.	—
2. "ADSL Analog Front-End," Data Sheet	sbws014

Related Web sites

analog.ti.com
www.ti.com/sc/device/AFE1302

UCC28517 100-W PFC power converter with 12-V, 8-W bias supply, Part 2

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Introduction

Power factor corrected (PFC) preregulators are generally used in offline ac/dc power converters with a power level higher than 75 W or to meet line harmonic requirements such as EN61000-3-2. PFC is typically done with a boost converter ac/dc topology due to the continuous input current that can be manipulated through average current-mode control to achieve a near-unity power factor (PF). However, due to the high output voltage of a boost converter, a second dc/dc converter is generally needed to step down the output to a usable voltage. In the past this has been accomplished with two pulse-width modulators (PWMs). One PWM controlled and regulated the PFC power stage, while the second was used to control the step-down converter. The UCC28517 controller reduces the need for two PWMs and combines both of these functions into one control-integrated circuit. The UCC28517 operates the second converter at twice the switching frequency of the PFC stage, which reduces the size of the boost magnetics and the ripple current in the boost capacitor. For more information on this device, please see Reference 7. This article reviews the design of the second 12-V, 8-W power stage to be used as an auxiliary bias supply. A review of the PFC preregulator power stage can be found in the 3Q03 issue of the TI *Analog Applications Journal*.

Variable definitions

Δt	Soft-start interval
$\eta 1$	Output A efficiency
$\eta 2$	Output B efficiency
C_{DIODE}	Boost diode capacitance
C_{OSS}	FET drain-to-source capacitance
D_{max}	Duty cycle maximum
ESR	Output capacitance equivalent resistance
f_c	Voltage-loop crossover frequency
f_{opto_pole}	Frequency where optoisolator gain is –3 dB from its dc operating point
f_S	Minimum switching frequency
f_{SA}	Output A switching frequency
f_{SB}	Output B switching frequency
$G_{c(s)}$	Control transfer function
$G_{co(s)}$	Control to output transfer function
$G_{opto(s)}$	Optoisolator gain transfer function
$H_{(s)}$	Voltage divider gain
I_m	Transformer magnetizing current
I_{op_min}	Minimum optocoupler current (1 mA)
I_{PK}	Peak inductor current, peak diode current, peak switch current
I_{RMS}	RMS device current
I_{SS}	UCC28517 soft-start current of 10 µA
L_m	Transformer primary magnetizing inductance
N	Transformer turns ratio
N_p	Primary turns
N_s	Secondary turns
P_{COND}	Device conduction losses
P_{COSS}	Power dissipated by the FET's drain-to-source capacitance
P_{DIODE}	Total loss in the boost diode
P_{DIODE_CAP}	Loss due to boost diode capacitance
P_{FET_TR}	FET transition losses
P_{GATE}	Power dissipated by the FET gate
P_{OUTA}	Output A maximum power
P_{OUTB}	Output B maximum power
Q_{GATE}	FET gate charge
$R_{DS(on)}$	On resistance of the FET
R_{load}	Typical load impedance
R_{SENSE}	Current sense resistor
s	Angular frequency ($j2\pi f$)
t_{blank}	Amount of leading-edge blanking time
t_f	FET fall time
t_r	FET rise time
T_{SB}	$1/f_{SB}$ = 5 µs
$T_{s(f)}$	Voltage loop frequency response
V_{boost}	Same as V_{OUTA}
V_c	Control voltage
V_{ct}	Oscillator peak (5 V)
V_d	Forward diode drop (0.6 V)
$V_{dynamic}$	Current sense voltage range
V_f	Forward voltage of a diode
V_{GATE}	Gate-drive voltage
V_{IN}	RMS input voltage
V_{OUTA}	Boost output voltage (V_{boost})
V_{OUTB}	Auxiliary output voltage
V_{pp}	Output peak-to-peak ripple voltage
V_{REF}	UCC28517 internal reference
V_{ripple}	Output B ripple voltage
V_{slope}	Voltage ramp peak added for slope compensation
V_{VERR}	Feedback error voltage
V_{VREF_TL431}	TL431 (D13) internal reference

Table 1. Design specifications

	MAXIMUM	TYPICAL	MINIMUM
V_{IN}	265 V_{rms}		85 V_{rms}
Output A (V_{OUTA})	410 V	390 V	370 V
Output B (V_{OUTB})	12.6 V	12 V	11.4 V
Output A efficiency (η1)		85%	
Output B efficiency (η2)		50%	
P_{OUTA}	100 W		10 W
P_{OUTB}	8 W		4 W
Output ripple A (V_{pp})	12 V		
Output ripple B (V_{ripple})	750 mV		
Output A THD (% THD)	10%		
PF	1		
Output A switching frequency (f_{SA})		100 kHz	
Output B switching frequency (f_{SB})		200 kHz	

The following design example was generated using typical parameters rather than worst-case values. Please refer to Table 1 and Figures 1–3 for design specifications and component placement. All variables are defined in the sidebar on page 21.

12-V, 8-W auxiliary converter (OUTB)

Due to the high input voltage from the boost converter, this design required a dc/dc converter with a step-down transformer to achieve the desired output voltage of 12 V. The low power requirements permitted use of a discontinuous-mode flyback topology, which uses fewer components than a standard forward converter.

Transformer turns ratio

The following equation can be used to calculate the transformer turns ratio (N) needed for this power stage.

$$N = \frac{D_{max} \times V_{OUTA} \times T_{SB}}{(0.9 - D_{max}) \times (V_{OUTB} + V_d) \times T_{SB}}$$

The UCC28517 PWM/PFC controller has a user-selectable duty-cycle clamp. For this design the duty-cycle clamp was set to a D_{max} of 0.55. The UCC28517 has a forward enable comparator that will not allow the forward converter to operate with a boost voltage less than 50% of the nominal value. This allows the cascaded step-down converter to

Figure 1. PFC power stage schematic

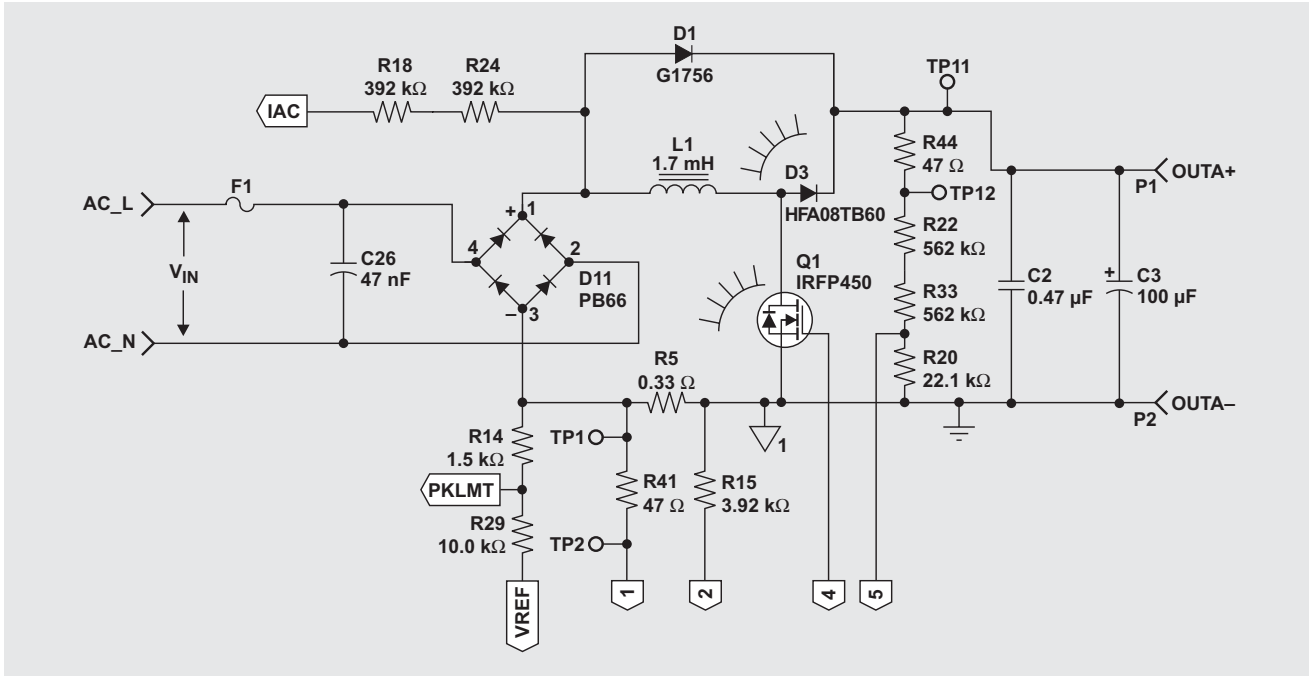


Figure 2. dc/dc power stage schematic

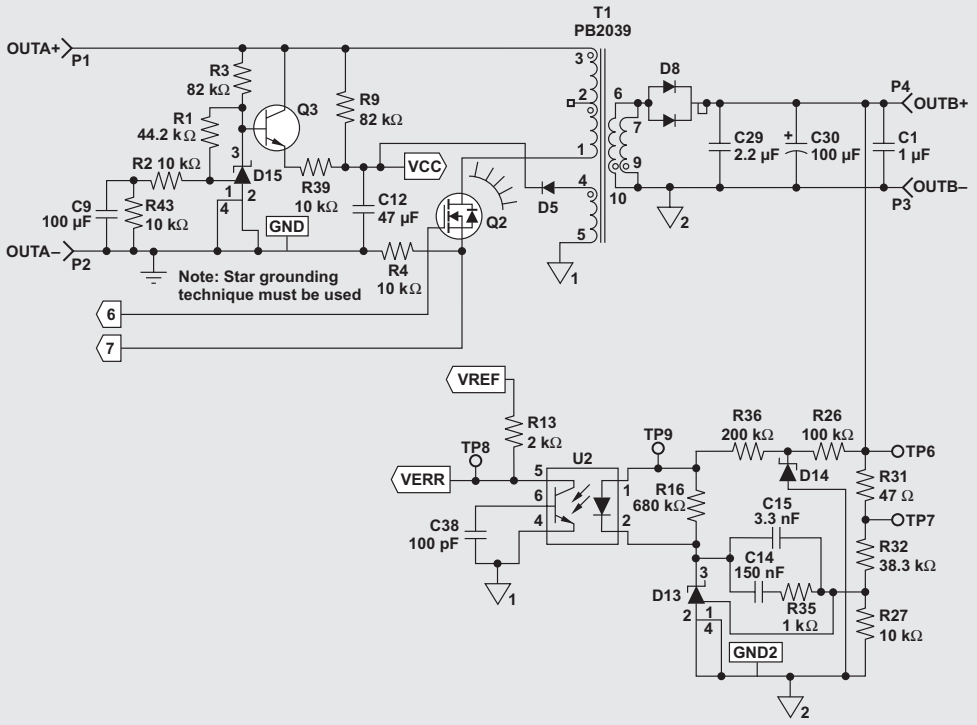
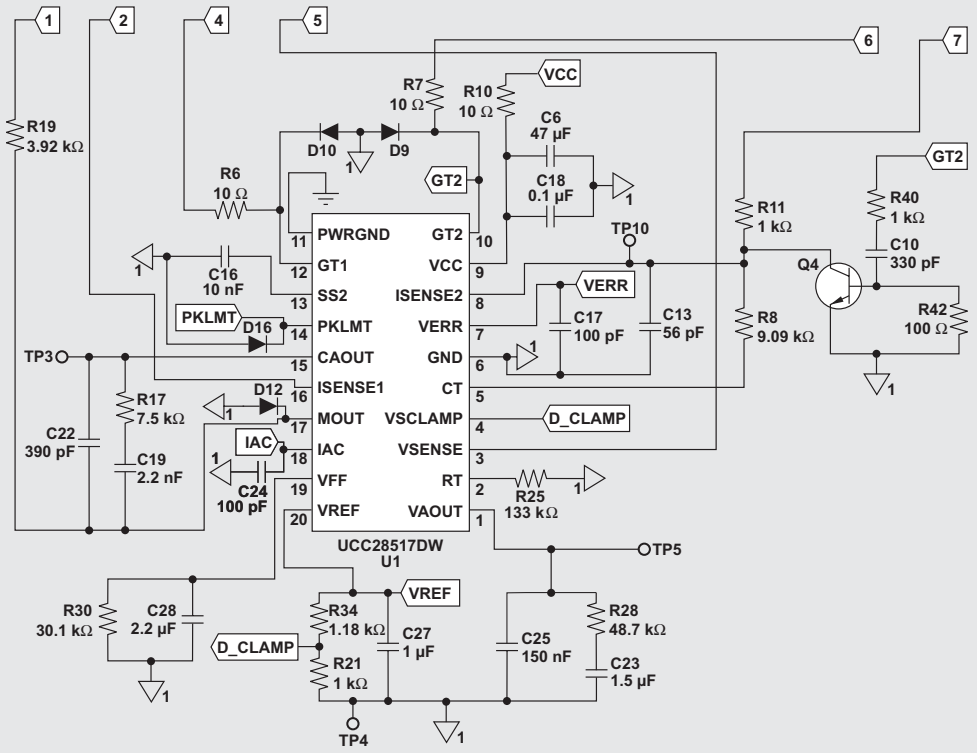


Figure 3. Controller schematic



operate during loss of line voltage. An auxiliary winding of 22 turns was added to power the UCC28517 control IC as well. For this design Pulse Engineering designed a 22-turn transformer (part number PB2039).

Power switch (Q2) and output diode (D8) selection

To select D8 and Q2 properly, a power budget is generally set for these devices to maintain the desired efficiency goal. The following equations were used to estimate power loss in the switching devices. To meet the power budget for this design, an IRFBF20S FET and a 20CJQ045 dual diode from International Rectifier were chosen.

$$I_{PK\_Q2} = \frac{2 \times \frac{P_{OUTB}}{V_{OUTB}}}{\eta 2 \times N}$$

$$I_{RMS\_FET\_Q2} = \frac{P_{OUTB}}{\eta 2 \times N} \times \sqrt{\frac{D_{max}}{3}}$$

$$P_{COND\_FET\_Q2} = R_{DS(on)} \times I^2_{RMS\_FET}$$

$$P_{GATE\_Q2} = Q_{GATE} \times V_{GATE} \times f_S$$

$$P_{COSS\_Q2} = \frac{1}{2} C_{OSS\_Q2} \times V^2_{OUTB} \times f_S$$

$$P_{FET\_TR\_Q2} = \frac{1}{2} V_{OUTB} \times I_{RMS\_Q2} \times (t_r + t_f) \times f_{SB}$$

$$P_{Q2} = P_{GATE\_Q2} + P_{COSS\_Q2} + P_{COND\_FET} + P_{FET\_TR\_Q2}$$

$$I_{PK\_D8} = \frac{2 \times P_{OUTB} \times (1 - D_{max})}{V_{OUTB}}$$

$$P_{DIODE\_CAP\_D8} = \frac{C_{DIODE}}{2} \times V^2_{OUTB} \times f_{SB}$$

$$P_{COND\_D8} = V_f \times I_{RMS\_D8}$$

$$I_{RMS\_D8} = I_{PK\_D8} \times \sqrt{\frac{1 - D_{max}}{3}}$$

$$P_{DIODE} = P_{COND\_D8} + P_{DIODE\_CAP\_D8}$$

Output capacitor

The output capacitor selection for the step-down converter was based on requirements for energy storage, output ripple voltage, RMS current, and peak current.

$$I_{PK\_C30} = 2 \times \frac{\frac{P_{OUTB}}{V_{OUTB}}}{1 - D_{max}}$$

$$ESR_{C30\_max} \le \frac{V_{ripple}}{I_{PK\_C30}}$$

$$C30 \ge \frac{0.5 \times I_{PK} \times (1 - D_{max})}{f_{SB} \times V_{OUTB}}$$

$$I_{RMS\_C30} = I_{PK\_C30} \times \sqrt{(1 - D_{max}) \times \left[\frac{4 - 3 \times (1 - D_{max})}{12}\right]}$$

R_{SENSE2}

The dc/dc power converter is designed for peak-current-mode control. R4 is the current sense resistor, which can be sized through the following two equations.

$$I_m = \frac{V_{OUTA} \times D_{max}}{L_m \times f_{SB}}$$

$$R4 = \frac{V_{dynamic}}{I_m + \frac{I_{PK\_C30}}{N}}$$

Soft start

The UCC28517 has soft-start circuitry to allow for a controlled ramp of the second stage's duty cycle during startup. The following equation was used to calculate the approximate capacitance needed to achieve a soft start of roughly 5 ms (Δt).

$$C16 = \frac{I_{SS} \times \Delta t}{5\ V}$$

Slope compensation

Designing a power converter that uses peak-current-mode control generally requires slope compensation to remove instabilities in the control loop and to make the design less susceptible to noise. Resistors R11 and R8 (Figure 3) sum in a portion of the oscillator signal to the current sense signal for slope compensation. Generally the added slope (V_{slope}) required is equal to half the down slope of the change in output current. By selecting R11 first, you can calculate the required value of R8 to generate the required slope compensation.

$$V_{slope} = \left(I_m + \frac{I_{PK\_C30}}{2N}\right) R4$$

$$R8 \le \frac{R11(V_{ct} - V_{slope})}{V_{slope}}$$

Leading-edge blanking circuit

The typical current sense signal for a converter using peak-current-mode control is shown in Figure 4. As shown, during time T1 there is a leading current spike. This is partly caused by the parasitic gate-to-source capacitance of the power stage switch Q4 and the voltage divider formed off the gate drive by R4 and R7. This leading-edge spike can cause the peak-current-mode signal to terminate the gate drive prematurely. To remove this instability, a leading-edge blanking circuit was constructed.

Electronic components Q4, R40, R42, and C10 form a leading-edge blanking circuit. This circuit is used to clamp leading-edge current spikes. The timing of the leading-edge blanking can be adjusted by modifying the size of timing capacitor C10:

$$C10 = \frac{t_{blank}}{2(R40 + R42)}$$

Figure 4. Typical current sense signal

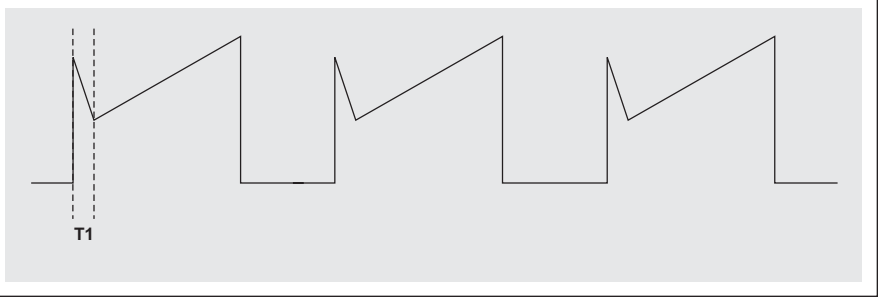
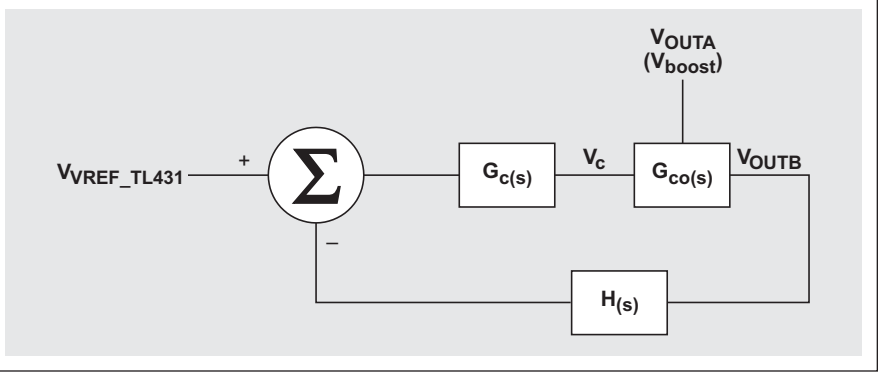


Figure 5. dc/dc converter control loop



Control loop for the dc/dc converter

Figure 5 shows the control block diagram for the control loop of the dc/dc converter. $G_{c(s)}$ is the compensation network's transfer function (TF), $G_{opto(s)}$ is the optoisolator gain TF, $G_{co(s)}$ is the control-to-output gain TF, and $H_{(s)}$ is the divider gain TF. To estimate the frequency response of each gain block, the following equations can be used. f_{opto_pole} is the frequency where the optoisolator gain is –3 dB from its dc operating point; and V_{VREF_TL431} is the internal reference voltage of the TL431 shunt regulator. R_{load} represents the typical load impedance for the design.

$$H_{(s)} = \frac{R27}{R27 + R32} = \frac{V_{VREF\_TL431}}{V_{OUTB}}$$

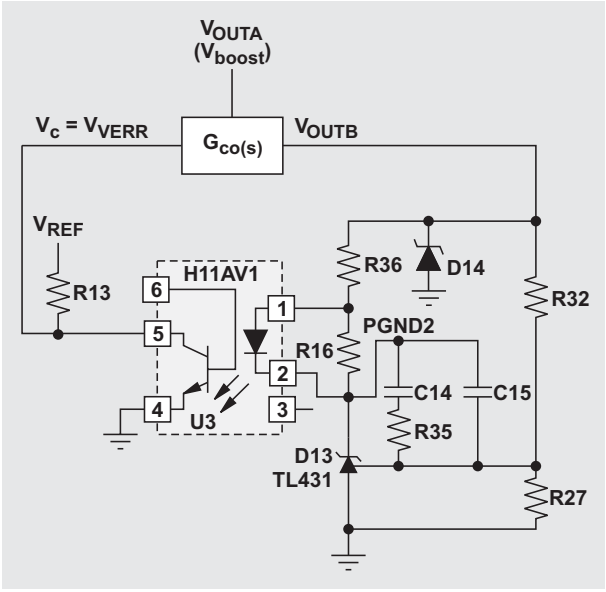
$$G_{opto(s)} = \frac{R13}{R36} \times \frac{1}{1 + \frac{s}{2\pi f_{opto\_pole}}}$$

$$G_{c(s)} = \frac{s \times R35 \times C14 + 1}{s \times C14 \times R31 \times (1 + s \times R35 \times C15)} \times \frac{R13}{R36} \times \frac{1}{1 + \frac{s}{2\pi f_{opto\_pole}}}$$

$$G_{co(s)} = \frac{V_{OUTB}}{V_c} = \frac{R_{load}}{R4} \times \frac{N_p}{N_s} \times \frac{1 + s \times C30 \times ESR}{1 + s \times C30 \times R_{load}}$$

Figure 6 shows the circuitry that was used for the voltage feedback loop. D13 is a TL431 shunt regulator that can function as an operational amplifier to provide feedback control when set up in this configuration.

Figure 6. Voltage feedback loop



Initially the resistor values for the divider gain, $H_{(s)}$, must be selected. The following equation can be used to size these resistors, where V_{OUTB} is the desired output voltage and V_{VREF_TL431} is the internal reference of the TL431.

$$R32 = \frac{R27(V_{OUTB} - V_{VREF\_TL431})}{V_{VREF\_TL431}}$$

It is important to bias the TL431 and the optoisolator correctly for proper operation. Resistors R16 and R13 provide the minimum bias currents for the TL431 and the optoisolator, respectively, and can be selected with the following equations. The optoisolator was configured to have a dc gain of roughly 20 dB, and the optoisolator had a crossover frequency of roughly 80 kHz. Figure 7 shows the small signal frequency response of the optoisolator.

$$R16 = \frac{V_f}{I_{TL431\_min}}$$

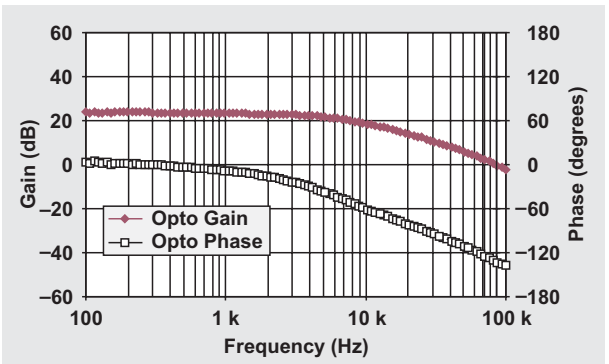
$$R13 = \frac{V_{REF} - V_{VERR(max)}}{I_{op\_min}}$$

Before attempting to compensate the control loop, $T_{s(f)}$, we must define some design goals for the closed-loop frequency response. Typically the loop is designed to cross over at a frequency below one-sixth of the switching frequency (see Reference 3). For this design example to have good transient response, the design goal was to have the loop gain crossover frequency (f_c) at roughly 1 kHz, which is less than one-sixth of the switching frequency (f_{SB}). The following equation describes the frequency response of the system loop gain, $T_{s(f)}$, in decibels.

$$T_{s(f)} = G_{c(s)_{dB}} + G_{co(s)_{dB}} + H_{(s)_{dB}}$$

The compensation network that is used ($G_{c(s)}$) has three poles and one zero. One pole occurs at the origin, and a second pole is caused by the limitations of the optoisolator. The third pole is set at one-half the switching frequency to attenuate the high frequency gain. The zero

Figure 7. Optoisolator frequency response



is set at the desired crossover frequency. The following equations can be used to select R35, C14, and C15 of $G_{c(s)}$ to obtain the desired design goals.

$$H_{(s)_{dB}} = 20\log(H_{(s)})$$

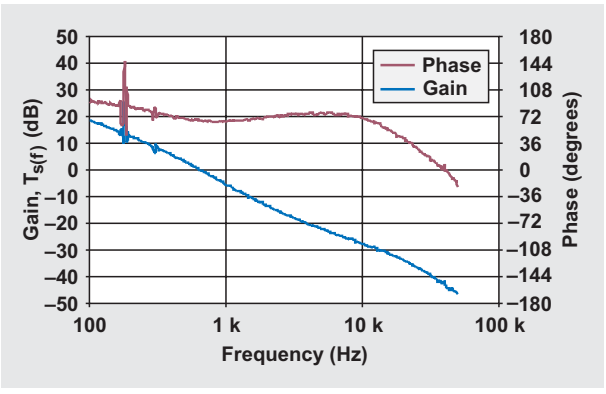
$$R35 = R32 \times 10^{\frac{-(G_{co(s)_{dB}} + G_{opto(s)_{dB}} + H_{(s)_{dB}})}{20}}$$

$$C14 = \frac{1}{2 \times \pi \times R35 \times f_c}$$

$$C15 = \frac{1}{2 \times \pi \times R35 \times \frac{f_S}{2}}$$

Figure 8 shows the measured loop gain frequency response, $T_{s(f)}$. The frequency response characteristics in Figure 8 show that f_c was roughly equal to 800 Hz with a phase margin of roughly 50°. It is important to note that the equations used to compensate the control loop by selecting C14, C15, and R35 are estimates and the values may have to be adjusted to get the appropriate compensation.

Figure 8. Frequency loop response, $T_{s(f)}$



Summary

In this design example we reviewed the design of a 100-W PFC ac/dc preregulator with an auxiliary 12-V, 8-W bias supply. The UCC2851x family of combination PWM controllers is perfect for offline applications that require PFC and auxiliary power supplies to meet different system requirements. The design performance of this two-stage power converter is shown in Figures 9–12.

References

For more information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/*litnumber* and replace *"litnumber"* with the **TI Lit. #** for the materials listed below.

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8. "UCC28517 Prototype Reference Design Module," Reference Design	sluu117

Related Web sites

analog.ti.com
www.ti.com/sc/device/TL431
www.ti.com/sc/device/UCC28517

Figure 9. Output A THD vs. output power

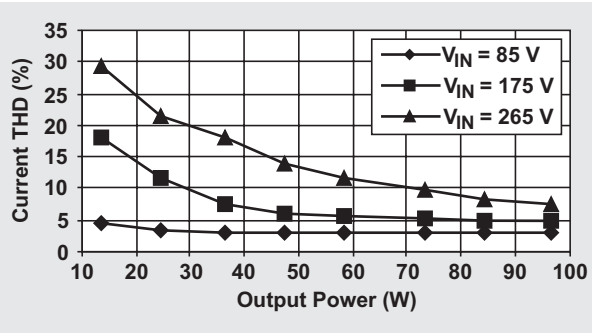


Figure 10. Output A efficiency vs. output power

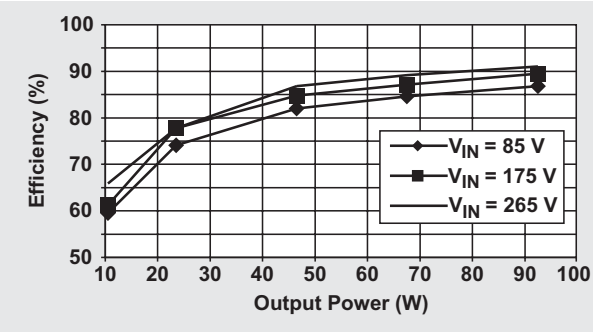


Figure 11. Output A PF vs. output power

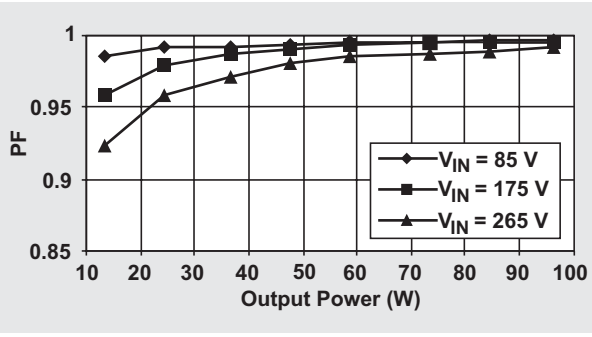
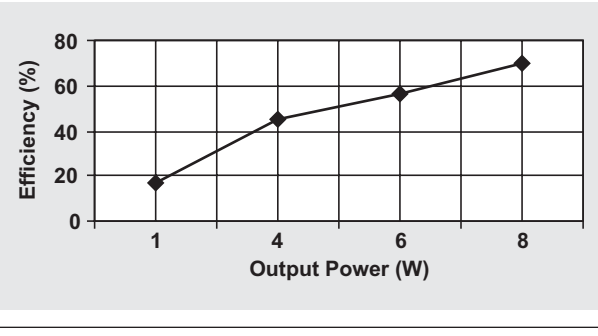


Figure 12. Output B efficiency vs. output power



Op amp attenuators

By Bruce Carter (Email: r-carter5@ti.com)
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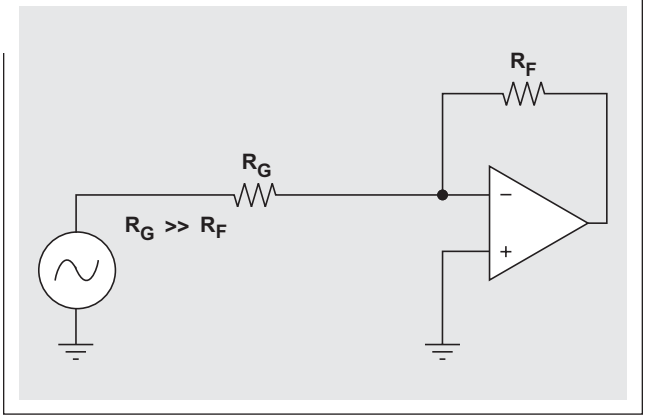
Introduction

Techniques to make op amp gain stages have been covered in literature for decades, and most designers are fairly competent in designing inverting and non-inverting gain stages. Those same designers, when faced with the need to attenuate a signal, may turn to the inverting op amp circuit configuration because it is capable of supporting "gains" < 1. All that is required is to make R_G greater than R_F (see Figure 1).

Figure 1. Incorrect method of attenuation



This attenuation technique is not advisable, because it makes the loop gain move toward the open-loop plot of the op amp while simultaneously decreasing the phase margin. This is the least stable configuration for the op amp. Combine this with small values of parasitic capacitance on the inverting input, and the op amp is almost guaranteed to oscillate.

The author recently presented a series of seminars on signal conditioning. Some attendees were attempting to produce a product in which an op amp stage had a gain < 1. One attendee in particular had a programmable op amp attenuator that was completely stable at a gain of 1, exhibited overshoot and/or ringing at a gain of 1/10, and oscillated uncontrollably at a gain of 1/100. The seminar material on stability was quite an eye-opener! This material is available in References 1 through 3.

Stable op amp attenuators

To make an op amp attenuator, a circuit must be constructed that keeps the closed-loop gain of the op amp ≥ 1. Making R_G large in comparison to R_F is not advisable. It is possible, however, to construct a circuit in which the op amp is "fooled" into thinking it is operating at or slightly above unity gain. There are two ways to do this. The first uses a rather complex inverting attenuator; the second uses a much simpler non-inverting attenuator. A discussion of these two methods follows.

Inverting attenuator

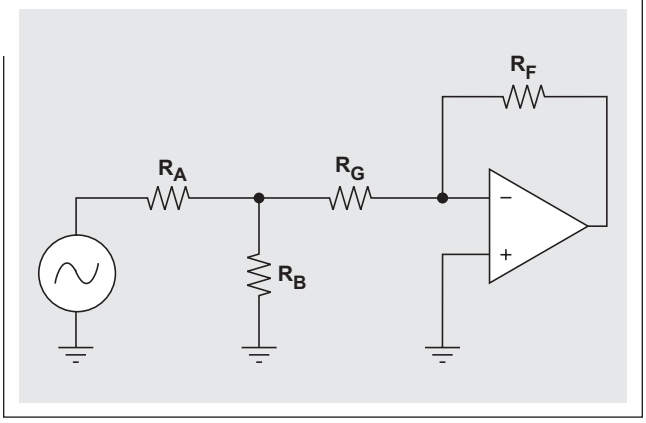
Figure 2 shows an inverting op amp attenuator where $R_F \geq R_G + R_A \parallel R_B$. Although it looks superficially simple, it is actually more complex. It makes a very nice attenuation circuit if a termination resistor is used, but in the gain calculations the designer needs to take into account the output impedance of the source as part of R_A.

In Figure 2, the op amp "sees" a gain ≥ 1 because the value of R_G plus the parallel combination of R_A and $R_B \leq R_F$. The input signal, however, is attenuated by a voltage divider comprised of R_A and $R_B \parallel R_G$. Overall "gain" of the single-ended stage is

$$\frac{V_{OUT}}{V_{IN}} = A_{CL} = \frac{R_B \| R_G}{R_A + R_B \| R_G} \times \frac{R_F}{R_G} = \frac{R_B R_F}{R_A R_B + R_A R_G + R_B R_G}.$$

It would probably be more useful to designers if the expression were solved for the proper values of resistors

Figure 2. Inverting op amp attenuator



to generate a desired attenuation. To do this more easily, some substitutions are made:

$$R_G = \frac{R_F}{2} \text{ and } R_A = \frac{R_F}{2}.$$

What this does, in effect, is twofold:

1. It guarantees that the op amp will never see less than unity gain. If $R_B \rightarrow \infty$, then $R_A + R_G = R_F$, and A_{CL} becomes

$$\frac{R_F}{R_A + R_G} = 1.$$

2. It also means that as R_B is included in the circuit and goes down in value, the op amp will see a gain > 1—which seems a bit wasteful, but there is no technical reason why it will not work. The op amp will never see a gain of 2 or above, because the limiting case with $R_B = 0$ would be a gain of 2. Of course, making $R_B = 0$ would not make a practical circuit.

Very often, designers will want to know the value of R_B for a given attenuation. If the substitutions mentioned earlier are made, R_B can be solved for as follows:

$$R_B = \frac{A_{CL}}{1 - A_{CL}} \times \frac{R_F}{4},\ R_A = \frac{R_F}{2},\ \text{and } R_G = \frac{R_F}{2}.$$

This relationship will yield the proper values of R_B when the values of R_F and A_{CL} are known. Data sheets for high-speed op amps frequently specify the values of R_F.

The Texas Instruments (TI) Web site includes a utility to calculate the best resistor values automatically for an inverting attenuator. (Go to Reference 4 and click on "Single Output Amplifier Design Utilities," then on "Inverting Attenuator Calculator.") Two options are included—one that allows the designer to select R_F based on the device data sheet, and another that calculates the closest possible match of resistors for a desired attenuation.

Non-inverting attenuator

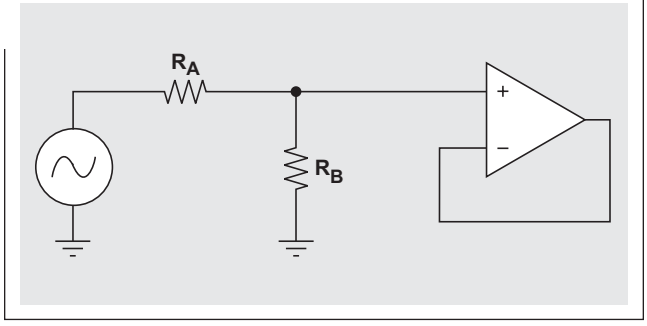
A much simpler attenuator, shown in Figure 3, employs a unity-gain, non-inverting buffer. Because the input impedance of the non-inverting op amp is high, it can be discounted in the gain calculations. The "gain" of this stage is the familiar voltage divider expression

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_B}{R_A + R_B}.$$

The designer can also use this attenuation circuit when R_B is an input termination resistor, if the output impedance of the source is taken into account as part of R_A.

TI also has a utility to generate the best possible match of resistors for a non-inverting op amp attenuator. (Go to Reference 4 and click on "Single Output Amplifier Design Utilities," then on "Voltage Divider Utility.")

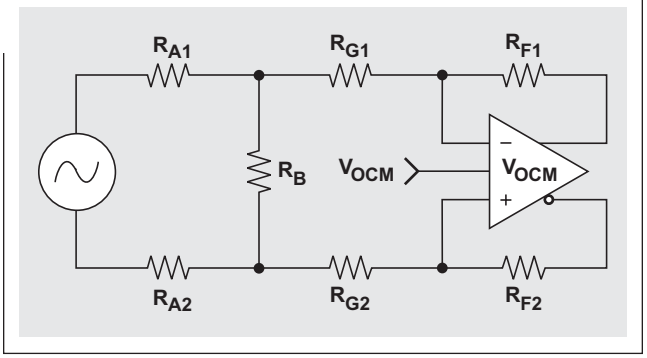
Figure 3. Non-inverting op amp attenuator



Fully differential op amp attenuators

Attenuators constructed from fully differential op amps are somewhat analogous to terminated fully differential op amp circuits, except that the resistor that accomplishes the attenuation does not necessarily have to be a termination resistor or a standard termination value.

Figure 4. Fully differential attenuator operation



Consider the circuit in Figure 4. In this configuration, a voltage divider is formed by the action of R_{A1}, R_{A2}, and R_B. Remember that each signal is the return path for the other polarity of signal.

The gain of the fully differential stage is

$$\frac{V_{OUT}}{V_{IN}} = A_{CL} = \frac{R_B \| 2R_G}{2R_A + R_B \| 2R_G} \times \frac{R_F}{R_G} = \frac{R_B R_F}{R_B R_G + R_A R_B + 2R_A R_G}.$$

To solve for the proper values of resistors to generate a desired attenuation, the same substitutions can be made that were made for the equation given earlier for the gain of the single-ended stage:

$$R_G = \frac{R_F}{2} \text{ and } R_A = \frac{R_F}{2}.$$

These substitutions have the same twofold effect explained before: The op amp will never see less than unity gain; and, as R_B is included in the circuit and goes down in value, the op amp will see a gain > 1. If these

substitutions are made, the value of R_B for a given attenuation can be solved for as follows:

$$R_B = \frac{A_{CL}}{1 - A_{CL}} \times \frac{R_F}{2},\ R_A = \frac{R_F}{2},\ \text{and}\ R_G = \frac{R_F}{2}.$$

As before, this relationship will yield the proper values of R_B when the values of R_F and A_{CL} are known. Data sheets for fully differential op amps frequently specify the values of R_F.

Fully differential attenuators can be designed by using the same utility mentioned before. (Go to Reference 4 and click on "Single Output Amplifier Design Utilities" or "Fully Differential Amplifier Design Utilities," then on "Inverting Attenuator Calculator.")

References

For more information related to this article, you can download an Acrobat Reader file at www-s.ti.com/sc/techlit/*litnumber* and replace *"litnumber"* with the **TI Lit. #** for the materials listed below.

Document Title	**TI Lit. #**
1. "Single Supply Op Amp Design Techniques," Application Note	sloa076
2. "Feedback and Stability Theory," Application Note	sloa077
3. "Development of the Non Ideal Op Amp Equations," Application Note	sloa078
4. "Engineering Design Utilities," Texas Instruments, www.ti.com/amplifier_utilities	—

Related Web sites

analog.ti.com
www.ti.com/amplifier_utilities

Calculating noise figure in op amps

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Introduction

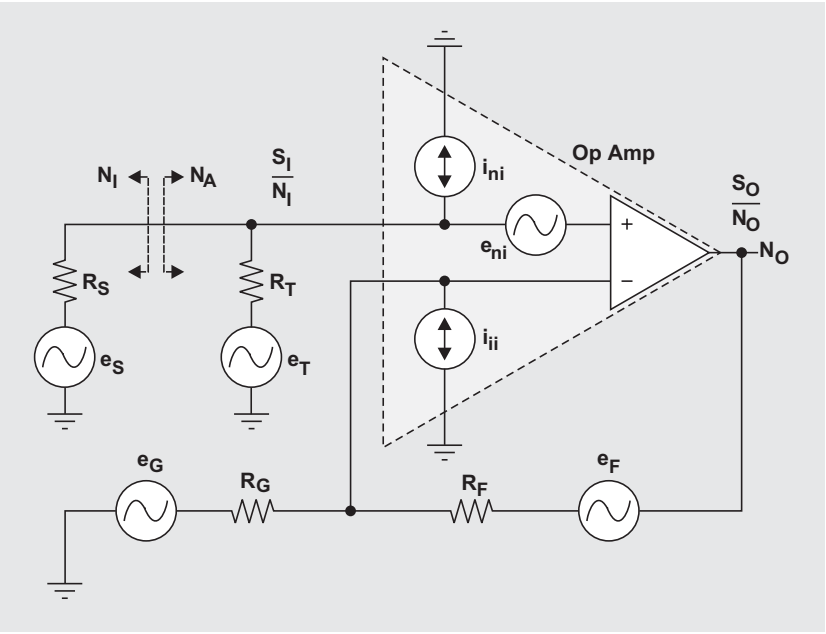
Noise figure is commonly used in communications systems because it provides a simple method to determine the impact of system noise on sensitivity.

Today, the performance of wide-band op amps is making them viable alternatives to more traditional open-loop amplifiers like monolithic microwave integrated circuits (MMICs) and discrete transistors in communications design.

Recognizing the need to specify wide-band op amps in RF engineering terminology, some manufacturers do provide noise figure, but they seem to be the exception rather than the rule.

Op amp manufacturers typically specify noise performance by giving the input-referred voltage and current noise. The noise figure depends on these parameters, the circuit topology, and the value of external components. If you have all this information, noise figure can be calculated.

Figure 1. Non-inverting noise analysis diagram



Review of noise figure

Noise figure (NF) is the decibel equivalent of noise factor (F): NF (dB) = 10log(F).

Noise factor of a device is the power ratio of the signal-to-noise ratio (SNR) at the input (SNR_I) divided by the SNR at the output (SNR_O):

$$F = \frac{SNR_I}{SNR_O}. \quad (1)$$

The output signal (S_O) is equal to the input signal (S_I) times the gain: $S_O = S_I \times G$. The output noise is equal to the noise delivered to the input (N_I) from the source plus the input noise of the device (N_A) times the gain: $N_O = (N_I + N_A) \times G$. Substituting into Equation 1 and simplifying, we get

$$F = \frac{SNR_I}{SNR_O} = \left[\frac{\frac{S_I}{N_I}}{\frac{G \times S_I}{G(N_I + N_A)}}\right] = 1 + \frac{N_A}{N_I}. \quad (2)$$

Assuming that the input is terminated in the same impedance as the source, $N_I = kT = -174$ dBm/Hz, where k is Boltzman's constant and T = 300 Kelvin). Once we find the input noise spectral density of the device, it is a simple matter to plug it into Equation 2 and calculate F.

NF in op amps

Op amps specify input-referred voltage and current noise. Using these two parameters, adding the noise of the external resistors, and calculating the total input-referred noise based on the circuit topology, we can calculate the input spectral density and use it in Equation 2.

In this discussion, the terms "op amp" and "amplifier" mean different things. "Op amp" refers to only the active device itself, whereas "amplifier" includes the op amp and associated passive resistors that make it work as a usable amplifier stage. In other words, the amplifier is everything shown in Figures 1–3 except R_S, and the op amp is only the components within the dashed triangles. In this way, the plane marked N_A and N_I is the input to the amplifier. This is the point to which the noise sources must be referred so that Equation 2 can be used.

The noise from the source and the input noise of the amplifier are referred to the same point. Because the impedance is the same, expressing the ratio between N_A and N_I as a voltage ratio squared is equivalent to the power ratio. An op amp is a voltage-driven device, so using voltage-squared terms makes the calculations easier. In the following discussion, voltage-squared terms are used for N_A and N_I.

Op amps use negative feedback to control the gain of the amplifier. One result is that the voltage across the input terminals is driven to zero. This is often referred to as a "virtual short." It is used in the following analysis* and referred to as "amplifier action," since it is a by-product of the op amp doing its job as an amplifier.

Superposition is used throughout the analysis, wherein all sources except the one under consideration are defeated—voltage sources are shorted and current sources are opened.

Non-inverting amplifier

Of the three basic op amp circuits, it is easiest to find the input-referred noise for the non-inverting op amp amplifier, so it will be discussed first. Figure 1 shows a noise analysis diagram for a non-inverting op amp amplifier with the noise sources identified.

The source resistance R_S generates a noise voltage equal to $\sqrt{4kTR_S}$. The noise voltage delivered to the amplifier input from the source is divided by the resistors R_S and R_T. Therefore,

$$N_I = 4kTR_S\left(\frac{R_T}{R_S + R_T}\right)^2.$$

R_T is typically used to terminate the input so that $R_T = R_S$, in which case $N_I = kTR_S$.

The amplifier's voltage noise is a combination of e_{ni}, i_{ni}, and i_{ii} with associated impedances e_T, e_G, and e_F. These are all referred

Figure 2. Inverting noise analysis diagram

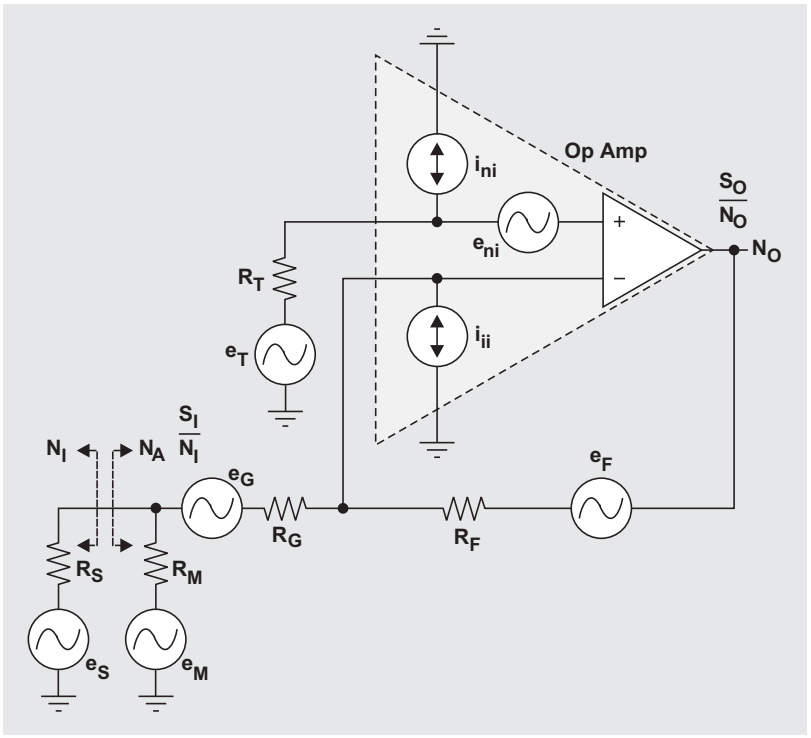
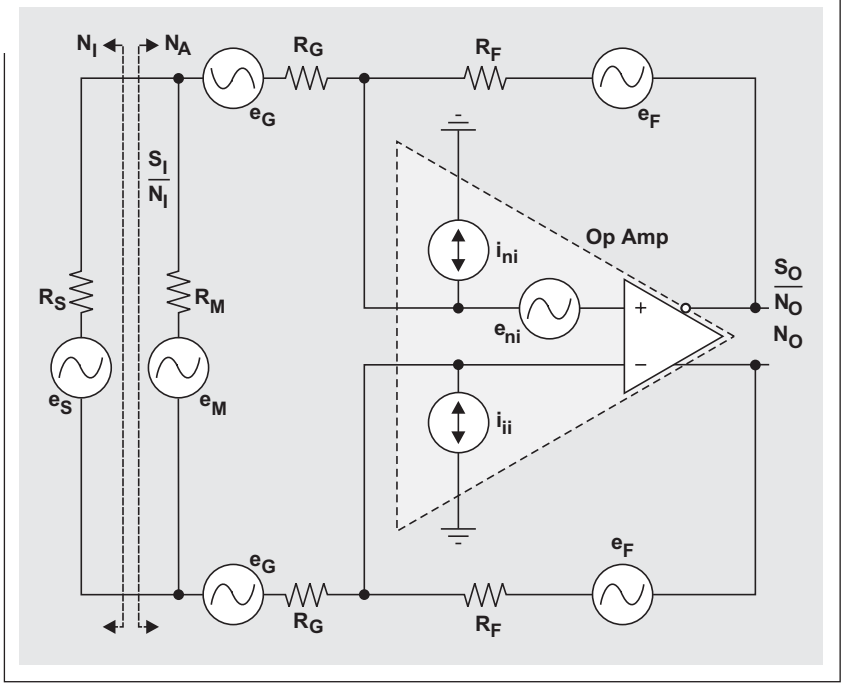


Figure 3. Fully differential noise analysis diagram



*The virtual-short concept simplifies the analysis. Much more work is required to obtain the same results by other means such as nodal analysis.

to the input by their respective scaling factors and summed to find N_A; i.e.,

$$N_A = c_1 e_{ni}^2 + c_2 i_{ni}^2 + c_3 i_{ii}^2 + c_4 e_T^2 + c_5 e_G^2 + c_6 e_F^2, \quad \textbf{(3)}$$

where c_1 through c_6 are the scaling factors.

The op amp's input voltage noise is e_{ni}. It appears directly at the amplifier's input and its scaling factor is 1 or unity, so that $c_1 e_{ni}^2 = e_{ni}^2$.

The op amp's non-inverting input current noise is i_{ni}. It develops a voltage through the parallel combination of R_S and R_T, which appears directly at the amplifier's input, so that

$$c_2 i_{ni}^2 = i_{ni}^2 \left(\frac{R_S R_T}{R_S + R_T} \right)^2.$$

The op amp's inverting input current noise is i_{ii}. It develops a voltage through the parallel combination of R_F and R_G at the op amp's inverting input. By amplifier action, this voltage appears at the amplifier's input, so that

$$c_3 i_{ii}^2 = i_{ii}^2 \left(\frac{R_F R_G}{R_F + R_G} \right)^2.$$

The noise voltage term e_T associated with R_T is equal to $\sqrt{4kTR_T}$. It is divided by the resistors R_S and R_T, so that

$$c_4 e_T^2 = 4kTR_T \left(\frac{R_S}{R_S + R_T} \right)^2.$$

If $R_T = R_S$, then $c_4 e_T^2 = kTR_T$.

The noise voltage term e_G associated with R_G is equal to $\sqrt{4kTR_G}$. This noise is divided by the resistors R_F and R_G and applied to the op amp's inverting input. Again by amplifier action, noise from R_G appears at the amplifier's input, so that

$$c_5 e_G^2 = 4kTR_G \left(\frac{R_F}{R_F + R_G} \right)^2.$$

The noise voltage term e_F associated with R_F is equal to $\sqrt{4kTR_F}$ and appears at the amplifier's output. Dividing by the signal gain gives us

$$c_6 e_F^2 = 4kTR_F \left(\frac{R_G}{R_F + R_G} \right)^2.$$

With all the terms in Equation 3 quantified, we can take the sum to find N_A and use N_A along with N_I in Equation 2 to find F.

Inverting amplifier

Finding the input-referred noise of an inverting op amp amplifier is more cumbersome than finding that of a non-inverting op amp amplifier. The main problem is that the signal gain of the amplifier and the noise gain are different.

Figure 2 shows a noise analysis diagram for an inverting op amp amplifier with the noise sources identified.

To find the input-referred noise, it is easiest in some cases to find the output noise and then divide by the signal gain of the amplifier.

The noise voltage delivered to the input from the source is divided by the resistors R_S and R_M in parallel with R_G. Therefore,

$$N_I = 4kTR_S \left[\frac{R_M R_S}{R_S(R_M + R_G) + (R_M R_G)} \right]^2.$$

R_M is typically selected so that $R_M \parallel R_G = R_S$, in which case $N_I = kTR_S$.

The amplifier's input-referred voltage noise is a combination of e_{ni}, i_{ni}, and i_{ii} with associated impedances e_T, e_G, e_F, and e_M. These are all referred to the input by their respective scaling factors and summed to find N_A; i.e.,

$$N_A = c_1 e_{ni}^2 + c_2 i_{ni}^2 + c_3 i_{ii}^2 + c_4 e_T^2 + c_5 e_G^2 + c_6 e_F^2 + c_7 e_M^2, \quad \textbf{(4)}$$

where c_1 through c_7 are the scaling factors.

The op amp's input voltage noise, e_{ni}, at the op amp's non-inverting input appears at the amplifier output as a function of the amplifier noise gain,

$$1 + \frac{R_F}{R_G + \dfrac{R_S R_M}{R_S + R_M}},$$

and is then referred back to the amplifier input as a function of the signal gain, R_F/R_G. Thus,

$$c_1 e_{ni}^2 = e_{ni}^2 \left(\frac{R_G}{R_F} + \frac{R_G}{R_G + \dfrac{R_S R_M}{R_S + R_M}} \right)^{**}.$$

The op amp's non-inverting input current noise is i_{ni}. It develops a voltage through R_T that appears directly at the amplifier's input, so that

$$c_2 i_{ni}^2 = i_{ni}^2 \left(\frac{R_T R_G}{R_F} + \frac{R_T R_G}{R_G + \dfrac{R_S R_M}{R_S + R_M}} \right).$$

It is hard to see how to calculate the op amp's inverting input current noise, i_{ii}. Basically, due to amplifier action, the inverting node is at ground so that no current is drawn through the input resistor R_G. The noise current flows through R_F, producing a voltage at the output equal to $i_{ii}R_F$. Referring to the amplifier's input results in $c_3 i_{ii}^2 = i_{ii}^2 (R_G)^2$.

The noise voltage term e_T associated with R_T is equal to $\sqrt{4kTR_T}$. Just like e_{ni}, it appears at the output as a function

**The gain is actually –RF/RG; but since it is squared, the minus sign is ignored in this analysis.

of the amplifier noise gain and is then referred back to the amplifier input as a function of the signal gain, so that

$$c_4 e_T^2 = kTR_T \left(\frac{R_G}{R_F} + \frac{R_G}{R_G + \frac{R_S R_M}{R_S + R_M}} \right)^2.$$

The noise voltage term e_G associated with R_G is equal to $\sqrt{4kTR_G}$. It is divided by the resistors R_G and R_S in parallel with R_M en route to the amplifier's input, so that

$$c_5 e_G^2 = 4kTR_G \left(\frac{R_G}{R_G + \frac{R_S R_M}{R_S + R_M}} \right)^2.$$

The noise voltage term e_F associated with R_F is equal to $\sqrt{4kTR_F}$ and appears directly at the amplifier's output. Dividing by the signal gain gives us

$$c_6 e_F^2 = 4kTR_F \left(\frac{R_G}{R_F} \right)^2.$$

The noise source e_M associated with the input termination matching resistor R_M is equal to $\sqrt{4kTR_M}$. It is divided by the resistors R_M and R_S in parallel with R_G, so that

$$c_7 e_M^2 = 4kTR_M \left[\frac{R_S R_G}{R_M (R_S + R_G) + R_S R_G} \right]^2.$$

With all the terms in Equation 4 quantified, we can take the sum to find N_A and use N_A along with N_I in Equation 2 to find F.

Fully differential amplifier

Fully differential op amp amplifiers are very similar to inverting op amp amplifiers, and the analysis follows very closely. Figure 3 shows the noise analysis diagram.

The source resistance generates thermal noise equal to $\sqrt{4kTR_S}$. The noise voltage delivered to the input from the source is divided by the resistors R_S and R_M in parallel with $2R_G$. Therefore,

$$N_I = 4kTR_S \left(\frac{\frac{2R_M R_G}{R_M + 2R_G}}{R_S + \frac{2R_M R_G}{R_M + 2R_G}} \right)^2.$$

R_M is typically selected so that $R_M \parallel 2R_G = R_S$, in which case $N_I = kTR_S$.

The amplifier's input-referred voltage noise is a combination of e_{ni}, i_{ni}, and i_{ii} with associated impedances e_G, e_F, and e_M. These are all referred to the input by their respective scaling factors and summed to find N_A; i.e.,

$$N_A = c_1 e_{ni}^2 + c_2 i_{ni}^2 + c_3 i_{ii}^2 + c_4 e_G^2 + c_5 e_F^2 + c_6 e_M^2, \quad \textbf{(5)}$$

where c_1 through c_6 are the scaling factors.

In this analysis it is assumed that the two input resistors R_G are equal and that the two feedback resistors R_F are equal.

The op amp's input voltage noise, e_{ni}, at the op amp's input appears at the amplifier output as a function of the amplifier noise gain,

$$1 + \frac{R_F}{R_G + \frac{R_S R_M}{2(R_S + R_M)}},$$

and is then referred back to the amplifier input as a function of the signal gain, R_F/R_G. Thus,

$$c_1 e_{ni}^2 = e_{ni}^2 \left[\frac{R_G}{R_F} + \frac{R_G}{R_G + \frac{R_S R_M}{2(R_S + R_M)}} \right]^2.$$

Since the input resistors are equal and the feedback resistors are equal, the op amp's non-inverting input current noise, i_{ni}, and inverting input current noise, i_{ii}, have the same scaling factors. Due to amplifier action, the input nodes of the op amp are ac grounds so that no current is drawn through the input resistors R_G. All the noise current flows through R_F, producing a voltage at the output equal to $i_{ni}R_F$ or $i_{ii}R_F$. Referring to the amplifier's input results in $c_2 i_{ni}^2 = i_{ni}^2 (R_G)^2$ and $c_3 i_{ii}^2 = i_{ii}^2 (R_G)^2$.

The noise voltage term e_G associated with each R_G is equal to $\sqrt{4kTR_G}$. It is divided by the resistors R_G and one-half R_S in parallel with R_M, so that

$$c_4 e_G^2 = 2 \times 4kTR_G \left[\frac{R_G}{R_G + \frac{R_S R_M}{2(R_S + R_M)}} \right]^2.$$

The noise voltage term e_F associated with each R_F is equal to $\sqrt{4kTR_F}$ and appears directly at the amplifier's output. Dividing by the signal gain gives us

$$c_5 e_F^2 = 4kTR_F \left(\frac{R_G}{R_F} \right)^2.$$

The noise source e_M associated with the input termination matching resistor R_M is equal to $\sqrt{4kTR_M}$. It is divided by the resistors R_M and R_S in parallel with $2R_G$, so that

$$c_6 e_M^2 = 4kTR_M \left(\frac{\frac{2R_S R_G}{R_S + 2R_G}}{R_M + \frac{2R_S R_G}{R_S + 2R_G}} \right)^2.$$

As before, with all the terms in Equation 5 quantified, N_A can be calculated and used with N_I in Equation 2 to find the noise factor.

Table 1. Comparison of calculated vs. measured noise figure

OP AMP	CONFIGURATION	e_{ni} (nV)	i_{ni} (pA)	i_{ii} (pA)	R_F (Ω)	R_G (Ω)	R_T (Ω)	R_M (Ω)	CALCULATED NF (dB)	MEASURED NF (dB)
THS3202	Non-inverting	1.65	13.5	20	255	49.9	49.9	—	11.6	11.5
THS3202	Inverting	1.65	13.5	20	255	49.9	—	—	13.6	13.0
THS4501	Fully differential	7	1.7	1.7	392	392	—	56.2	30.1	30.6

Conclusion

The input-referred voltage noise and current noise, along with the circuit configuration and component values, can be used to calculate noise figure. This is a tedious task at best. Setting up a spreadsheet for each topology where component values and op amp specs can be entered is recommended. In this way, various scenarios can be quickly tested. Verification by testing the circuit with a noise figure analyzer is always suggested.

As an example of how well the theory outlined in this article matches test results, the noise figure of three op amp amplifiers configured as previously detailed were measured with an Agilent N8973A noise figure analyzer. Table 1 shows that the results are good, with the input current and voltage noise specifications given as typical values.

Related Web sites

analog.ti.com
www.ti.com/sc/device/THS3202
www.ti.com/sc/device/THS4501

Appendix—Summary of noise terms in op amp amplifiers

Signal input noise (N_I) terms

AMPLIFIER CONFIGURATION	NOISE SOURCE	NOISE CONTRIBUTION
Non-inverting	Source thermal noise	$4kTR_S\left(\frac{R_T}{R_S+R_T}\right)^2$
Inverting	Source thermal noise	$N_I = 4kTR_S\left[\frac{R_M R_S}{R_S(R_M+R_G)+(R_M R_G)}\right]^2$
Fully differential	Source thermal noise	$4kTR_S\left(\frac{\frac{2R_M R_G}{R_M+2R_G}}{R_S+\frac{2R_M R_G}{R_M+2R_G}}\right)^2$

Appendix—Summary of noise terms in op amp amplifiers (Continued)

Device input noise (N_A) terms

AMPLIFIER CONFIGURATION	NOISE SOURCE	NOISE CONTRIBUTION
Non-inverting	Op amp input-referred voltage noise	e_{ni}^2
	Op amp non-inverting input-referred current noise	$i_{ni}^2\left(\frac{R_S R_T}{R_S + R_T}\right)^2$
	Op amp inverting input-referred current noise	$i_{ii}^2\left(\frac{R_F R_G}{R_F + R_G}\right)^2$
	Termination resistor thermal noise voltage	$4kTR_T\left(\frac{R_S}{R_S + R_T}\right)^2$
	Gain resistor thermal noise voltage	$4kTR_G\left(\frac{R_F}{R_F + R_G}\right)^2$
	Feedback resistor thermal noise voltage	$4kTR_F\left(\frac{R_G}{R_F + R_G}\right)^2$
Inverting	Op amp input-referred voltage noise	$e_{ni}^2\left(\frac{R_G}{R_F} + \frac{R_G}{R_G + \frac{R_S R_M}{R_S + R_M}}\right)^2$
	Op amp non-inverting input-referred current noise	$i_{ni}^2\left(\frac{R_T R_G}{R_F} + \frac{R_T R_G}{R_G + \frac{R_S R_M}{R_S + R_M}}\right)^2$
	Op amp inverting input-referred current noise	$i_{ii}^2(R_G)^2$
	Non-inverting bias matching resistor thermal noise voltage	$4kTR_T\left(\frac{R_G}{R_F} + \frac{R_G}{R_G + \frac{R_S R_M}{R_S + R_M}}\right)^2$
	Gain resistor thermal noise voltage	$4kTR_G\left(\frac{R_G}{R_G + \frac{R_S R_M}{R_S + R_M}}\right)^2$
	Feedback resistor thermal noise voltage	$4kTR_F\left(\frac{R_G}{R_F}\right)^2$
	Inverting termination matching resistor thermal noise voltage	$4kTR_M\left[\frac{R_S R_G}{R_M(R_S + R_G) + R_S R_G}\right]^2$

Appendix—Summary of noise terms in op amp amplifiers (Continued)

Device input noise (N_A) terms (Continued)

AMPLIFIER CONFIGURATION	NOISE SOURCE	NOISE CONTRIBUTION
Fully differential	Op amp input-referred voltage noise	$e_{ni}^2\left[\frac{R_G}{R_F}+\frac{R_G}{R_G+\frac{R_S R_M}{2(R_S+R_M)}}\right]^2$
	Op amp non-inverting input-referred current noise	$i_{ni}^2(R_G)^2$
	Op amp inverting input-referred current noise	$i_{ii}^2(R_G)^2$
	Gain resistor thermal noise voltage	$2\times 4kTR_G\left[\frac{R_G}{R_G+\frac{R_S R_M}{2(R_S+R_M)}}\right]^2$
	Feedback resistor thermal noise voltage	$2\times 4kTR_F\left(\frac{R_G}{R_F}\right)^2$
	Termination matching resistor thermal noise voltage	$4kTR_M\left(\frac{\frac{2R_S R_G}{R_S+2R_G}}{R_M+\frac{2R_S R_G}{R_S+2R_G}}\right)^2$

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