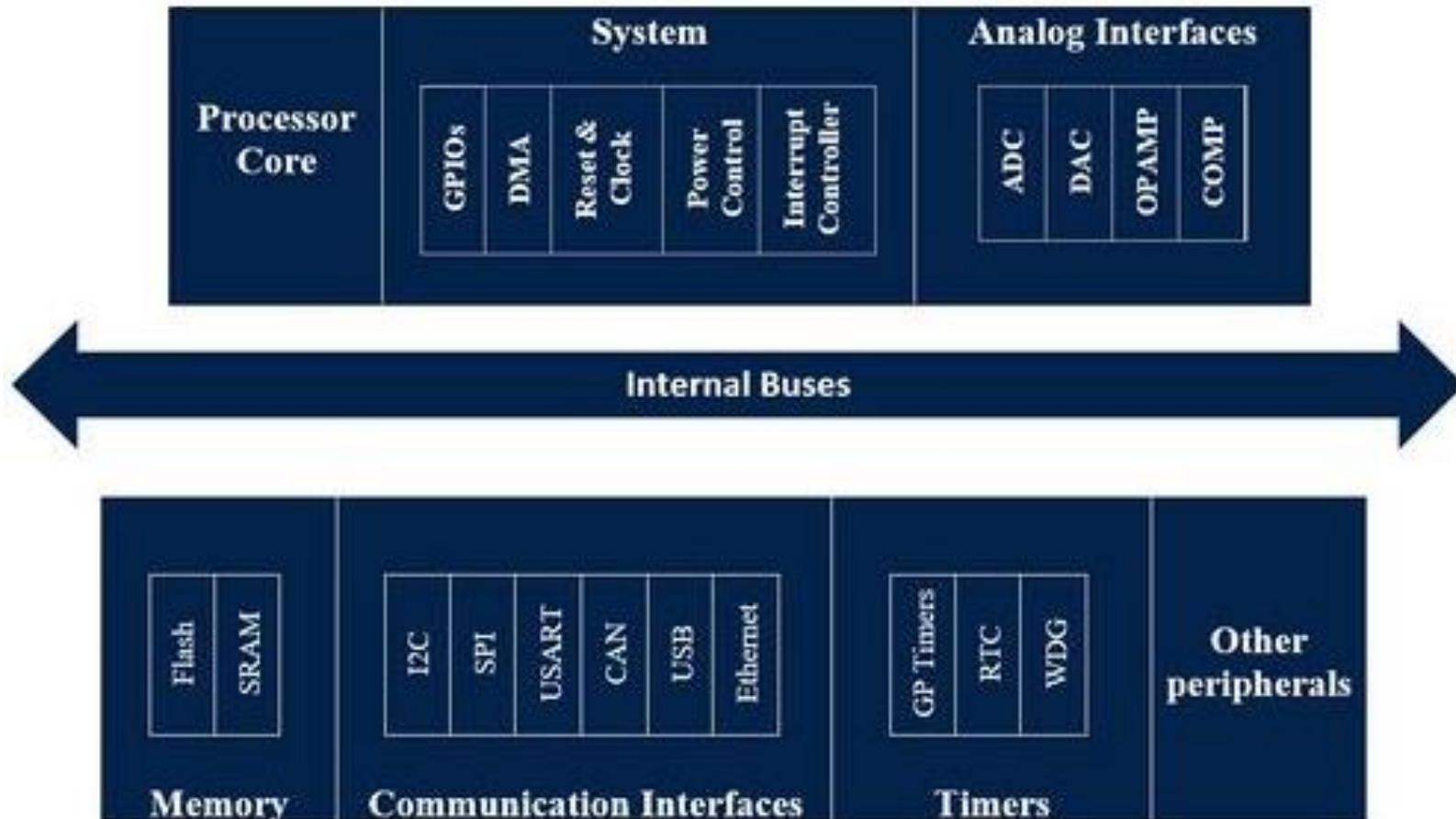




Cortex-M MCUs

General MCU block diagram

- Typical microcontroller: processor, memory and Input/Output (I/O) peripherals
- Its components may be include Digital I/O, Analog I/O, Timers, Communication interfaces...



Cortex-M family

arm CORTEX®-M0



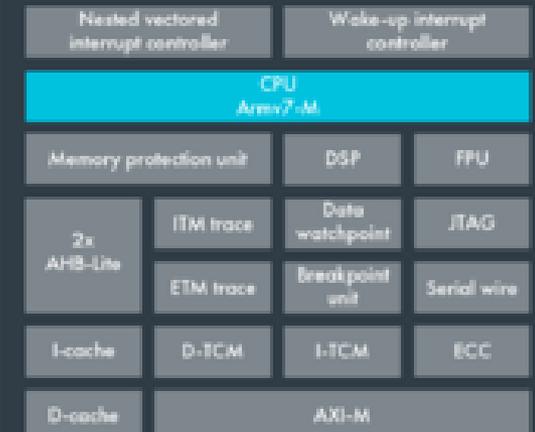
Cortex-M0 [↗](#)

arm CORTEX®-M4



Cortex-M4 [↗](#)

arm CORTEX®-M7



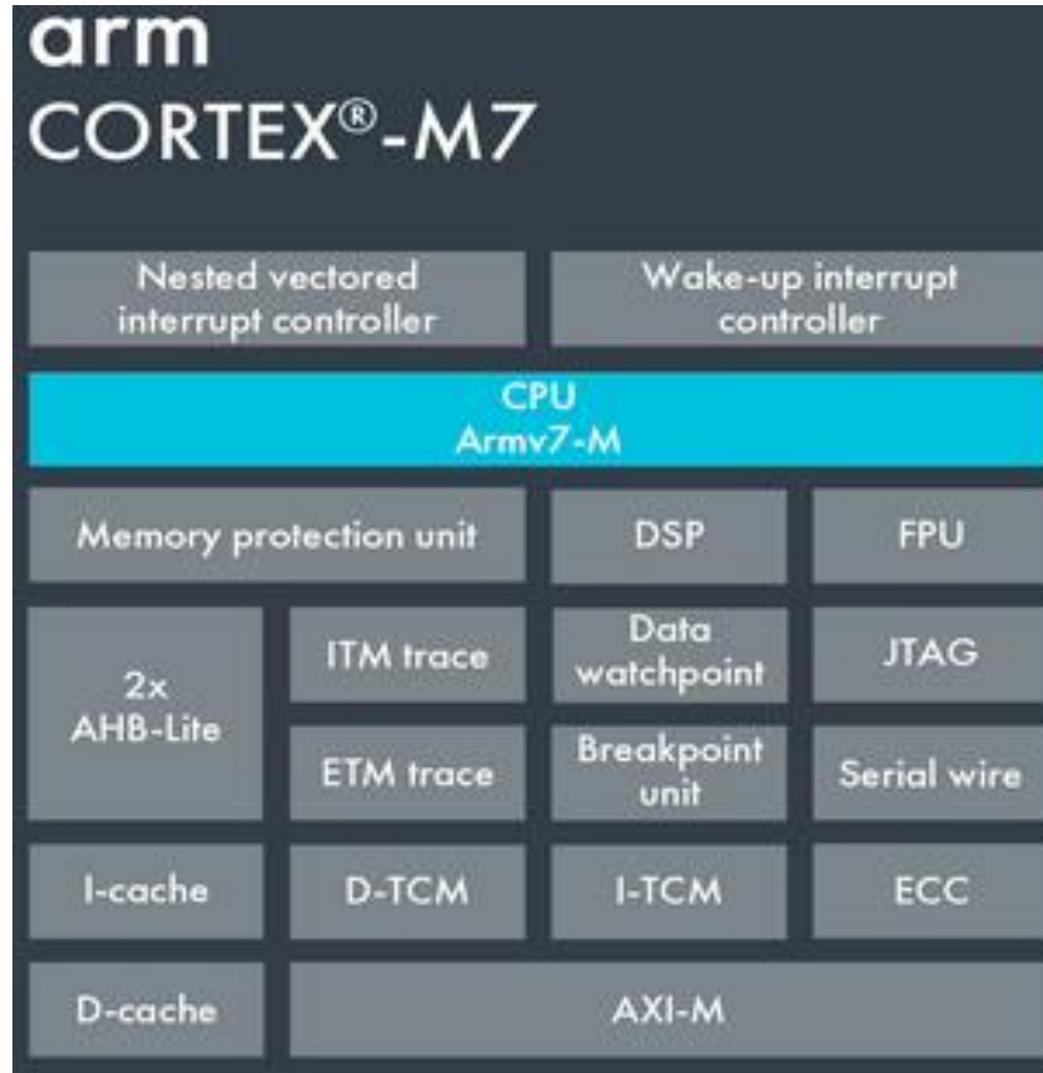
Cortex-M7 [↗](#)

Cortex-M family

Feature	Cortex-M0	Cortex-M0+	Cortex-M3	Cortex-M4	Cortex-M33	Cortex-M7
Instruction set architecture	Armv6-M	Armv6-M	Armv7-M	Armv7-M	Armv8-M Mainline	Armv7-M
	Thumb, Thumb-2					
Pipeline stages	3	2	3	3	3	6
Memory Protection Unit	No	Yes	Yes	Yes	Yes	Yes
Maximum MPU regions	0	8	8	8	16	16
Trace (ETM or MTB)	No	MTB	ETMv3	ETMv3	MTB and/or ETMv4	ETMv4
DSP	No	No	No	Yes	Yes	Yes
Floating point hardware	No	No	No	Yes	Yes	Yes
Bus protocol	AHB Lite	AHB Lite	AHB Lite, APB	AHB Lite, APB	AHB5	AXI4, AHB Lite, APB, TCM
Maximum # external interrupts	32	32	240	240	480	240
CMSIS Support	Yes					

Cortex-M7

- *Nested Vectored Interrupt Controller* : to organize the interruptions in order to reduce the suspensions
- *Wakeup Interrupt Controller (WIC)*: to detect an interruption and wake the processor from sleep mode
- *TCM*: tightly coupled memory
- *ECC*: error checking and correction
- *AHB-Lite*: simplified version of the AHB high-performance bus interface
- (*AXI-M*): single 64-bit AXI interface for on-chip or off-chip memory and devices



- *I*: instruction
- *D*: Data

Cortex-M7 documentation

... can be found here

<https://developer.arm.com/Processors/Cortex-M7>

<https://developer.arm.com/documentation/dui0646/b/>

<https://developer.arm.com/documentation/ddi0489/d/>

STM32H7: Architecture for performance

- Arm ® Cortex ® -M7 @ 280MHz
- Double precision FPU
 - Cortex®-M7 FPU core is binary compatible with the Cortex®-M4 core
- Memory Protection Unit (MPU), advanced DSP
- 16kB+16kB L1 I/D cache
- 16kBytes Instruction TCM and 128kBytes Data Tightly Coupled Memories (TCMs) for most critical code and data
 - → 0-wait state guaranteed
- Main DMA able to move over 2.2 Gbytes/s of data between chip resources

STM32H7: Architecture for power efficiency

Typ with @ $V_{DD} = 3\text{ V}$ @ $25\text{ }^{\circ}\text{C}$

Wake-up
time to RUN



* from Flash (Cache ON and Peripheral OFF), SMPS ON

** BAM run at 64MHz,SPI clock 16 MHz,
data stored in Smart Run Domain RAM via BDMA

*** VOS5, Flash LP mode, no IWDG ,SMPS ON

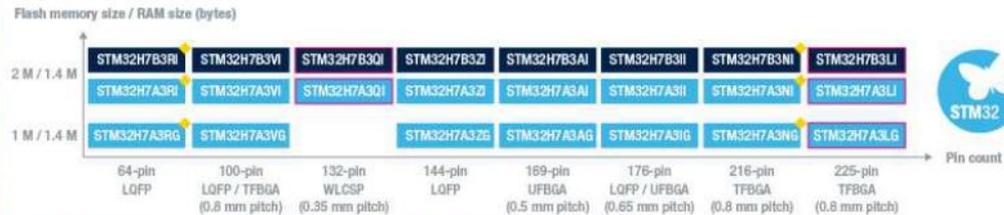
**** with RTC

STM32H7Ax family

System SMPS, LDO, USB and backup regulators POR/PDR/PVD/BOR Dual-power domains Xtal oscillators 32 kHz + 4 ~48 MHz Internal RC oscillators 32 kHz + 4, 48 & 64 MHz 3x PLL Clock control RTC/AWU 1x SysTick timer 2x watchdogs (independent and window) Up to 168 I/Os Cyclic redundancy check (CRC) Unique ID	Chrom-ART Accelerator™ Chrom-GRC™ JPEG Codec Acceleration	2-Mbyte dual-bank Flash memory RAM 1376KB incl. 64KB ITCM FMC/SRAM/NOR/NAND/ SDRAM 2x OctoSPI 1024-byte + 4-Kbyte backup SRAM
	Cache I/D 16+16 Kbytes	Connectivity TFT LCD controller HDMI-CEC 6x SPI, 3x I²S, 4x I²C Camera interface MDIO slave 2x FDCAN (Flexible Data rate) 1x USB 2.0 OTG FS 2x SDMMC 5x USART + 5 UART LIN, smartcard, IrDA, modem control 1x Low-power UART 2x SAI (Serial audio interface) SPDIF input x4 DFSDM (8 inputs/4 filters)
	Arm® Cortex®-M7 280 MHz	
	Floating point unit (DP-FPU)	
	Nested vector interrupt controller (NVIC)	
	JTAG/SW debug/ETM	
	Memory Protection Unit (MPU)	
	ROP, PC-ROP active-tamper	
	AXI and Multi-AHB bus matrix	
	3x DMA	
True random number generator (RNG)		
Control 2x 16-bit motor control PWM synchronized AC timer 10x 16-bit timers 2x 32-bit timers 2x Low-power timer	Analog 3x 12-bit, 2-channel DACs 2 x 16-bit ADC (up to 3.6 Msps) 20 channels/up to 2 MSPS Temperature sensor 2x COMP 2x OpAmp	
	optional Crypto/Hash processor 3DES, AES 256, GCM, CCM SHA-1, SHA-256, MD5, HMAC, OTFDEC Security services SFI and SB-SFU	

STM32H7A/7B

Single Core best balance between performance and power



Legend: All part numbers are available in LDO version or LDO + SMPS version unless otherwise specified
 ■ without HW crypto/hash ■ with HW crypto/hash ◆ LDO □ LDO + internal SMPS only

- Up to 280MHz
- Large embedded RAM 1.4MB
- Available in 1 and 2MB Flash
- Optional Crypto/Hash and security services
- 32 µA in STOP mode with 1.4 MB RAM content retained
- A wide choice of packages and form factors



Data sheets

- The datasheet of our MCU is document DS13195
 - e.g., pinout can be found at page 48 and 68
- while RM0455 is the reference manual