Power-line communication

[NXP_PLC]

■ Introduction

- Growth of green-energy sources' deployment creates a need to measure and control the distribution network dynamically
- Distribution networks may not only supply electric energy, but also act as communication channel
  - Power-line communication (PLC)
- Several different protocols compete in the CENELEC 50065 band A (9 kHz to 95 kHz) in Europe
  - mainly G3 and Prime
- Protocols
  - all use the OFDM modulation for physical layer
  - differ in the number of subcarriers, sample rates, and the forward error-correction calculation

G3

- Subcarriers used for the communication are 23 to 58, frequency range is 35.9 to 90.6 kHz
- Sampling frequency is 400 kHz, with 256 samples for the FFT calculation
- Data are encoded by the DBPSK (differential binary phase shift keying) or DQPSK (differential quadrature phase shift keying) modulations, and protected by convolutional and Reed Solomon codes

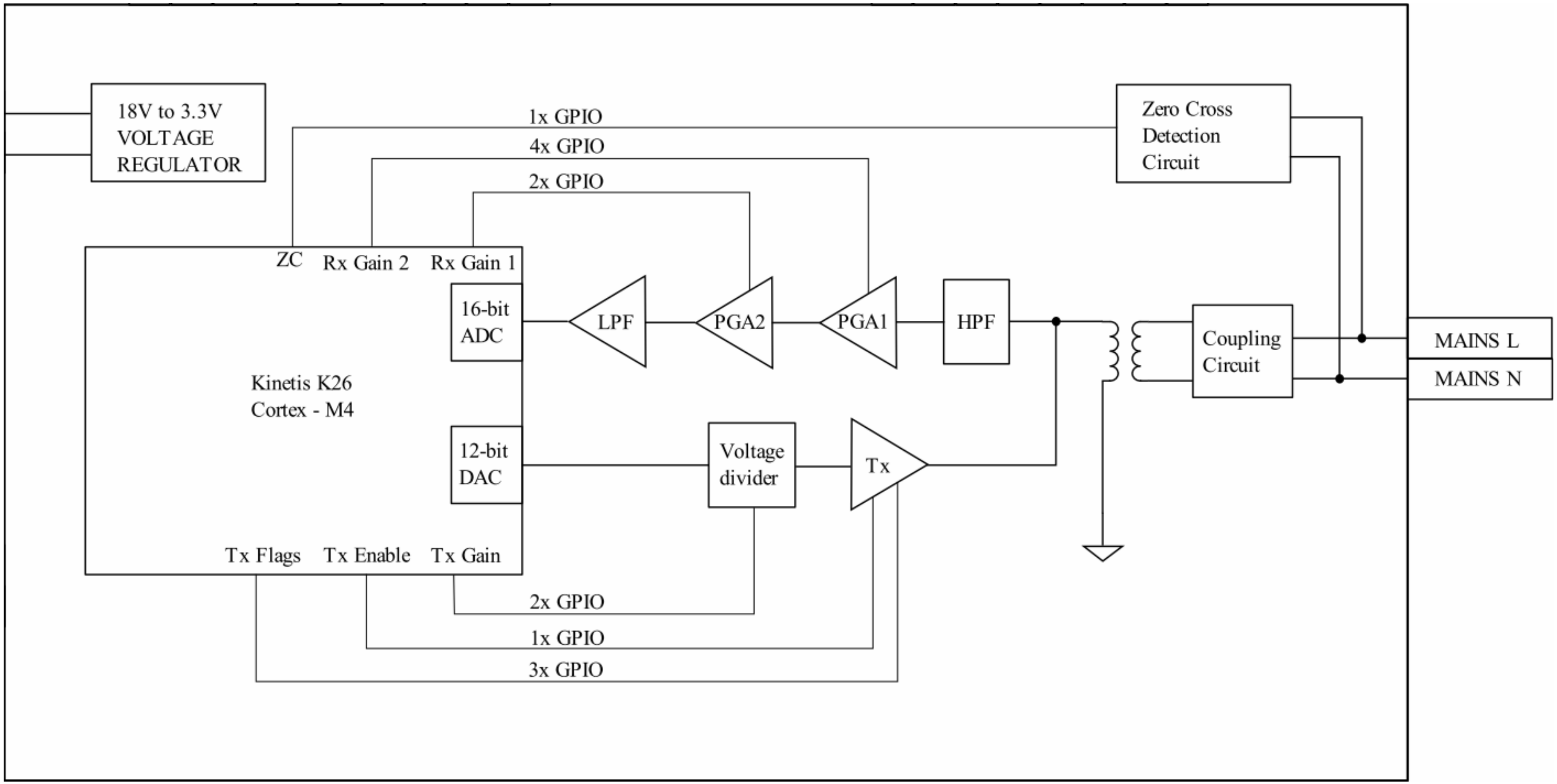
■ Prime

- Subcarriers used for the communication are 86 to 182, frequency range is 42 to 89 kHz
- Sampling frequency is 250 kHz, with 512 samples for the FFT calculation
- Data are encoded by the DBPSK (differential binary phase shift keying), DQPSK (differential quadrature phase shift keying) or D8PSK (differential 8-phase shift keying) modulations, and protected by convolutional code

■ G3 and Prime

- Both protocols can be demodulated on the ARM ® Cortex ® -M4 core
  - G3 requires more CPU time than PRIME
- There are many variants of higher layers above the PHY and MAC layers
  - IPv4, IPv6, or DLMS COSEM
- Each protocol has a different memory (RAM and FLASH) footprint
- It is convenient to use a software-defined communication

■ Example of block diagram



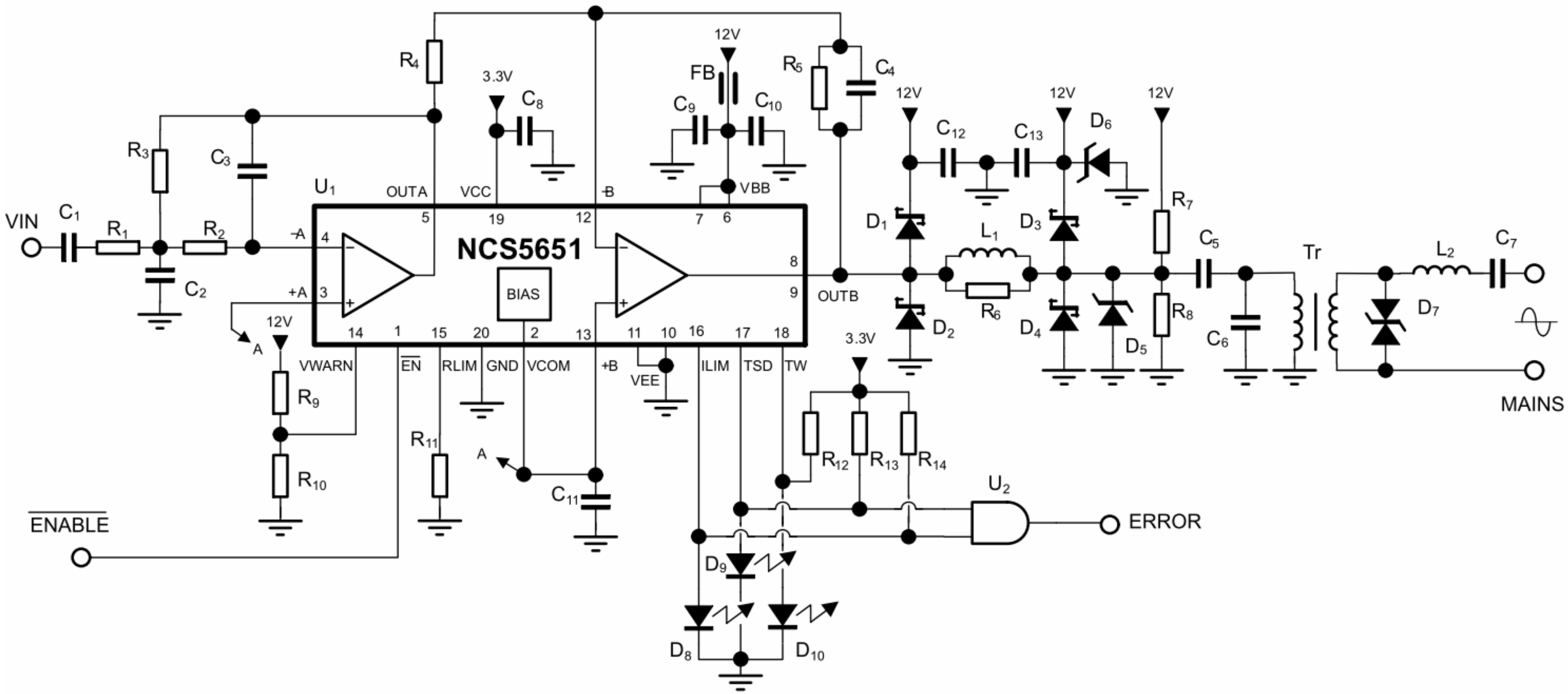
■ Example of block diagram

- Transmit/receive circuits are based on
  - standard operational amplifier for the receiver path
  - the NCS5651 line driver for the transmitter path
- There are filters tuned for the CENELEC 50065 band (35 kHz to 95 kHz) in both paths
- Receiver also contains two PGA modules to adjust the received signal to the ADC voltage level
- DAC and ADC are integrated in the Kinetis K26 MCU
- In the transmitter signal path, there is a voltage divider for decreasing the output voltage without compromising the DAC output signal quality
- The coupling circuit
  - filters out the 230 V AC
  - contains *many protection components* to remove spurious over-voltages

■ Transmitter

- Transmitter must have
  - good current-feeding capability to transmit to the low-impedance line
  - good signal harmonic distortion to achieve purity of the communication channel
- NCS5651 is a high-efficiency, Class A/B, low-distortion power-line driver
  - it consists of two OpAmps, one acting as a pre-amplifier, and the other as a line driver
- Trasmitter voltage level at NCS5651 output is ~12 Vpp max

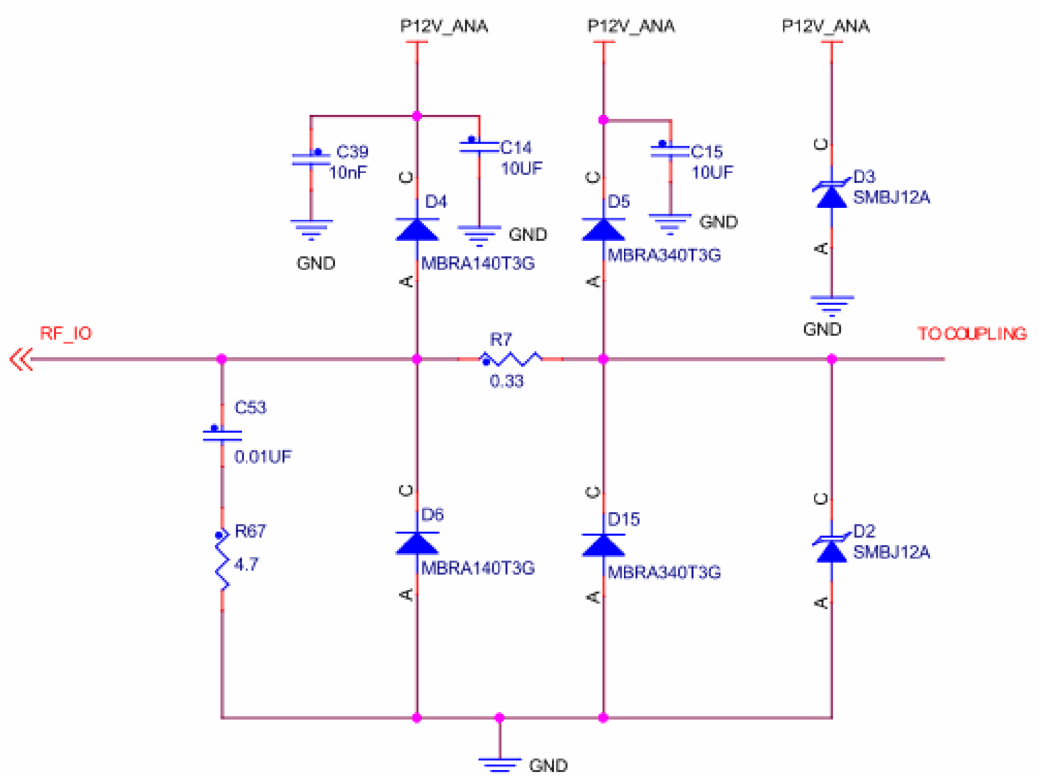
■ NCS5651: typical application schematic for PLC modem



- A 4-th order low pass filter is implemented
- The circuit formed by D1−D5, L1 and R6 is for protection

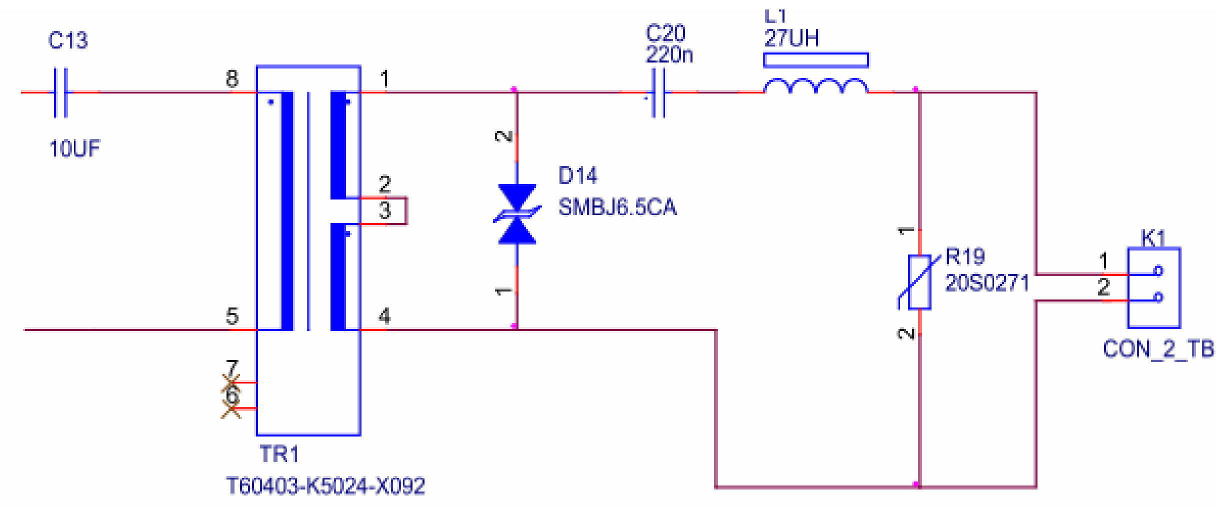
■ Protection circuit

- SMBJ12A are TVS (transient voltage suppression) diodes
- Diodes D5/D15 and D4/D6 short-cut the voltage spikes to the capacitors and the power supply
- The protection circuit introduces an unwanted 0.33 Ω resistivity to the transmitter coupling path



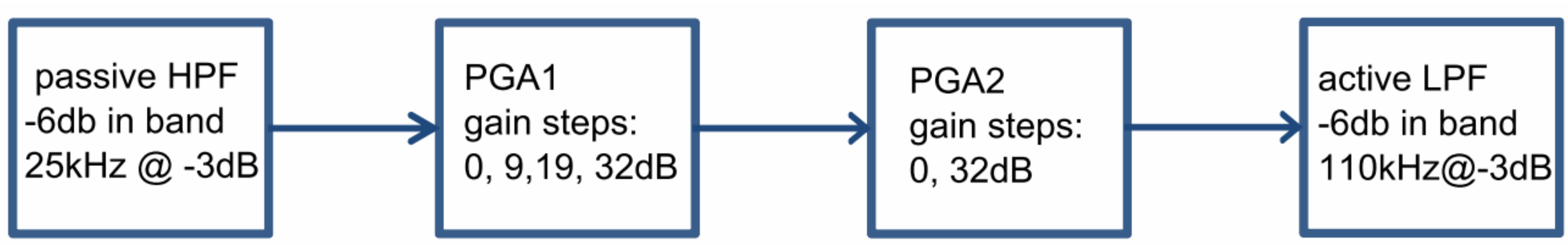
■ Coupling circuit

- C20/L1 serial resonant circuit forms the band-pass filter, and attenuates the 50 Hz mains voltage
  - resonation frequency is set to the middle of the communication band (~65 kHz)
- R19 varistor and the D14 TVS diode protect the coupling circuit over-voltages and spikes in the mains
- TR1 transformer provides galvanic isolation
- C13 removes the transmitter DC voltage signal
  - which would be short-cut on the transformer



■ Receiver

- The receiver path consists of
  - a passive high-pass input filter with a corner frequency of 25 kHz and an in-band attenuation of -6 dB
  - two PGA stages with a combined gain from 0 to 63 dB
  - a low-pass filter with a corner frequency of 110 kHz and an in-band attenuation of -6 dB
- After the final receiver stage (low-pass filter) the signal is 1.5 Vpp



■ Zero-crossing detection

- Some PLC protocols use the mains zero-crossing event for synchronization
- The signal is opto-isolated, and provides a rectangular analog output