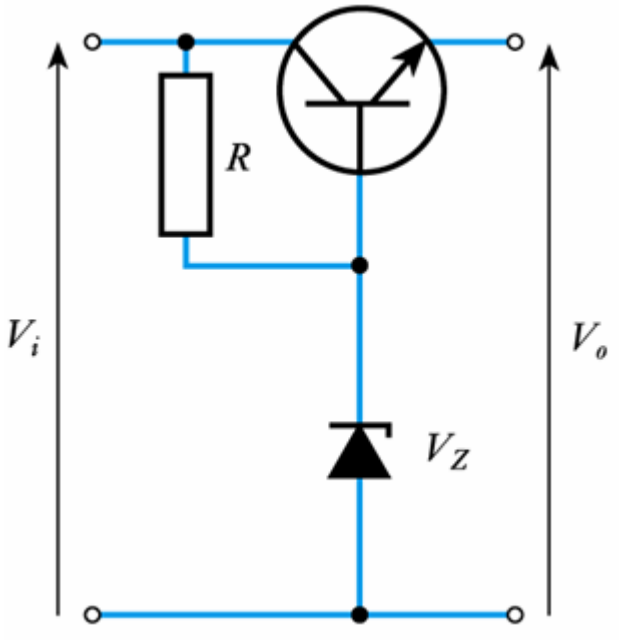
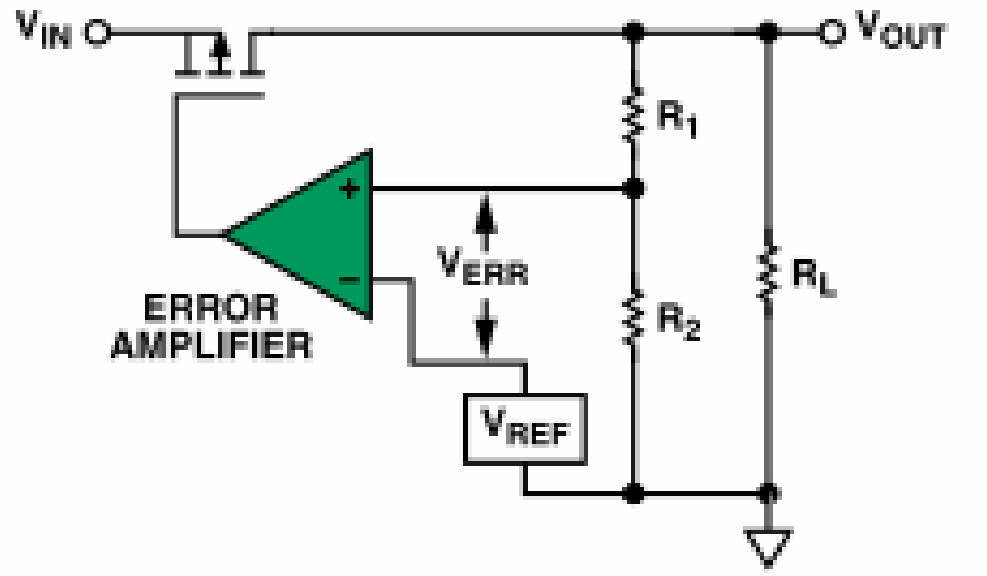
LDOs

[AD_vol41n2, TI_slyy151a, AD_57-3, AN-1120,TI_sbva026f,TI_slva068a]

LDO: introduction

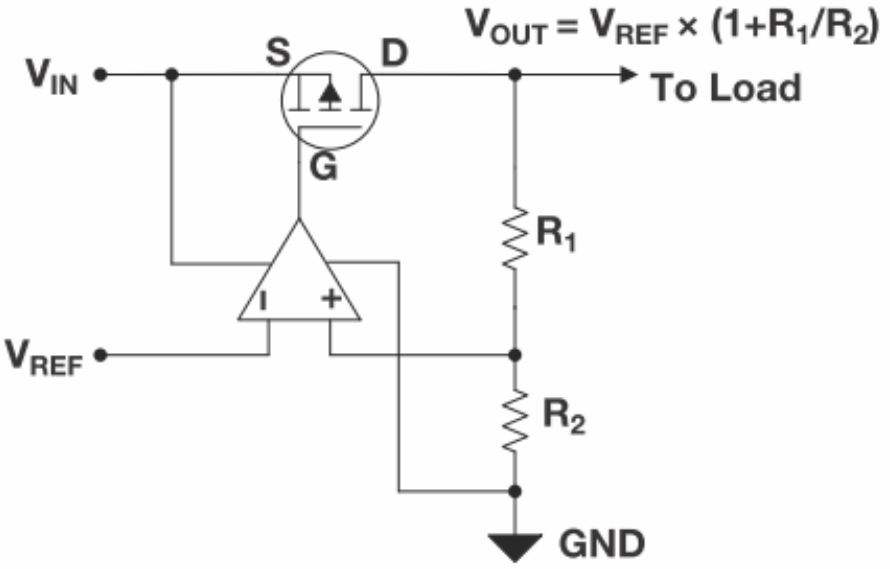
- Standard regulators typically employ NPN pass transistors, usually drop out at about 1-2 V.
- LDO regulators normally use (normally P-channel) MOSFETs; dropout voltage is typically 100-200 mV.
- *Dropout voltage* refers to the minimum voltage differential that the input voltage V_{IN} must maintain above the desired output voltage $V_{OUT(nom)}$ for proper regulation.





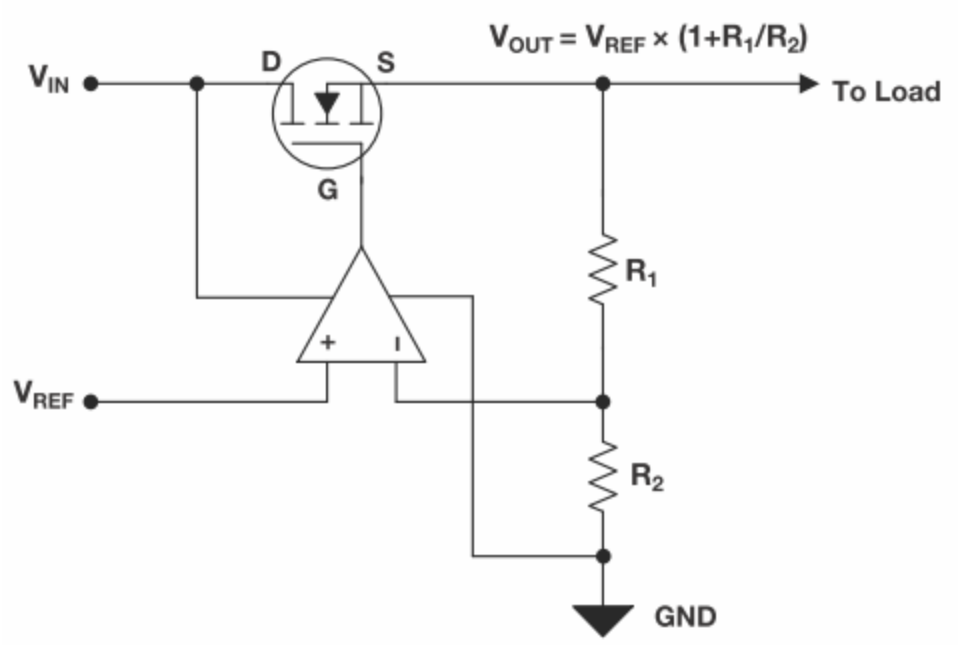
LDO: low-dropout voltage regulators

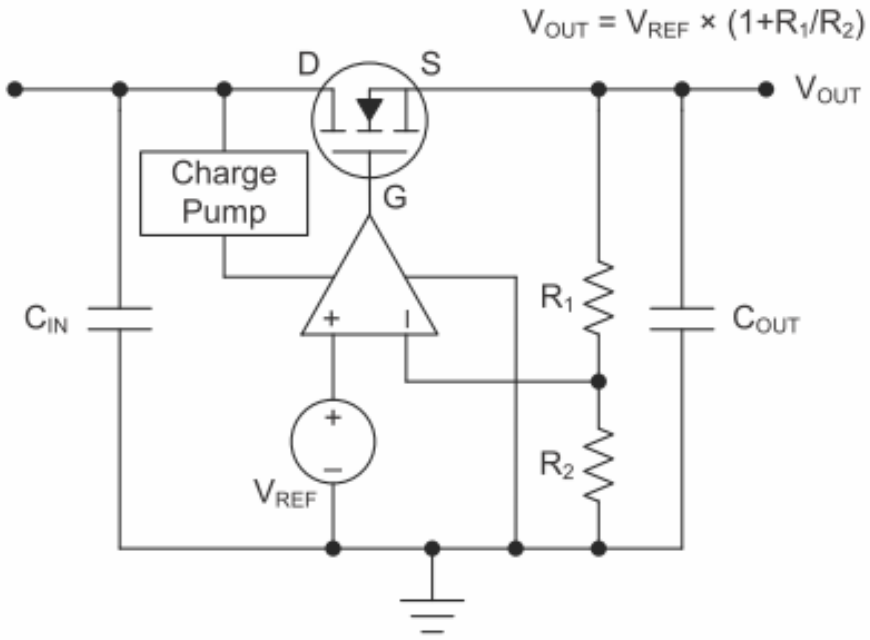
- The voltage reference is usually a band-gap type
- The error amplifier
  - takes a scaled-down version of the output
    $V_{OUT}\, R_2 / (R_1 + R_2)$,
  - compares it against the reference voltage,
  - and adjusts V_{OUT} via the series-pass element (the MOSFET).



LDO: low-dropout voltage regulators

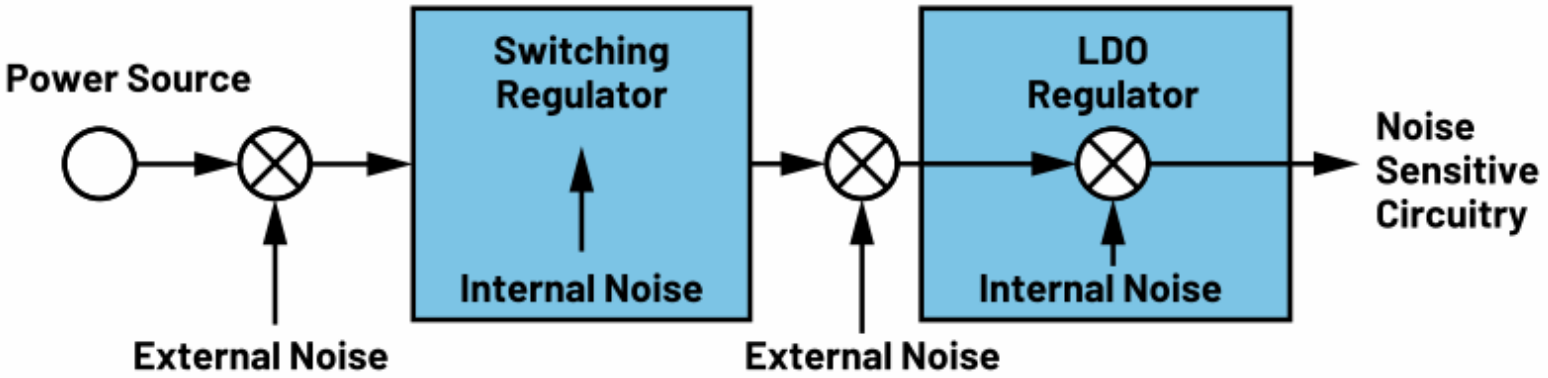
- NMOS LDOs do also exist, but it's more difficult to have low dropouts
  - unless an extra bias voltage is available, or is generated using a charge pump





LDOs and noise

- An LDO regulator is rarely used directly from the power source to other circuitry
  - the power loss would be too large in most cases.
- Instead, a designer typically uses either an AC-to-DC or DC-to-DC switching regulator.
- As the power source feeds the switching regulator, it may have its own noise and may pick up external noises
- Quite often, an LDO regulator is added to provide better regulation and suppress output ripple.

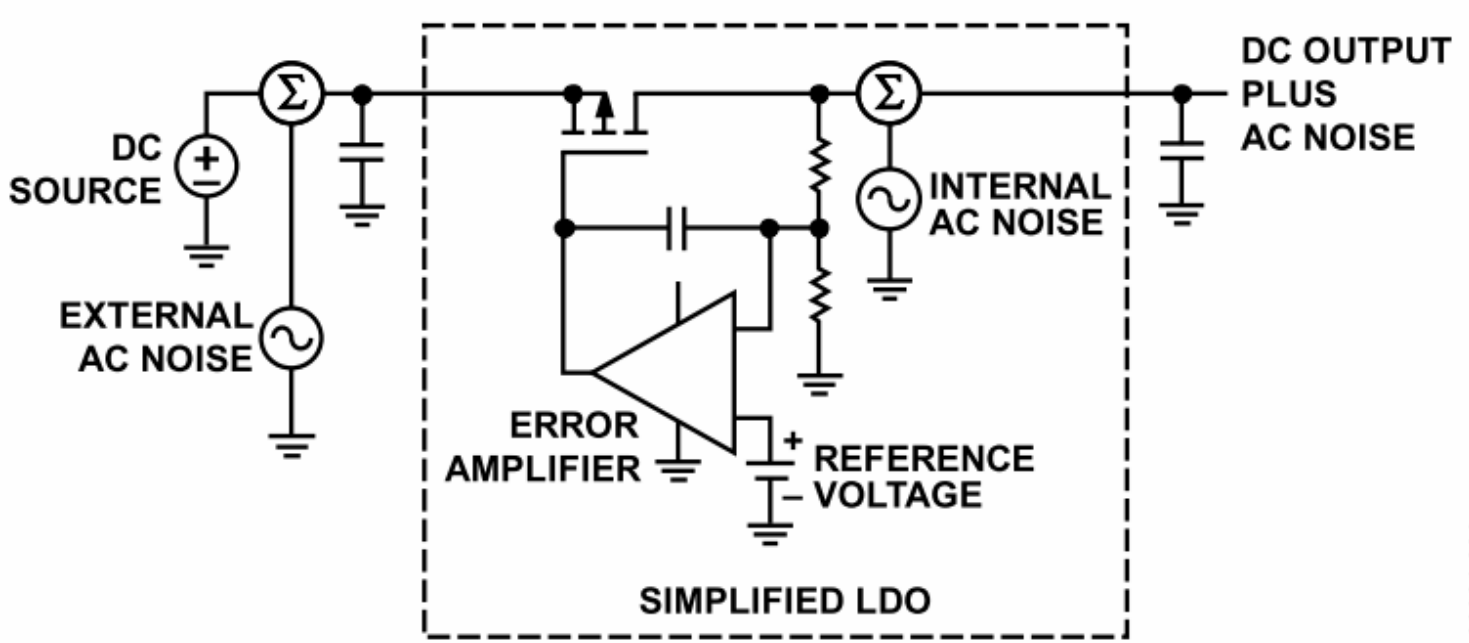


LDOs and noise

- Other extrinsic noise sources include the following:
  - electromagnetic fields that couple into sensitive circuits
  - mechanical shock or vibration that causes piezoelectric materials to generate unintended ac voltages
  - noise from other circuits that is conducted or radiated into circuits via the power supply or poorly designed PCB layouts

LDOs and noise

- This was *extrinsic* noise; *intrinsic* noise (noise that is internally generated by any electronic device) also exists
  - the error amplifier determines the PSRR of the LDO and its ability to reject noise at its input
  - intrinsic noise, however, always appears at the output of the LDO



LDOs and noise

- The major types of intrinsic noise include the following: thermal noise, 1/f noise, shot noise (and burst, or popcorn, noise)
  - the major sources of intrinsic noise in LDOs are the internal reference voltage and the error amplifier

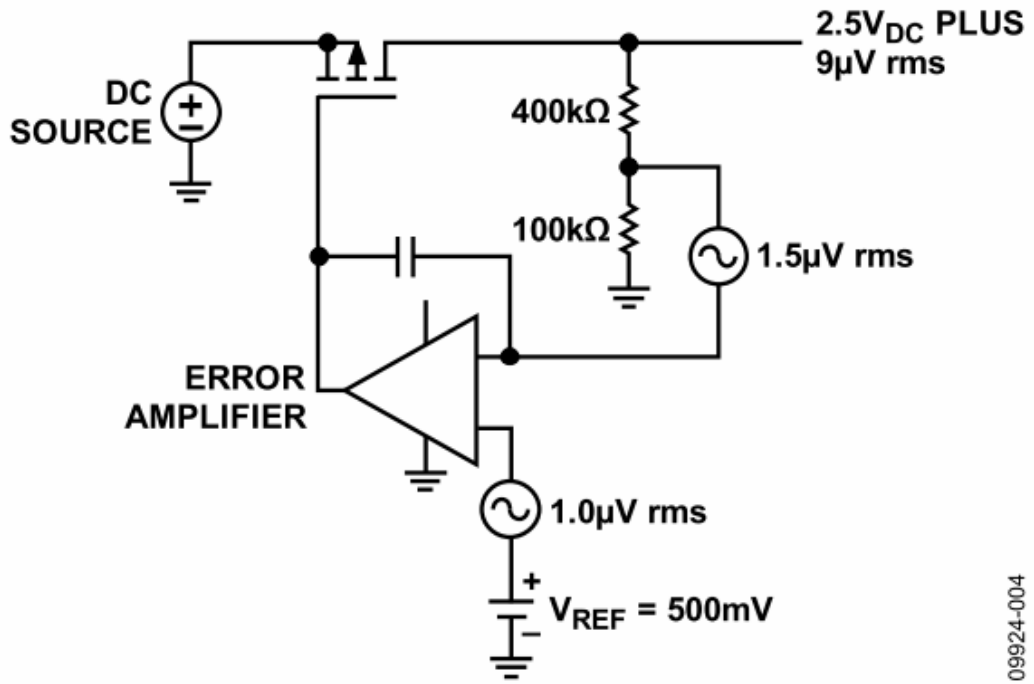
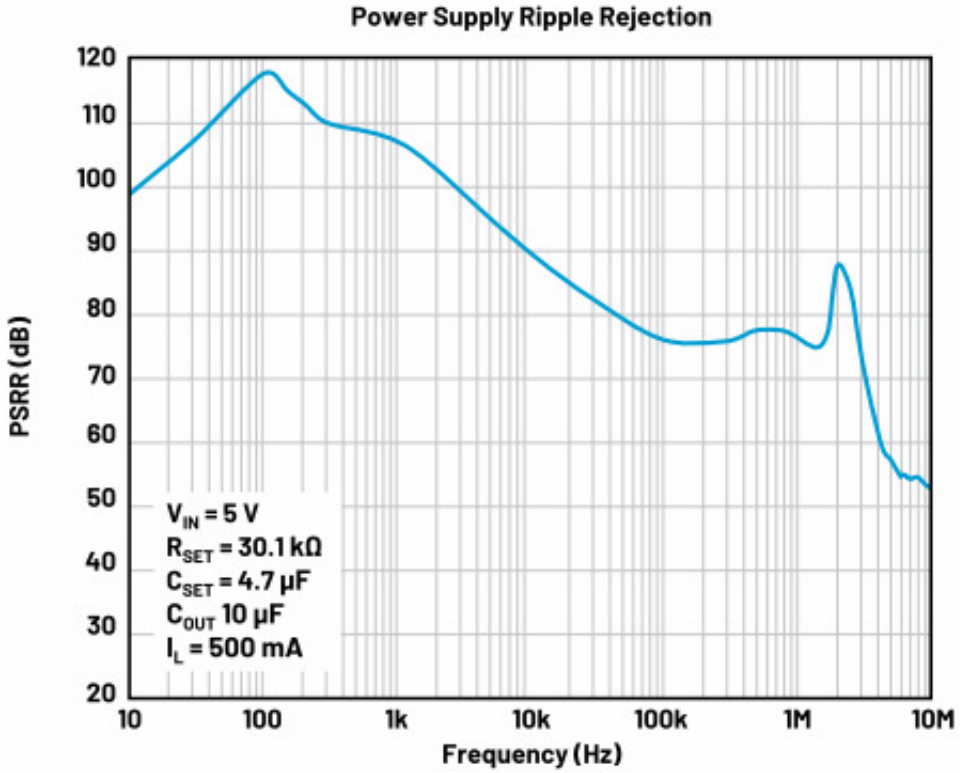


Figure 4. Noise Contributions from Reference and Error Amplifier (ADP223)

LDOs and noise

- LDOs are mainly characterized by three key factors:
  - PSRR
  - total integrated output noise
  - and noise spectral density
- *PSRR* represents the fluctuations in the output voltage caused by the input voltage

$$PSRR = 20\log(VE_{IN}/VE_{OUT})$$

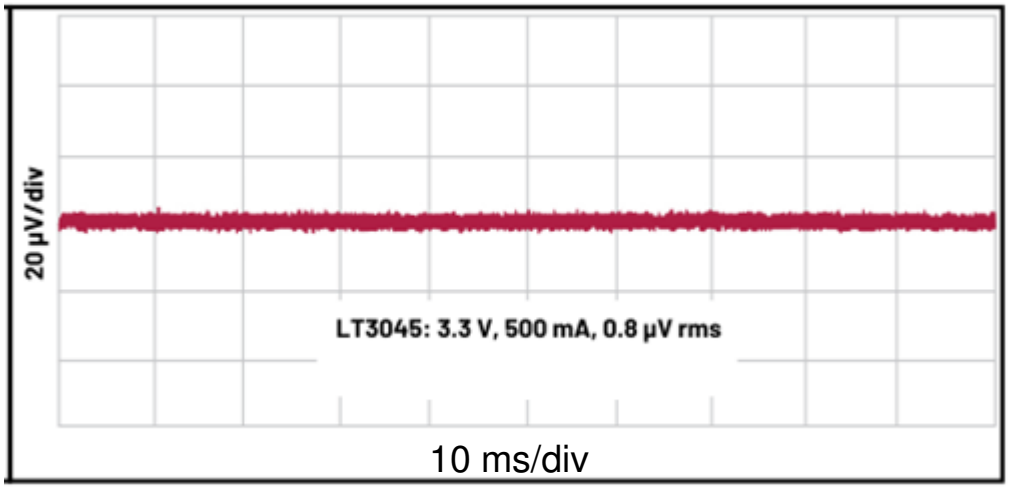


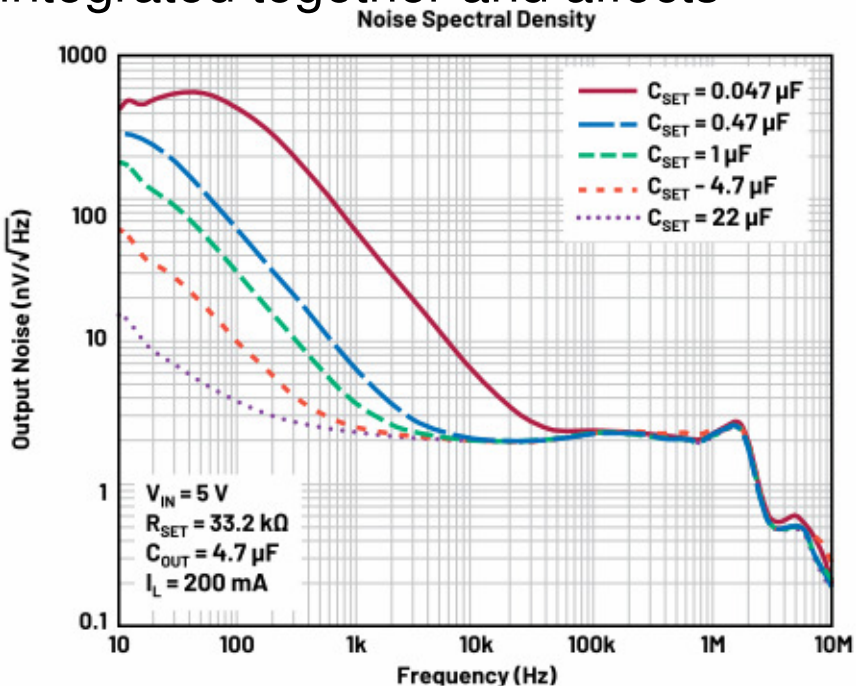
LDOs and noise

- For a given load current, the PSRR of an LDO can be improved in several ways:
  - operate the LDO with at least 1 V of headroom (the input-to-output voltage differential)
    - some LDOs, such as the ADP151, perform well with as little as 500 mV
  - use an LDO with a maximum load current rating of at least 1.5× greater than the expected load
  - add external filtering to the input or output of the LDO
  - cascade two or more LDOs, if there is adequate headroom

LDOs and noise

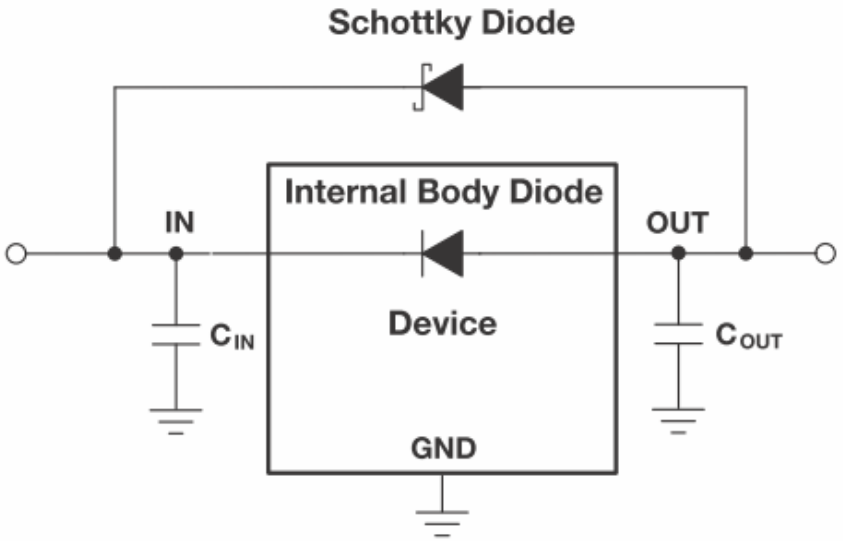
- *Noise density vs. frequency* is important e.g. in communication-related applications with a regulation on the frequency spectrum, or sensor applications where the ambient signal is sensed and processed within a certain band
- *Total (integrated) output noise* is the rms value of the spectral noise density integrated over a finite frequency range.
  - for ADC and DAC conversion circuitry, all the LDO regulator noise from DC to the bandwidth of the system is integrated together and affects system accuracy

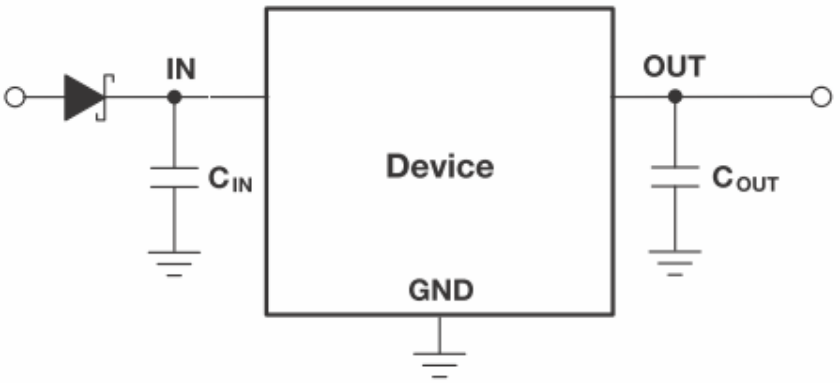




LDOs: preventing *reverse* current

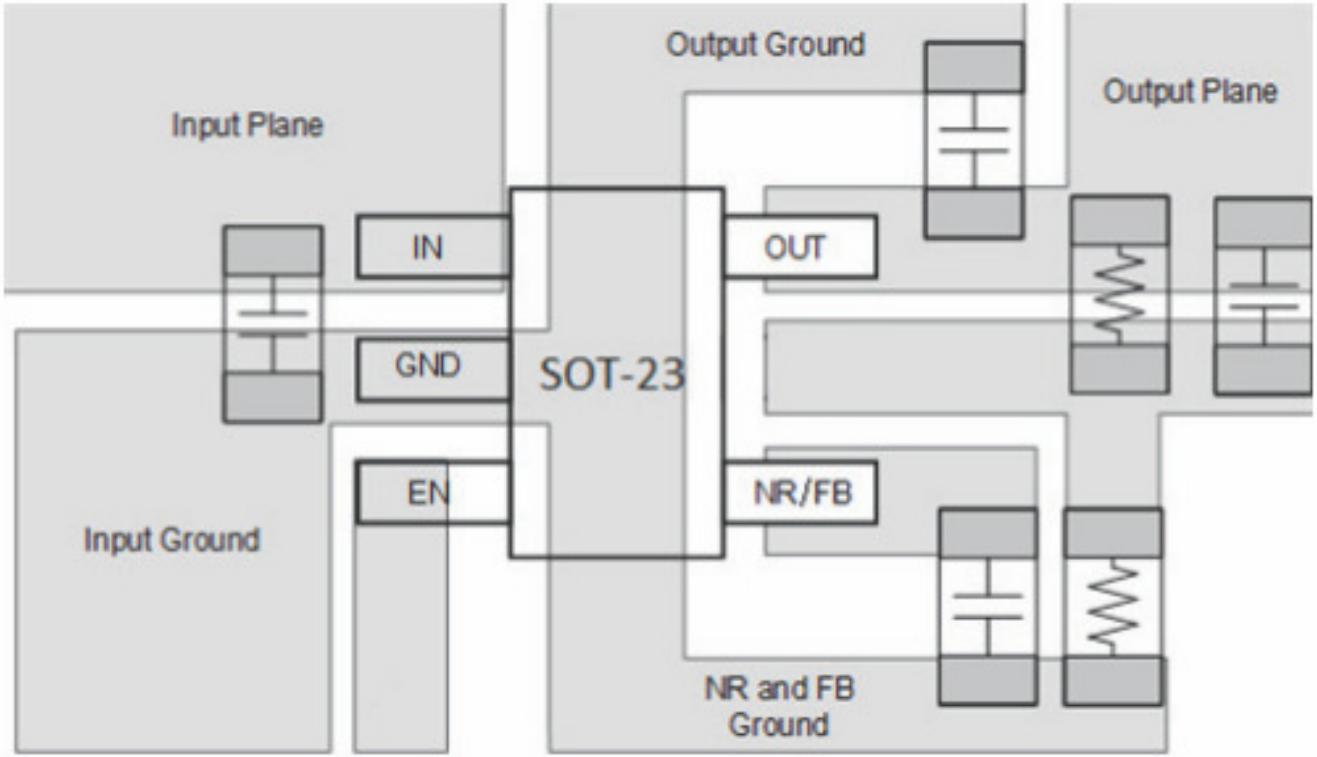
- The bulk is connected to the source -> a parasitic body diode forms in the FET
  - this parasitic diode is called the body diode
- The body diode can turn on when the output exceeds the input voltage plus the ~0.7 V of the parasitic diode.
- Current flow through this diode can cause device damage through device heating, electromigration or latch-up events
- A couple of possible solutions:





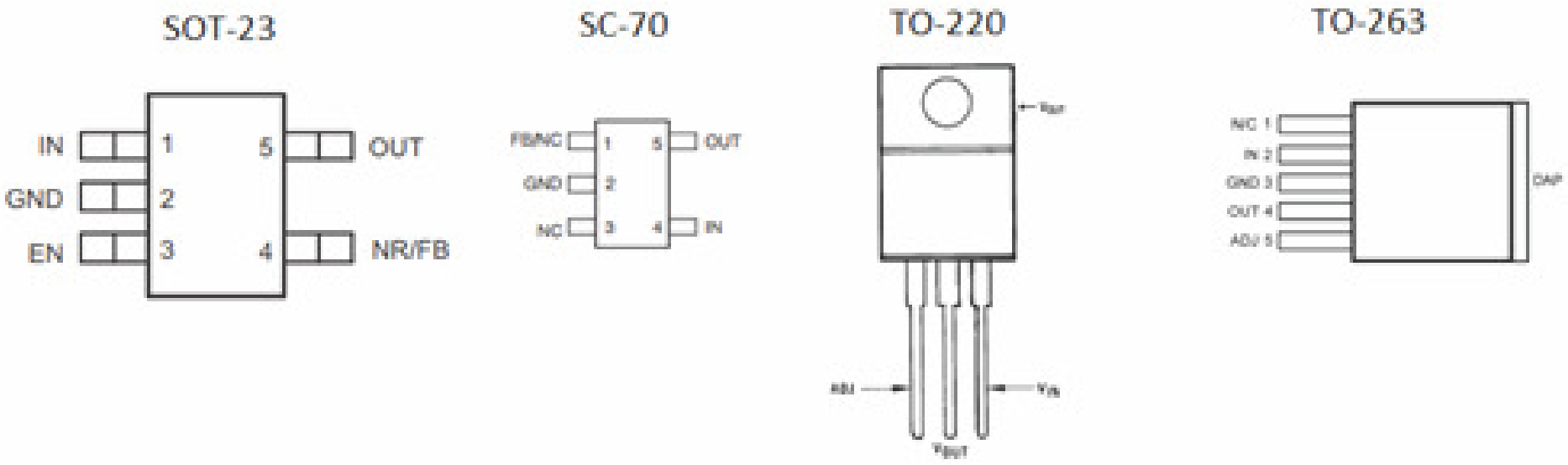
LDOs: power dissipation

- When power dissipates, heat escapes the LDO through the thermal pad -> increasing the size of the input, output and ground planes in the PCB will decrease the thermal resistance
- When designing a multilayer PCB, it's usually a good idea to use a separate layer covering the entire board with a ground plane



LDOs: power dissipation

- Heat sinks decrease $R_{\theta JA}$, but add size and cost to the system



LDOs: quiescent current

- *Quiescent current* is the current drawn by a system in standby mode with light or no load

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + (V_{IN} \times I_Q)$$

- Quiescent current is commonly confused with *shutdown current*, which is the current drawn when a device is turned off but the battery is still connected to the system
- Both specifications are important in any low battery-consumption design