SMPS design example

[TI_slva034a (from page 24), tl5001]

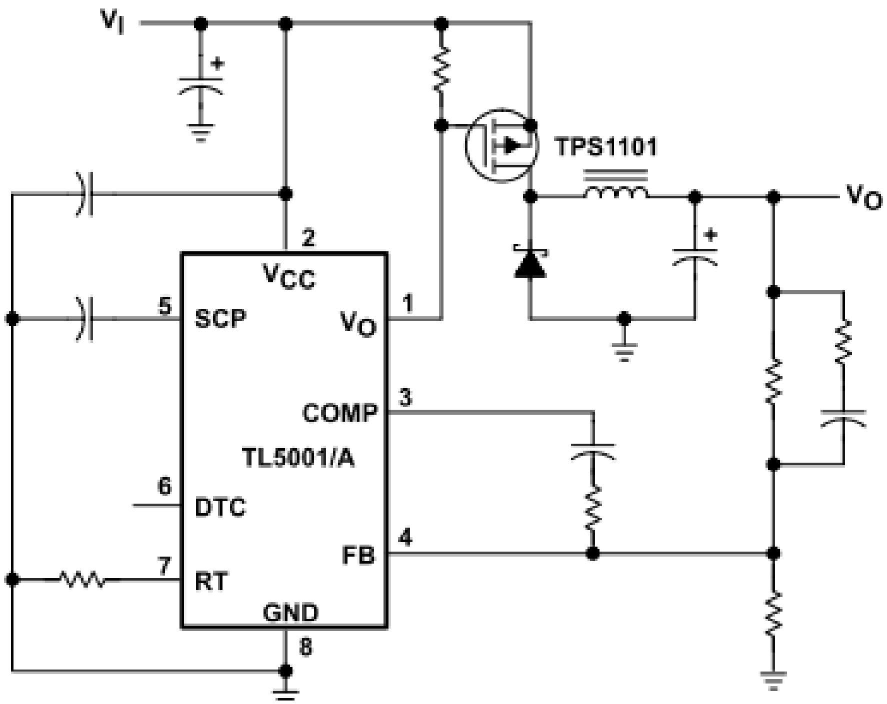
5 V to 3.3 V at 0.75 A stepdown converter

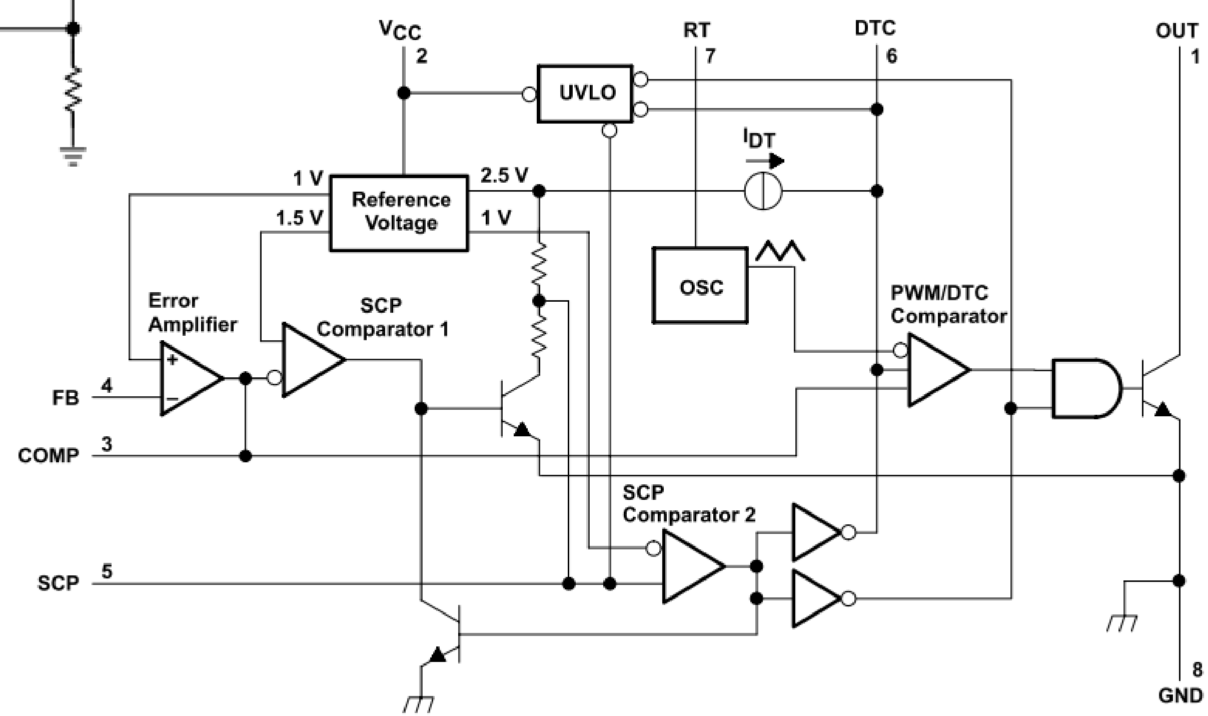
- Specifications as reported below
- IC: TI PWM controller TL5001 at f_s = 200 kHz
- External power FET

Specifications

Input voltage range, V_I	4.75 V to 5.25 V
Output voltage, V_O	3.3 V
Output current, I_O	0 A to 0.75 A
Output ripple voltage	≤50 mV
Regulation	1%
Efficiency	>70%
Ambient temperature range, T_A	–20°C to 65°C

TL5001 functional block diagram and typical application





Duty-Cycle estimates

- Estimate the power-switch duty cycle over the range of input voltages using

$$D = \frac{V_O + V_d}{V_I - V_{sat}}$$

- The duty cycle for V_I = 4.75, 5, and 5.25 V is 0.84, 0.80, and 0.76, respectively

Output filter: inductor

- Choose *L1* to maintain continuous-mode operation to 20% of the rated output current

$$\Delta I_O = 2 \times 0.2 \times I_{O(max)} = 2 \times 0.2 \times 0.75 = 0.3 \text{ A peak-to-peak}$$

- The inductor value is calculated using $L1 = \dfrac{\left(V_I - V_{sat} - V_O\right)DTs}{\Delta I_O}$

$$L1 = \frac{(5.25 - 0.25 - 3.3)(0.76)\left(5 \times 10^{-6}\right)}{0.3} = 21.5\ \mu H$$

- Use *L1* = 20 μH (Coiltronics CTX20-1, 1.15 A dc-current rating, surface-mount package).
- Using the new value for *L1*, $\Delta I_O = 323\ mA_{pp}$

$$\Delta I_O = \frac{\left(V_I - V_{sat} - V_O\right)DTs}{L1}$$

Output filter: capacitor

- For the ideal (no ESR) capacitor, the 50 mV ripple requires

$$C = \frac{\Delta I_O}{8 \times f_s \times \Delta V_O} = \frac{0.323}{(8)\left(200 \times 10^3\right)(0.05)} = 4.04\ \mu F$$

- For the ESR only, the 50 mV peak-to-peak requires

$$ESR = \frac{\Delta V_O}{\Delta I_O} = \frac{0.05}{0.323} = 155\ m\Omega$$

- In order to have some margin, a 100 uF, 10 V tantalum electrolytic with an ESR of 100 mΩ maximum is chosen
  - the ideal capacitor gives ΔV_O = 50m(4.94μ/100μ) = 2.5 mV
  - the ESR gives ΔV_O = 50m(100m/155m) = 32 mV

Power switch: FET

- Preliminary estimate: a maximum V_{ds} of 0.25 V gives

$$0.25\ \text{V} \div 0.75\ \text{A} = (333\ \text{m}\Omega)$$

- A low V_{GSth} is desirable
- The TPS1101D is a 15 V p-channel MOSFET in an SO-8 package, $r_{DS(on)} = 0.19\ \Omega$ maximum with a 4.5 V gate drive
- Power dissipation is

$$P_D = I_O^2 \times r_{DS(on)} \times D + 0.5 \times V_I \times I_O \times t_{r+f} \times f_s$$

  - where t_{r+f} = 100 ns = total MOSFET switching time (turn-on and turnoff) and $r_{DS(on)} = 0.25\ \Omega$ has been adjusted for temperature (100 °C)

$$P_D = \left[\left(0.75^2\right)(0.25)(0.80)\right] + \left[(0.5)(5)(0.75)\left(0.1 \times 10^{-6}\right)\left(200 \times 10^3\right)\right]$$

$$P_D = 113 + 38 = 151\ \text{mW}$$

Power switch: FET

- The thermal impedance $R_{\theta JA}$ = 158 °C/W gives (with T_A=65 °C) a junction temperature

$$T_J = T_A + (R_{\theta JA} \times P_D) = 65 + (158 \times 0.151) = 89°C$$

- so no heat sink is required

Power switch: catch diode

- The power dissipation in this design is very low
- Consequently, a small surface-mount Schottky device such as the MBRS140T3 is ok
  - 1 A forward current
  - $V_{breakdown}$ = 40 V
  - conduction drop V_d = 0.35 V at 1 A and 100 °C
- The power dissipation is

$$P_D = I_O \times V_d \times (1 - D)$$

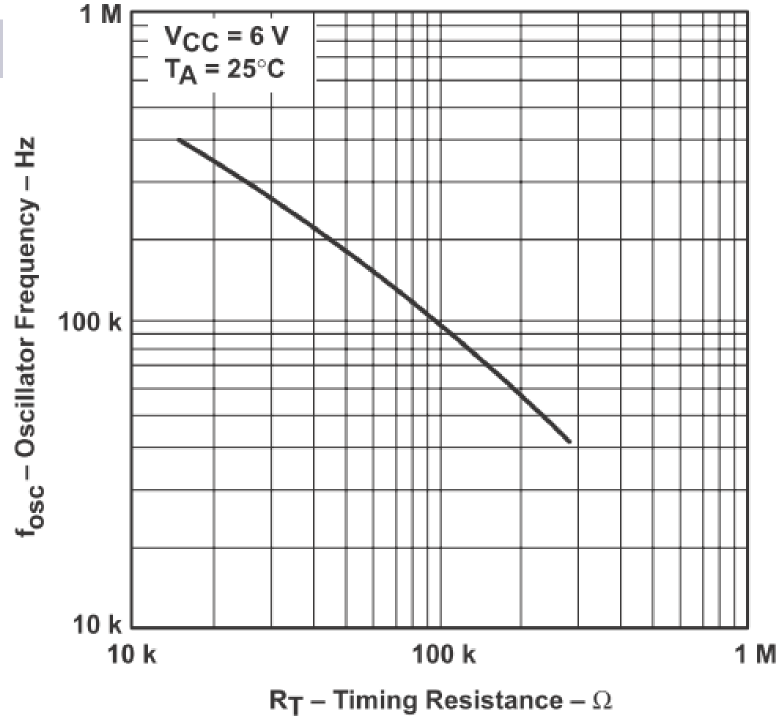
$$P_D = 0.75 \times 0.35 \times (1 - 0.76) = 63 \text{ mW}$$

  - signal diodes are in the 300 to 400 °C/W range;

    T_J = 65+400*0.063 =90.2 °C, ok

Controller design

- *Oscillator frequency*: from the graph, choose *R2* = 43 kΩ to set the oscillator frequency to 200 kHz
- *Dead-time control (DTC):* provides a means of limiting *D* (important for boost and flyback converters); not needed -> the DTC resistor is omitted



- *Soft-start timing:* slows the rise of the output voltage to prevent excessive overshoot*.* The soft-start capacitor is charged with a current approximately equal to the current flowing from the RT terminal (I_{R2}). The output voltage should be in regulation by the time *C5* has charged to 1.4 V. Choose *C5* such that the output voltage comes up in 6 ms.

$$\text{Charging current} = \frac{1\ \text{V}}{43\ \text{k}\Omega} = 23.3\ \mu\text{A}$$

$$C5 = \frac{\left(23.3 \times 10^{-6}\right)\left(6 \times 10^{-3}\right)}{1.4} = 0.1\ \mu\text{F}$$

Controller design

- The TL5001 includes *short-circuit protection* (SCP)
- When a short circuit occurs, SCP comparator 1 starts an RC timing circuit
- If the short is removed and the error-amplifier output drops below 1.5 V before time out, normal converter operation continues, otherwise the timer sets the latching circuit and turns off the TL5001 output transistor
- t_{SCP} must be much longer (10-15 times) than the converter start-up period
- From the datasheet (t in s, C in uF): $$C_{SCP} = 12.46 \times t_{SCP}$$

then $C4 = C_{SCP}$ = 12.46*(6ms*15) = 1.2 uF

Controller design

- *Output sense network*
  - the worst-case input bias current for TL5001 is 0.5 uA
  - -> the divider current must be ~1000 × 0.5 mA = 0.5 mA
  - the reference voltage of the comparator is $V_{ref} = 1$ V
  - when $V_O = 3.3$ V we want 1 V at the voltage divider output -> we may set

    $R5 = 7.5\ \mathrm{k}\Omega$

    $R6 = 3.24\ \mathrm{k}\Omega$
- *Undervoltage-lockout protection* (UVLO)
  - the undervoltage-lockout circuit turns the output transistor off and resets the SCP latch whenever the supply voltage drops too low
  - nothing to do for this ☺

Controller design: loop compensation

- We want to shape the error-amplifier frequency response to stabilize the dc/dc converter feedback control loop without destroying its ability to respond to line and/or load transients
- We'll implement a PID controller
  - in particular, just the integral part

- The response of the pulse-width modulator and power switch operating in CCM can be modeled as a simple gain block
  - the magnitude of the gain is the change in output voltage for a change in the pulse-width-modulator input voltage
  - in this IC, increasing PWM modulator input voltage from 0.6 V to 1.4 V increases D from 0 to 100% and V_O from 0 V to 5 V at the nominal input voltage

$$A_{PWM} = \frac{\Delta V_O}{\Delta V_{O(COMP)}} = \frac{(5-0)}{(1.4-0.6)} = 6.25 \Rightarrow 15.9 \text{ dB at nominal input}$$

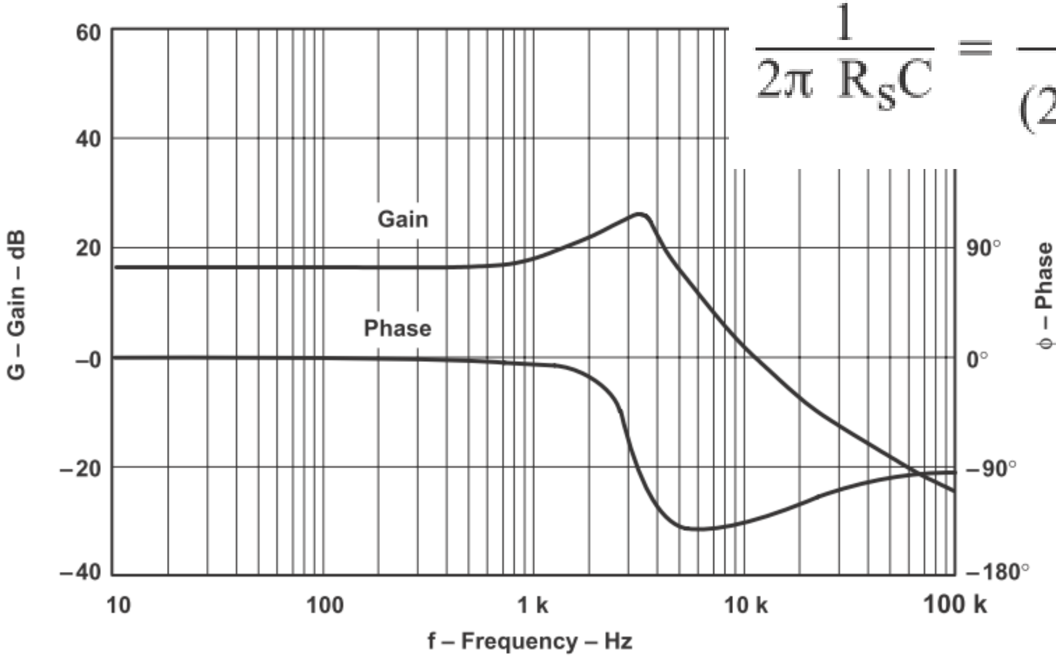
Controller design: loop compensation

- The output filter produces an underdamped complex-pole pair at the filter's resonant frequency,

$$\frac{1}{2\,\pi\,\sqrt{LC}} = \frac{1}{2\,\pi\,\sqrt{\left(20\times10^{-6}\right)\left(100\times10^{-6}\right)}} = 3.56\ \text{kHz}$$

- and the capacitor ESR (0.1 Ω) puts a zero in the response above the resonant frequency

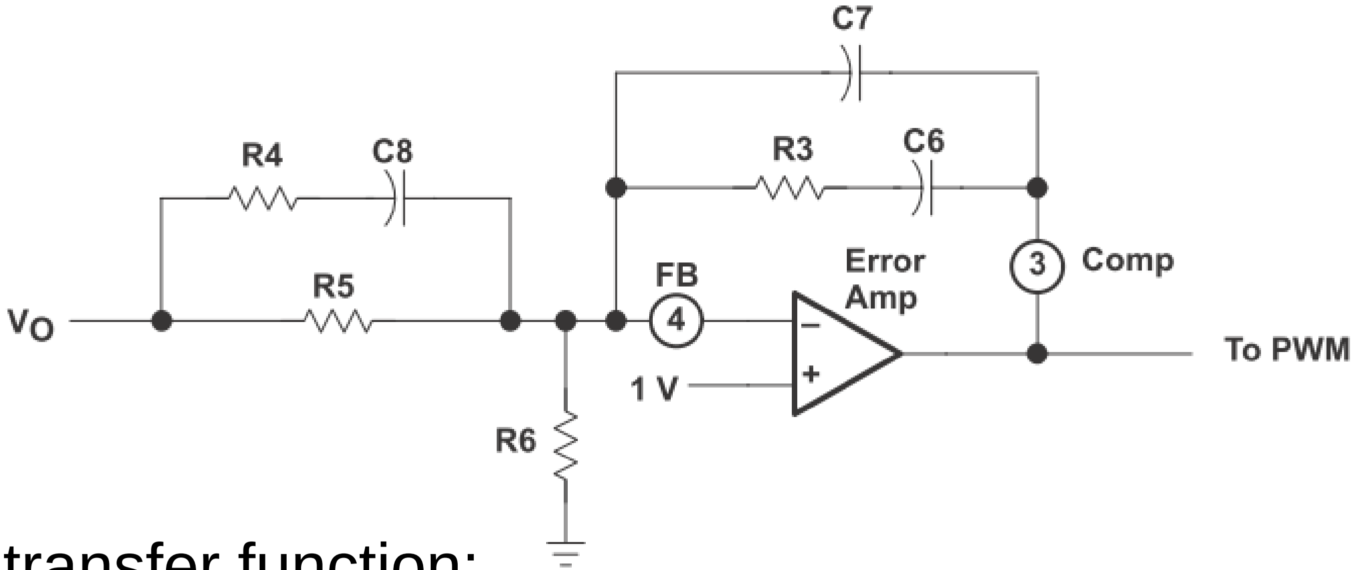
$$\frac{1}{2\pi\,R_S C} = \frac{1}{(2\pi)(0.1)\left(100\times10^{-6}\right)} = 15.9\ \text{kHz}$$



open-loop response (error amplifier not included) obtained from a simple SPICE simulation

Controller design: loop compensation

- We choose a unity-gain frequency of approximately 20 kHz to provide good transient response
- The standard compensation network chosen for this example



has this transfer function:

$$A_{ea}(S) = -\left[\frac{1}{S\ R5(C6 + C7)}\right]\left[\frac{[S(R5 + R4)\ C8 + 1]\ (S\ R3\ C6 + 1)}{(S\ R4\ C8 + 1)\ [S\ R3\ (C6 \parallel C7) + 1]}\right]$$

no, series

Controller design: loop compensation

- *Integrator gain*, 1/[R5·(C6+C7)]: sets the open-loop unity-gain frequency
- *Zeros*: locate them at approximately the same frequency as the output-filter poles (3.6~3.56 kHz) to roughly compensate them
- *Pole* at 1/(2π·R4·C8): position them at approximately the same frequency as the zero in the output filter (15.9 kHz) to compensate it
- *Pole* at 1/(2π·R3·(C6ΣC7)): place them between $f_s/2$ and f_s (100 kHz) to minimize noise at the pulse-width-modulator input

$$A_{ea}(S) = -\left[\frac{1}{S\ R5(C6 + C7)}\right]\left[\frac{[S(R5 + R4)\ C8 + 1]\ (S\ R3\ C6 + 1)}{(S\ R4\ C8 + 1)\ \left[S\ R3\ \left(C6 \Sigma\ C7\right) + 1\right]}\right]$$

Controller design: loop compensation / integrator gain

- From the bode plot, gain of the modulator/LC filter at 20 kHz is –8 dB
- The two zeros are set at 3.6 kHz (~3.56 kHz), so at 20 kHz they give +14.5*2=+29 dB (calculated or using spice)
- so the integrator at 20 kHz must have a gain of – 21 dB = 0.089
  - -8-21+29=0 dB
- Normally, C6 >> C7, so from

$$\frac{1}{(2\pi)\left(f_T\right)(R5)(C6 + C7)} = 0.089 \qquad C6 = \frac{1}{(2\pi)\left(f_T\right)(R5)(0.089)}$$

we find (R5 = 7.5 kΩ, f_T= 20 kHz) C6 = 12 nF

- Actually, the pole we insert at 15.9 kHz should also be considered
  - it adds -4 dB, so the integrator should be set at -17 dB:

    -8-17+29-4=0 dB

Controller design: loop compensation / other poles and zeros

- R3 sets a zero at 3.6 kHz

$$R3 = \frac{1}{(2\pi)(f)(C6)} = \frac{1}{(6.28)\left(3.6 \times 10^{3}\right)\left(0.012 \times 10^{-6}\right)} = 3.69\ k\Omega \Rightarrow \text{Use } 3.6\ k\Omega$$

- R4 and C8 are chosen to provide an additional zero, f_Z, at 3.6 kHz and a pole, f_P, at 15.9 kHz; by solving the system we get

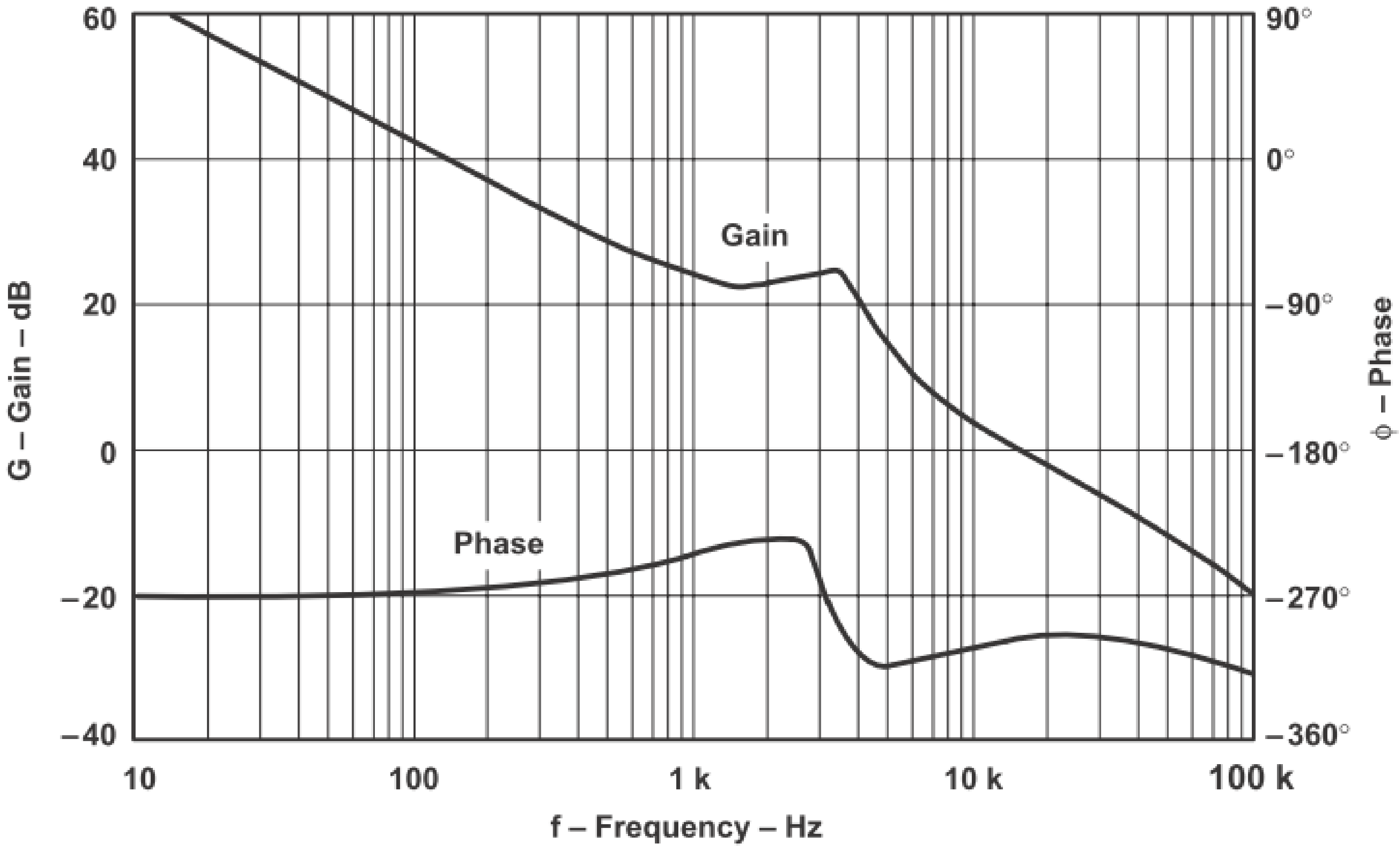
$$C8 = \frac{\frac{1}{f_Z} - \frac{1}{f_P}}{(2\pi)(R5)} = \frac{\left[\frac{1}{3.6\times 10^{3}} - \frac{1}{15.9\times 10^{3}}\right]}{(6.28)\left(7.5 \times 10^{3}\right)} = 0.0046\ \mu F \Rightarrow \text{Use } C8 = 0.0047\ \mu F$$

$$R4 = \frac{1}{(2\pi)\left(f_P\right)(C8)} = \frac{1}{(6.28)\left(15.9 \times 10^{3}\right)\left(0.0047 \times 10^{-6}\right)} = 2.13\ k\Omega \Rightarrow \text{Use } 2.0\ k\Omega$$

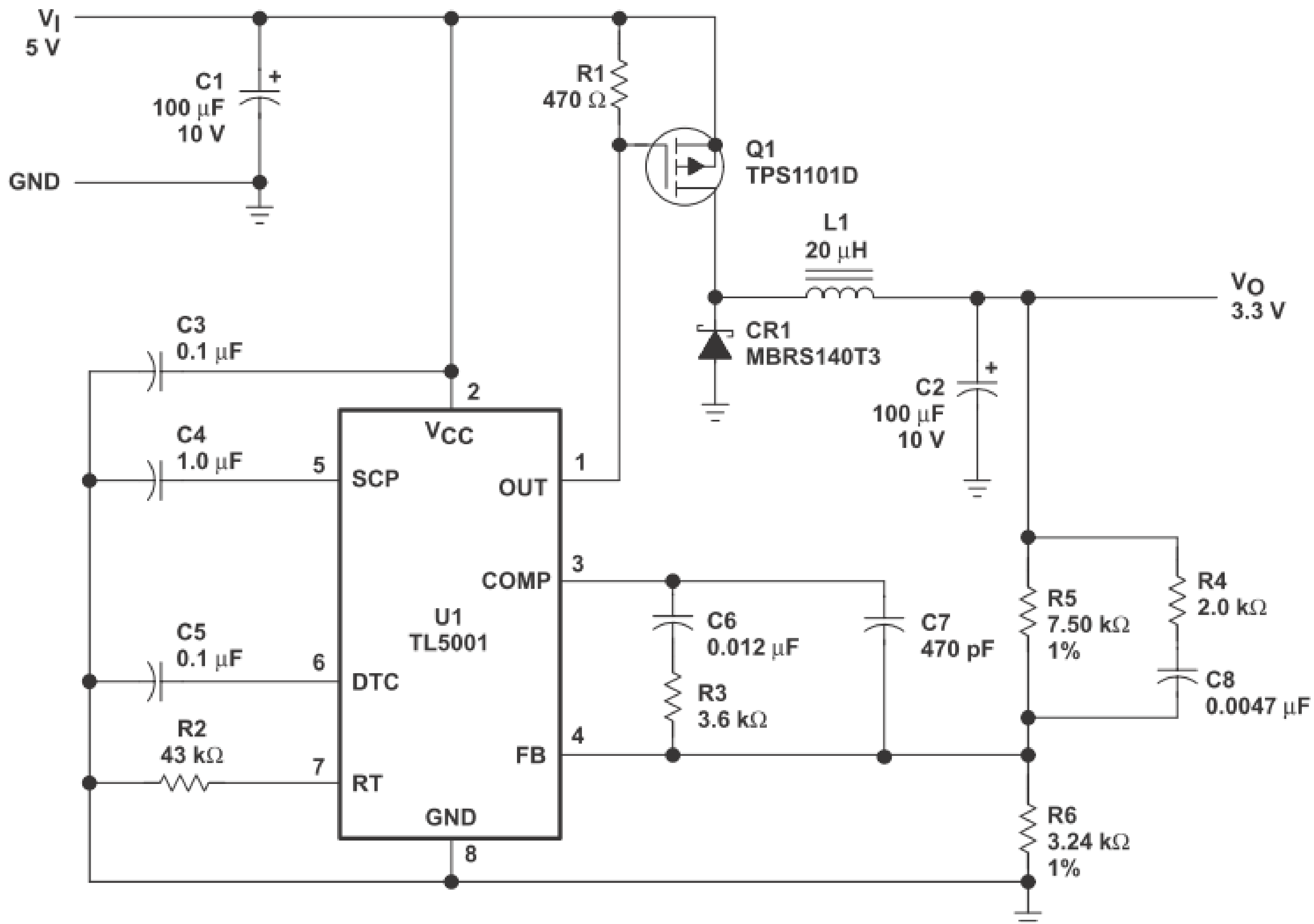
- C7 is chosen to provide the pole at 100 kHz; with C6 >> C7

$$C7 = \frac{1}{(2\pi)\left(f_p\right)(R3)} = \frac{1}{(6.28)\left(100 \times 10^{3}\right)(3600)} = 442\ pF \Rightarrow \text{Use } 470\ pF$$

Controller design: compensated system response



Final schematic



NOTES:
A. Frequency = 200 kHz
B. Duty cycle = 100% MAX
C. Soft-start timing = 6 ms
D. SCP timing = 75 ms

Test results

Table 6. Example 3: Test Results

PARAMETER	TEST CONDITIONS	MEASUREMENT
Load regulation	$V_I = 5$ V, $I_O = 0 \sim 750$ mA	1.4%
Output ripple (peak-to-peak)	$I_O = 750$ mA	<20 mV
Efficiency	$V_I = 5$ V, $I_O = 750$ mA, Q1 = SI9405	74.4%
	$V_I = 5$ V, $I_O = 750$ mA, Q1 = TPS1101	84.1%†

† The higher efficiency achieved with the TPS1101 is due to lower gate capacitance, which speeds up switching and reduces switching loss.