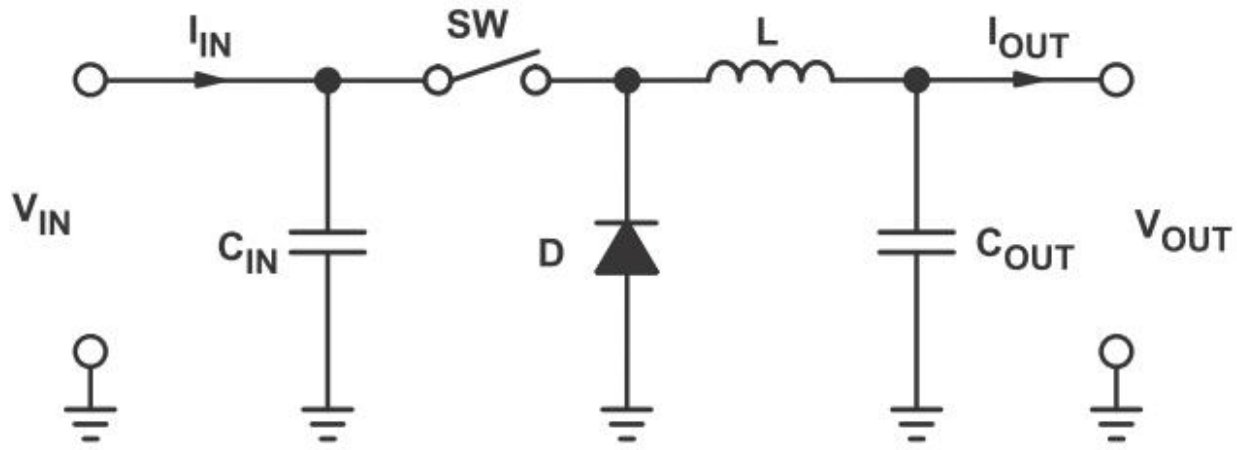
# Basic calculations for buck SMPS design

[TI_slva477b, TI_slva034a, TI_slvaeq9]

# Basic Configuration of a Buck Converter




- The following four parameters are needed to calculate the power stage:
  - Input voltage range: $V_{IN(min)}$ and $V_{IN(max)}$
  - Nominal output voltage: $V_{OUT}$
  - Maximum output current: $I_{OUT(max)}$
  - Integrated circuit used to build the buck converter

# Calculate the Maximum Switch Current

- *Maximum switch current* duty cycle:

$$D_m = \frac{V_{OUT}}{V_{IN(max)} \times \eta}$$

with $\eta$ = efficiency of the converter, e.g., estimated 90%

- Inductor ripple current:

$$\text{Inductor Ripple Current: } \Delta I_L = \frac{\left(V_{IN(max)} - V_{OUT}\right) \times D_m}{f_S \times L}$$

with $D_m$ as above, and $L$ taken from datasheet, or computed (see later)

- Verify that the IC or FET can deliver the maximum switch current

$$I_{SW(max)} = \frac{\Delta I_L}{2} + I_{OUT(max)}$$

# Inductor selection

- Data sheets often give a range of recommended inductor values
  - if this is the case, choose an inductor from this range
  - the higher the inductor value, the higher the maximum output current (because of the reduced ripple current)
  - the lower the inductor value, the smaller the solution size
  - the inductor must always have a higher current rating than the maximum switch current
- Otherwise, using $D=V_{OUT}/V_{IN}$

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{\Delta I_L \times f_S \times V_{IN}}$$

with $V_{IN}$ typical input voltage and $\Delta I_L$ estimated with

$$\Delta I_L = (0.2 \text{ to } 0.4) \times I_{OUT(max)}$$

## Diode selection

- To reduce losses, use Schottky diodes
- Forward current rating: maximum average output current

$$I_F = I_{OUT(max)} \times (1 - D_m)$$

with $D_m$ as above

- Schottky diodes have a much higher peak current rating than average rating -> peak current in the system is not a problem
- Power dissipation of the diode:

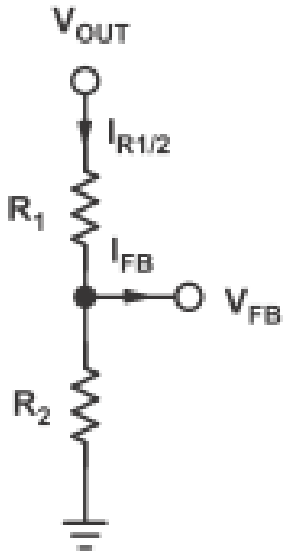
$$P_D = I_F \times V_F$$

# Output Voltage Setting

- Almost all converters set the output voltage with a resistive divider network
  - which is integrated if they are fixed output voltage converters
- Current through the resistive divider needs to be at least 100 times as big as the feedback bias current (from data sheet)
- $R_1$ and $R_2$ must give

$$V_{FB}=R_2/(R_1+R_2)V_{OUT}$$

with $V_{FB}$ from data sheet



# Input Capacitor Selection

- Minimum value for the input capacitor is normally given in the data sheet
  - necessary to stabilize the input voltage due to the peak current requirement of the switching power supply
- Use low-equivalent series resistance (ESR) ceramic capacitors
- The value can be increased if the input voltage is noisy

## Output Capacitor Selection

- Use low-ESR capacitors to minimize the ripple on the output voltage
- *Externally compensated converters*:
  - any capacitor value above the recommended minimum in the data sheet can be used, but
  - the compensation has to be adjusted for the used output capacitance.
- *Internally compensated converters*:
  - the recommended inductor and capacitor values must be used, or
  - the recommendations in the data sheet for adjusting the output capacitors to the application in the data sheet must be followed for the ratio of L × C

# Output Capacitor Selection: external compensation

- The following equations can be used to adjust the output capacitor values for a desired output voltage ripple

$$C_{OUT(min)} = \frac{\Delta I_L}{8 \times f_S \times \Delta V_{OUT}}$$

$C_{OUT(min)}$ = minimum output capacitance
$\Delta I_L$ = estimated inductor ripple current
$f_S$ = minimum switching frequency of the converter
$\Delta V_{OUT}$ = desired output voltage ripple

- The ESR of the output capacitor adds some more ripple:

$$\Delta V_{OUT(ESR)} = ESR \times \Delta I_L$$

# Output Capacitor Selection: external compensation

- Often the selection of the output capacitor is not driven by the steady-state ripple, but by the output transient response
  - the necessary output capacitance for a desired maximum overshoot can be calculated with

$$C_{OUT(min),OS} = \frac{\Delta I_{OUT}^{2} \times L}{2 \times V_{OUT} \times V_{OS}}$$

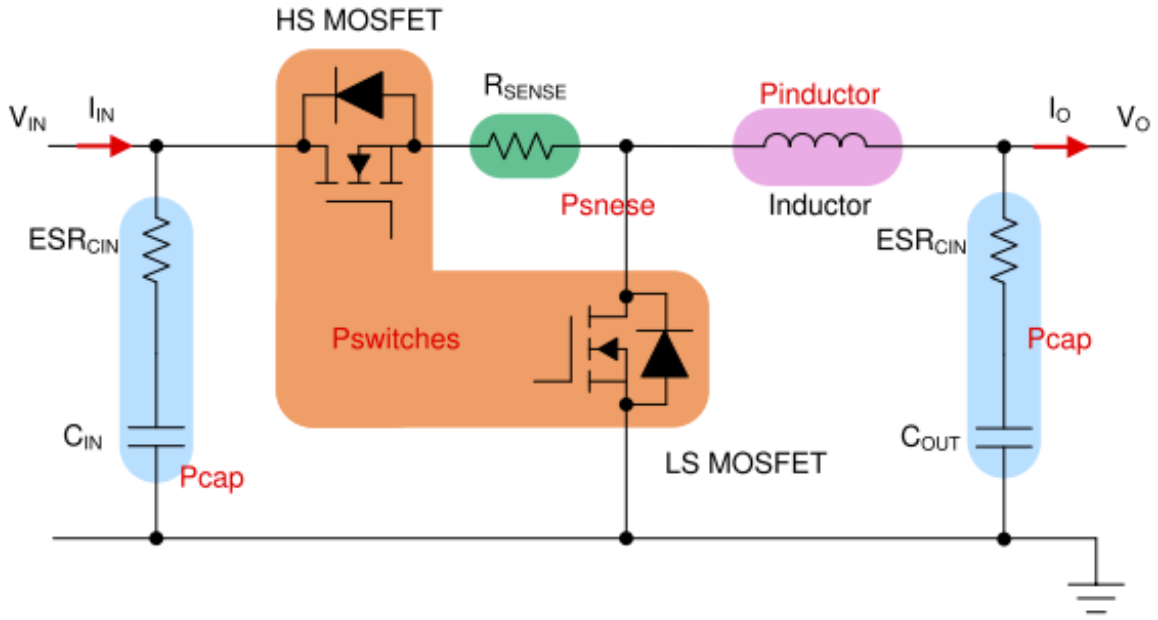
$C_{OUT(min),OS}$ = minimum output capacitance for a desired overshoot
$\Delta I_{OUT}$ = maximum output current change in the application
$V_{OUT}$ = desired output voltage
$V_{OS}$ = desired output voltage change due to the overshoot

# Power dissipation and efficiency

- There are several sources of loss

$$P_{total\_loss} = P_{switches} + P_{inductor} + P_{capacitors} + P_{other}$$

$$\eta = \frac{V_o I_o}{V_o I_o + P_{total\_loss}} \times 100\%$$



# Power dissipation and efficiency

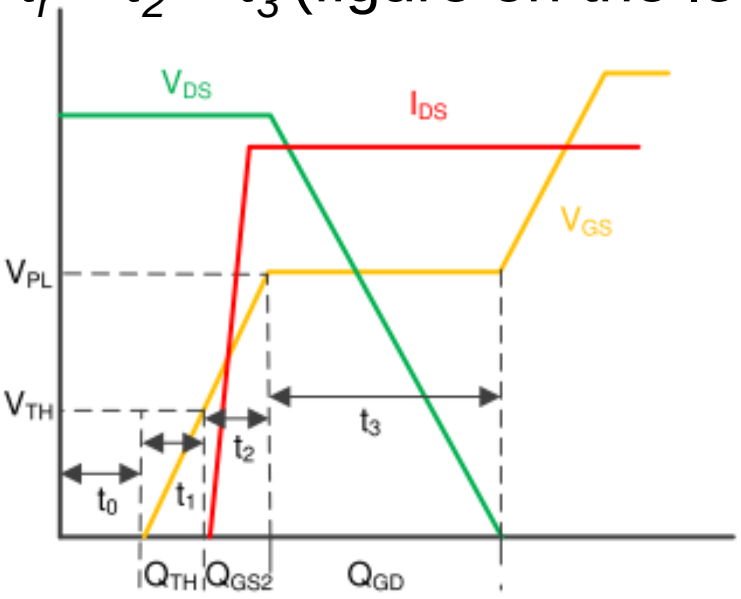
*Switch losses*

- During $t_2$ and $t_3$, $I_{DS}$ and $V_{DS}$ are not zero, so the switching loss is caused when MOSFET turns on and turns off

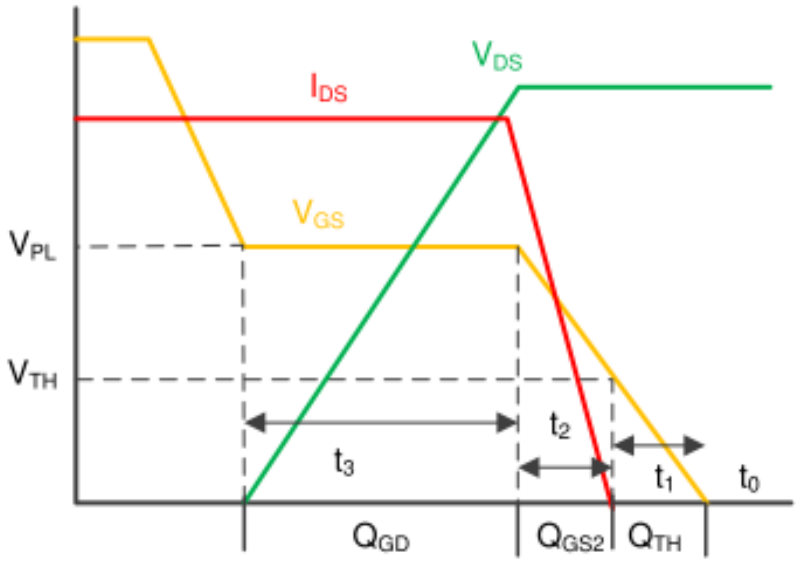
$$P_D = 0.5 \times V_I \times I_O \times t_{r+f} \times f_s$$

with $t_{r+f} = t_r + t_f$ = total (turn-on and turn-off) FET switching time

with $t_r = t_2 + t_3$ (figure on the left), $t_f = t_3 + t_2$ (figure on the right)




MOSFETs Turn on



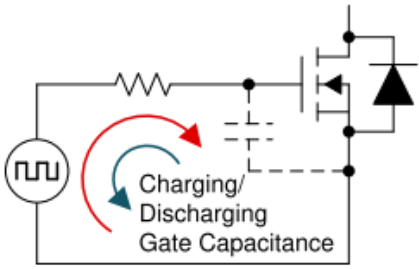

MOSFETs Turn off

# Power dissipation and efficiency

- Power dissipation, which includes both conduction and switching losses, can be approximated with

$$P_D = I_O^2 \times r_{DS(on)} \times D + 0.5 \times V_I \times I_O \times t_{r+f} \times f_s$$

- More precise calculations, which include
  - switching losses
  - conduction losses (due to $r_{DS(on)}$)
  - gate drive losses
  - FET output capacitance losses (charge and discharge)
  - inductor losses (due to ESR and core material)
  - input and output capacitors losses (due to ESRs)
  - sense resistor losses




can be found in *TI_slvaeq9*

## SW tools

Some (often proprietary) tools do exist to help in the design:

- Linear Technology LTpowerCAD
  - free download at www.linear.com/LTpowerCAD
  - ready for LTspice simulation
- STM eDesignSuite
  - https://eds.st.com/console/#/app/dcdc/ic_dcdc_catalogs/filter/%5B%5D/grid