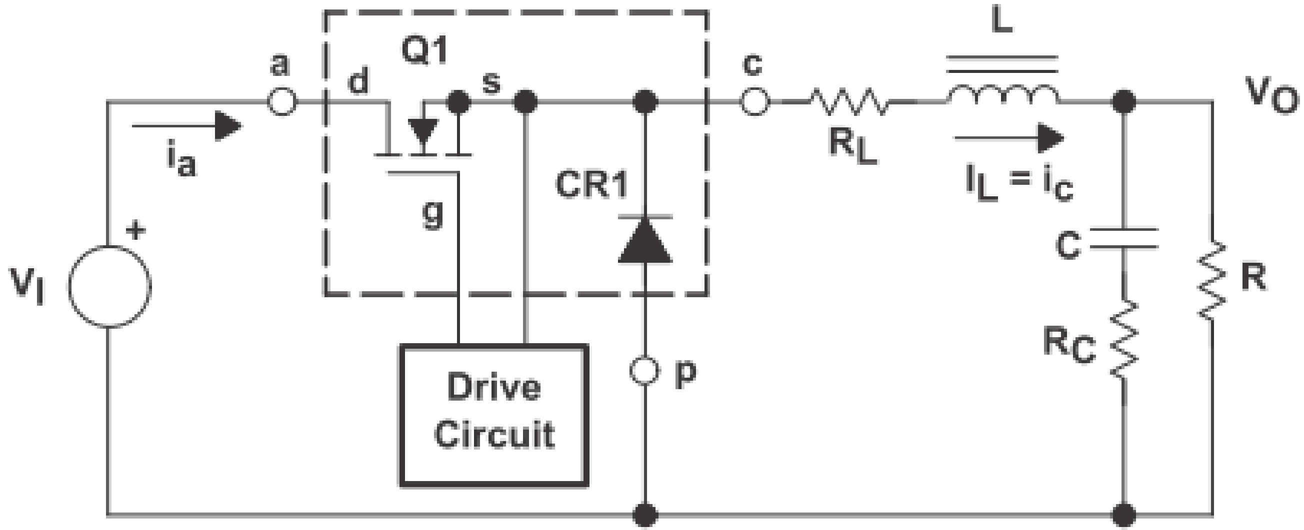
Buck SMPS fundamentals

[TI_slva057]

Introduction

- Simplified schematic of the buck power stage with a drive circuit block included. The power switch, *Q1*, here is an n-channel MOSFET.



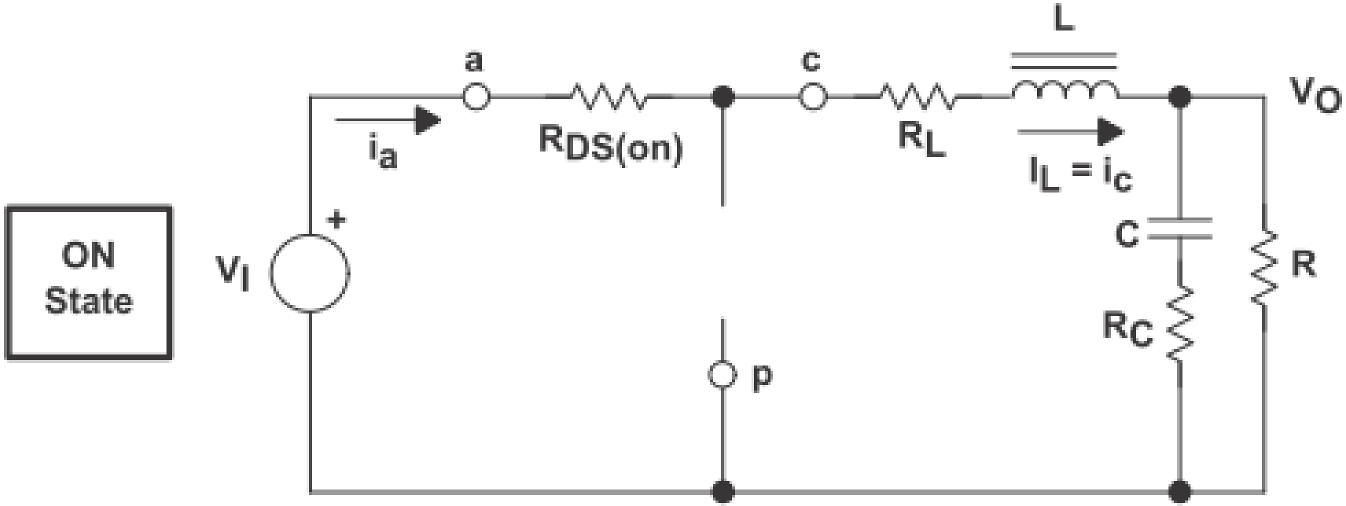
- The diode, CR1, is usually called *catch diode*, or *freewheeling* diode
- The inductor, *L*, and capacitor, *C*, make up the output filter
- The capacitor ESR, R_C, (equivalent series resistance) and the inductor DC resistance, R_L, are included in the analysis

Buck Steady-State Mode Analysis

- A power stage can operate in continuous (CCM) or discontinuous (DCM) inductor current mode (see later)
  - continuous inductor current mode is characterized by current flowing continuously in the inductor
  - discontinuous inductor current mode is characterized by the inductor current being zero for a portion of the switching cycle
- Here, an n-channel power MOSFET is used
  - the advantage of using an n-channel FET is its lower $R_{DS(on)}$ but the drive circuit is more complicated because a floating drive is required
  - for the same die size, a p-channel FET has a higher $R_{DS(on)}$ but usually does not require a floating drive circuit
- Steady-state implies that the input voltage, output voltage, output load current, and duty-cycle are fixed and not varying

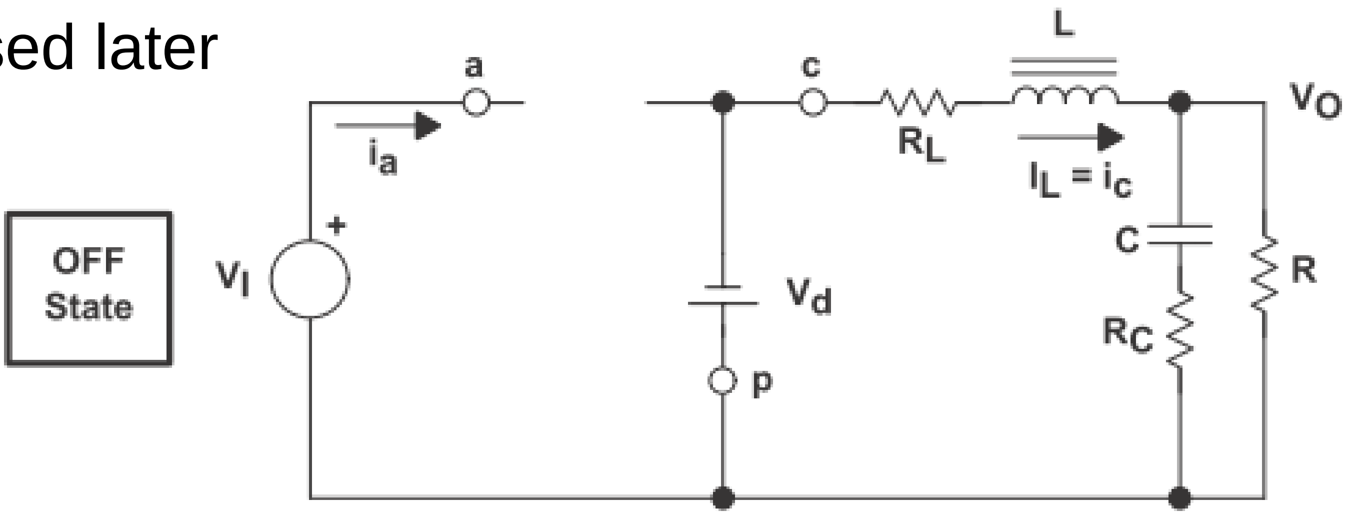
Buck Steady-State CCM Analysis

- In CCM, the Buck power stage assumes two states per switching cycle



Note the
- active (a),
- passive (p), and
- common (c)

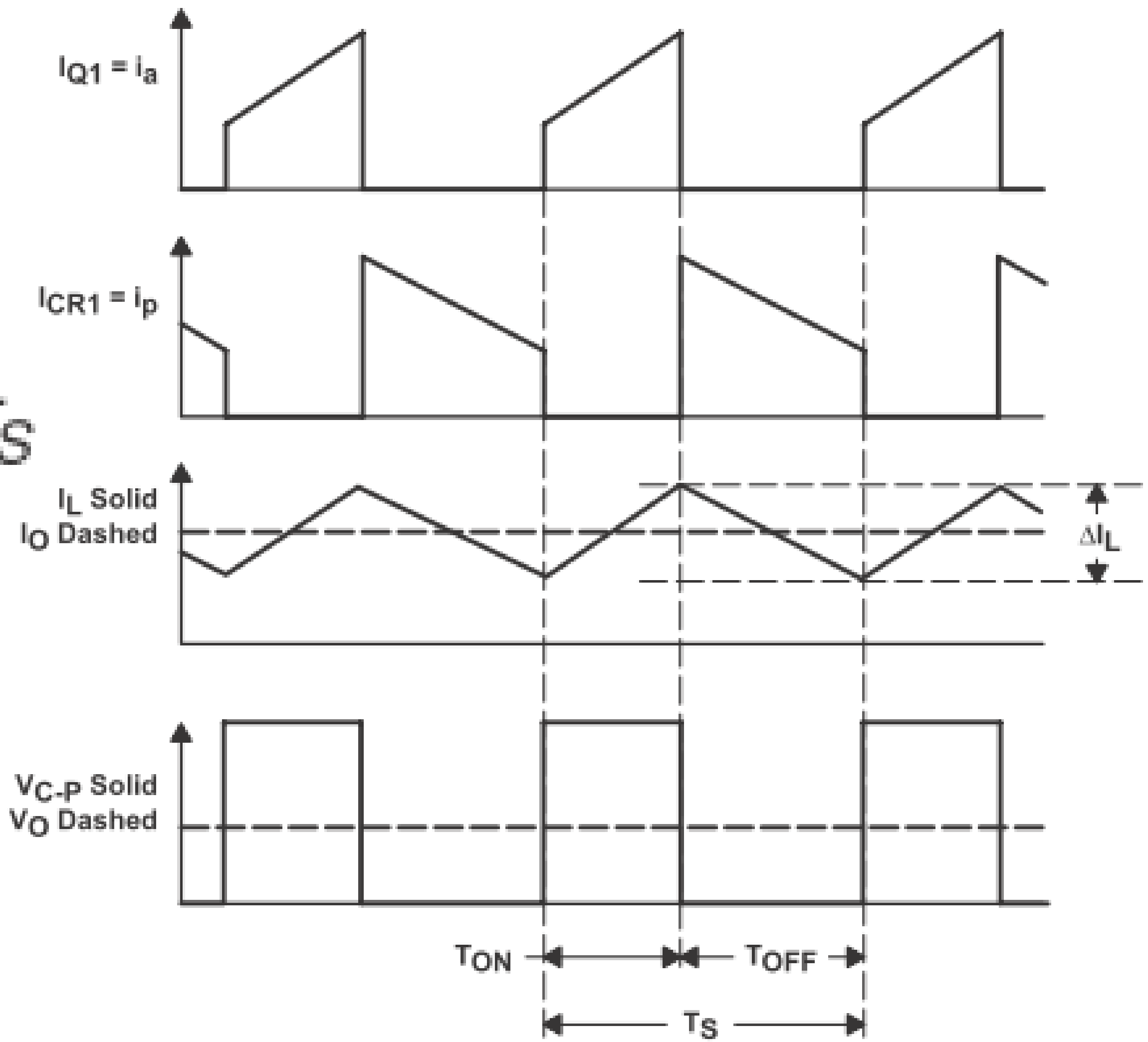
nodes: they'll be used later



Buck Steady-State CCM Analysis

- Waveforms in CCM

$$D = T_{ON}/T_S$$



Buck Steady-State CCM Analysis

- During ON state, Q1 presents a low resistance $R_{DS(on)}$ and has a small voltage drop of

$$V_{DS} = I_L \times R_{DS(on)}$$

- There is also a small voltage drop across the dc resistance of the inductor equal to

$$I_L \times R_L$$

- During ON state, the voltage applied to the left side of the inductor is constant and equal to

$$V_I - V_{DS} - I_L \times R_L$$

while the right side is at V_O

- Since the applied voltage is essentially constant, the inductor current increases linearly
- and the inductor current ripple is

$$\Delta I_L(+) = \frac{\left(V_I - V_{DS} - I_L \times R_L\right) - V_O}{L} \times T_{ON}$$

Buck Steady-State CCM Analysis

- During OFF state, the voltage on the left-hand side of L becomes

$$-(V_d + I_L \times R_L)$$

where V_d is the forward voltage drop of CR1, while the right side is at V_O

- Since the applied voltage is essentially constant, the inductor current decreases linearly
- and the inductor current ripple is

$$\Delta I_L(-) = \frac{V_O + \left(V_d + I_L \times R_L\right)}{L} \times T_{OFF}$$

- In steady state conditions, current increase during ON time and current decrease during OFF time must be equal ->

$$V_O = \left(V_I - V_{DS}\right) \times D - V_d \times (1-D) - I_L \times R_L$$

Buck Steady-State CCM Analysis

- From

$$V_O = \left(V_I - V_{DS}\right) \times D - V_d \times (1 - D) - I_L \times R_L$$

- if we neglect V_{DS} V_d *,and* R_L we of course get our “old” result

$$V_O = D\ V_I$$

  - the voltage conversion relationship is a function of input voltage and duty cycle only
  - things will be different in DCM mode (see later)

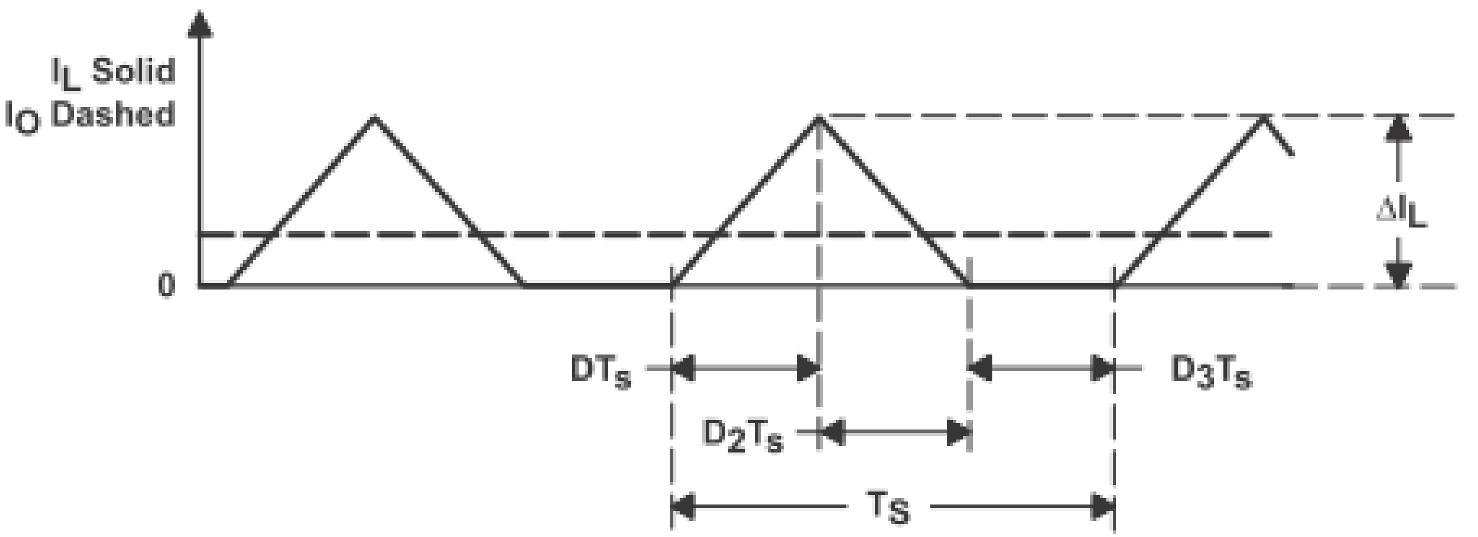
Buck Steady-State CCM Analysis

- Note: the DC output voltage was implicitly assumed to be constant with no AC ripple voltage during ON time and OFF times
  - the output capacitor is assumed to be large enough that its voltage change is negligible
  - the voltage across the capacitor ESR is also assumed to be negligible
- These assumptions are valid because the AC ripple voltage is designed to be much less than the DC part of the output voltage.

- *Of course, the inductor current averaged over the switching cycle is equal to the output current*
  - because the average current in the output capacitor must be zero

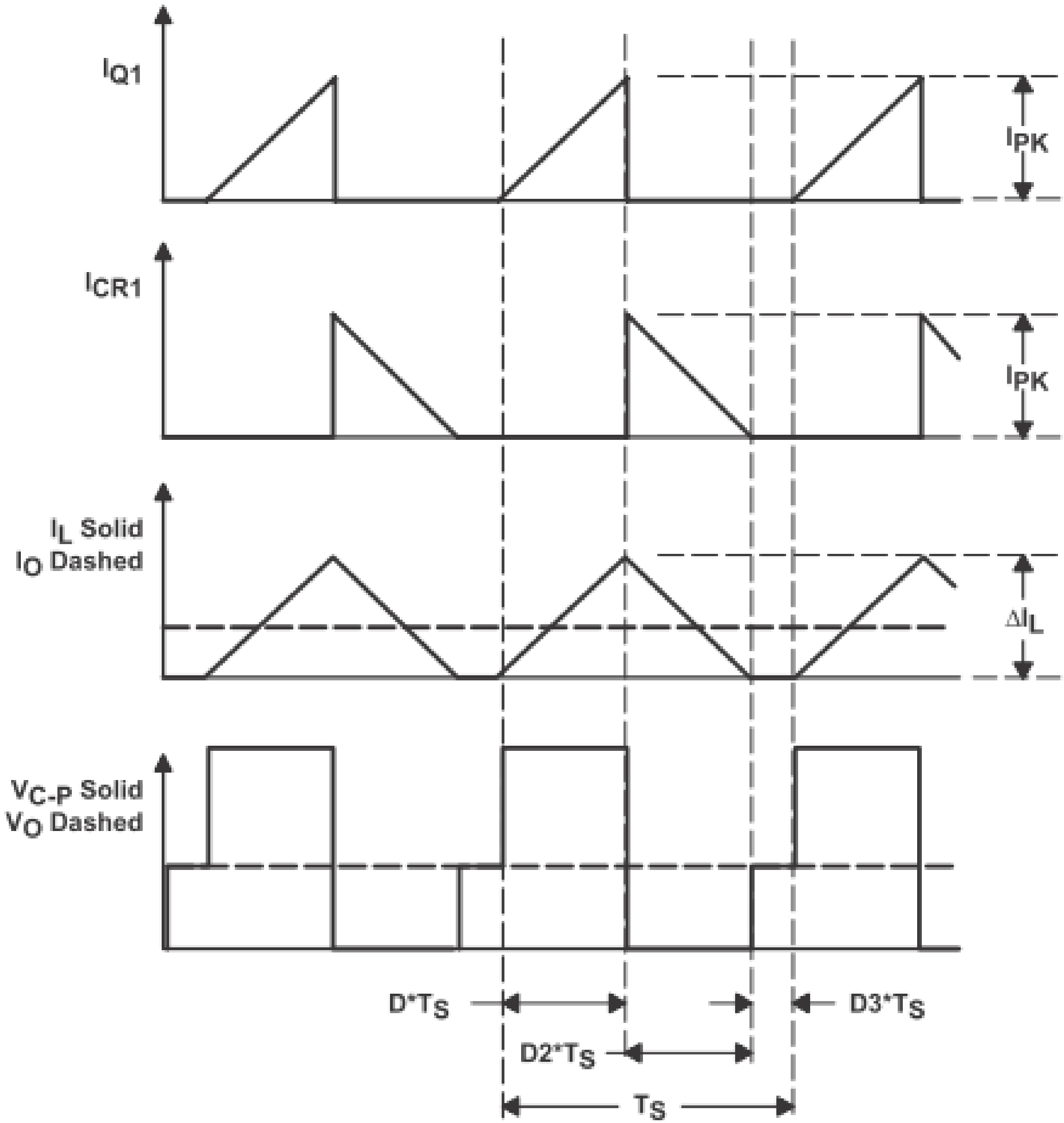
Buck Steady-State DCM Analysis

- If the output load current is reduced below the critical current level, the inductor current will be zero for a portion of the switching cycle
  - in CCM, the peak to peak amplitude of the ripple current does not change with output load current
  - if the inductor current attempts to fall below zero, it just stops at zero because of the diode
- A power stage operating in DCM has three unique states during each switching cycle (ON, OFF and IDLE ($D_3 T_S$))



Buck Steady-State DCM Analysis

- Waveforms:



Buck Steady-State DCM Analysis

- In the following, the DC resistance of the output inductor, the output diode forward voltage drop, and the power MOSFET ON-state voltage drop are all assumed to be small enough to omit
- $T_{ON}=DT_S$, $T_{OFF}=D_2T_S$, $T_{IDLE}=D_3T_S$
- Similarly to the CCM mode, we find that

$$\Delta I_L(+) = \frac{V_I - V_O}{L} \times T_{ON} = \frac{V_I - V_O}{L} \times D \times T_S = I_{PK}$$

which is also the peak inductor current, I_{PK}, because in DCM the current starts at zero each cycle

$$\Delta I_L(-) = \frac{V_O}{L} \times T_{OFF}$$

Again, these must be equal and we get

$$V_O = V_I \times \frac{T_{ON}}{T_{ON} + T_{OFF}} = V_I \times \frac{D}{D + D2}$$

Buck Steady-State DCM Analysis

- The output current is the average of the inductor current

$$I_O = I_{L(avg)} = \frac{V_O}{R} = \frac{I_{PK}}{2} \times \frac{D \times T_S + D2 \times T_S}{Ts}$$

and by substituting I_{PK} from the previous slide we get

$$I_O = \frac{V_O}{R} = \left(V_I - V_O\right) \times \frac{D \times T_S}{2 \times L} \times (D + D2)$$

- Putting together the equations of V_O and I_O we get

$$V_O = V_I \times \frac{2}{1 + \sqrt{1 + \frac{4 \times K}{D^2}}} \qquad K = \frac{2 \times L}{R \times T_S}$$

  - the voltage conversion relationship is a function of input voltage, duty cycle, *power stage inductance, switching frequency and output load resistance*

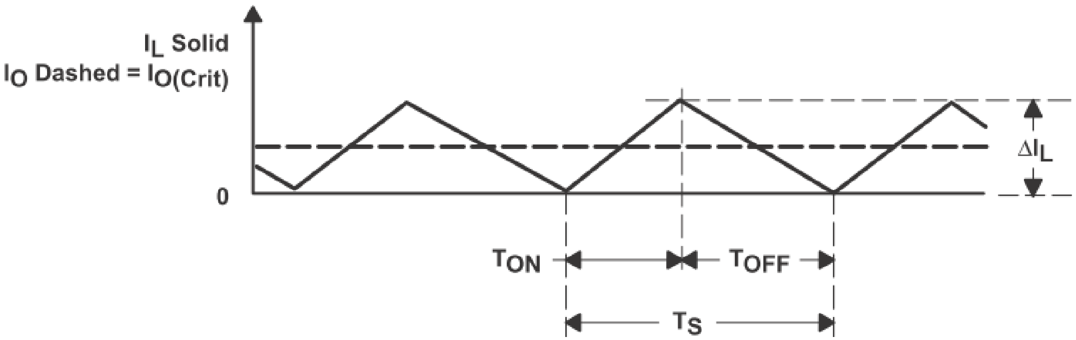
CCM and DCM

- Buck power stage are rarely operated in DCM in normal situations,
  - but DCM will occur anytime the load current is below the critical level
- A buck power stage can be designed to operate in CCM for load currents above a certain level
  - usually 5% to 10% of full load

Inductor

- Assume the input voltage range, the output voltage and load current are defined; let's compute the minimum inductor
- Minimum current to maintain CCM, so called *critical current*, is

$$I_{O(crit)} = \frac{\Delta I_L}{2}$$



- Using e.g. $\Delta I_L(-)$, with the maximum input voltage (because this gives the maximum ΔI_L), we get

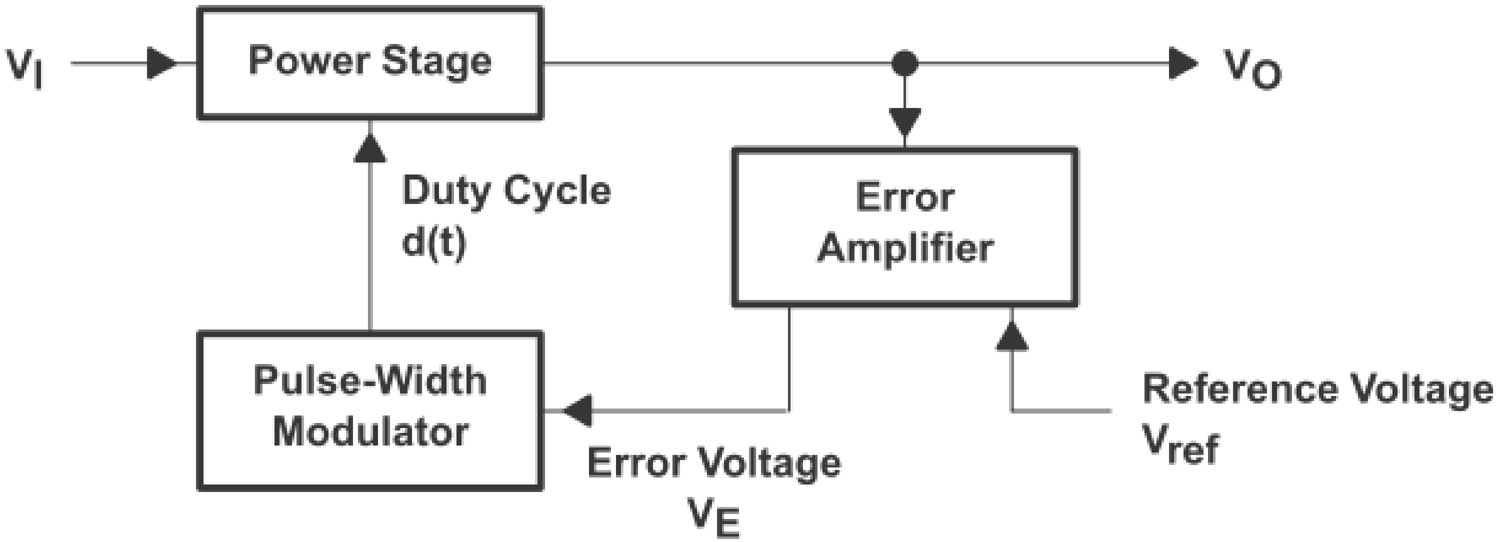
$$L_{min} \geq \frac{1}{2} \times \left(V_O + V_d + I_L \times R_L\right) \times \frac{T_{OFF(max)}}{I_{O(crit)}}$$

or equivalently, from $\Delta I_L(+)$

$$L_{min} \geq \frac{V_O \times \left(1 - \frac{V_O}{V_{I(max)}}\right) \times T_S}{2 \times I_{O(crit)}}$$

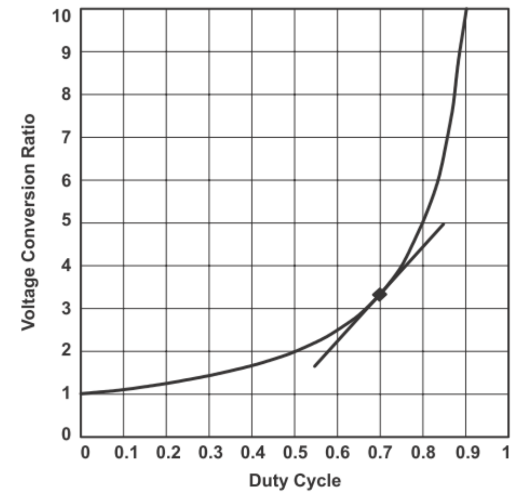
Buck Power Stage Small Signal Modeling

- Three major components of the power supply control loop (i.e., the power stage, the pulse width modulator and the error amplifier):



Power stage modeling: "PWM switch model"

- Buck power stage has an essentially linear voltage conversion ratio versus duty cycle
- but other power stages have a *nonlinear* voltage conversion ratio versus duty cycle
  - e.g., for a boost:



- We want a linear model
- The only nonlinear components in a power stage are the switching devices
- *a linear model of the nonlinear components can be derived by averaging their voltages and currents over one switching cycle.*
- *the model is then substituted into the original circuit for analysis of the complete power stage*

CCM PWM switch model

- By averaging

$$i_a(t) = \begin{cases} i_c(t) & during\ d \times T_S \\ 0 & during\ d' \times T_S \end{cases}$$

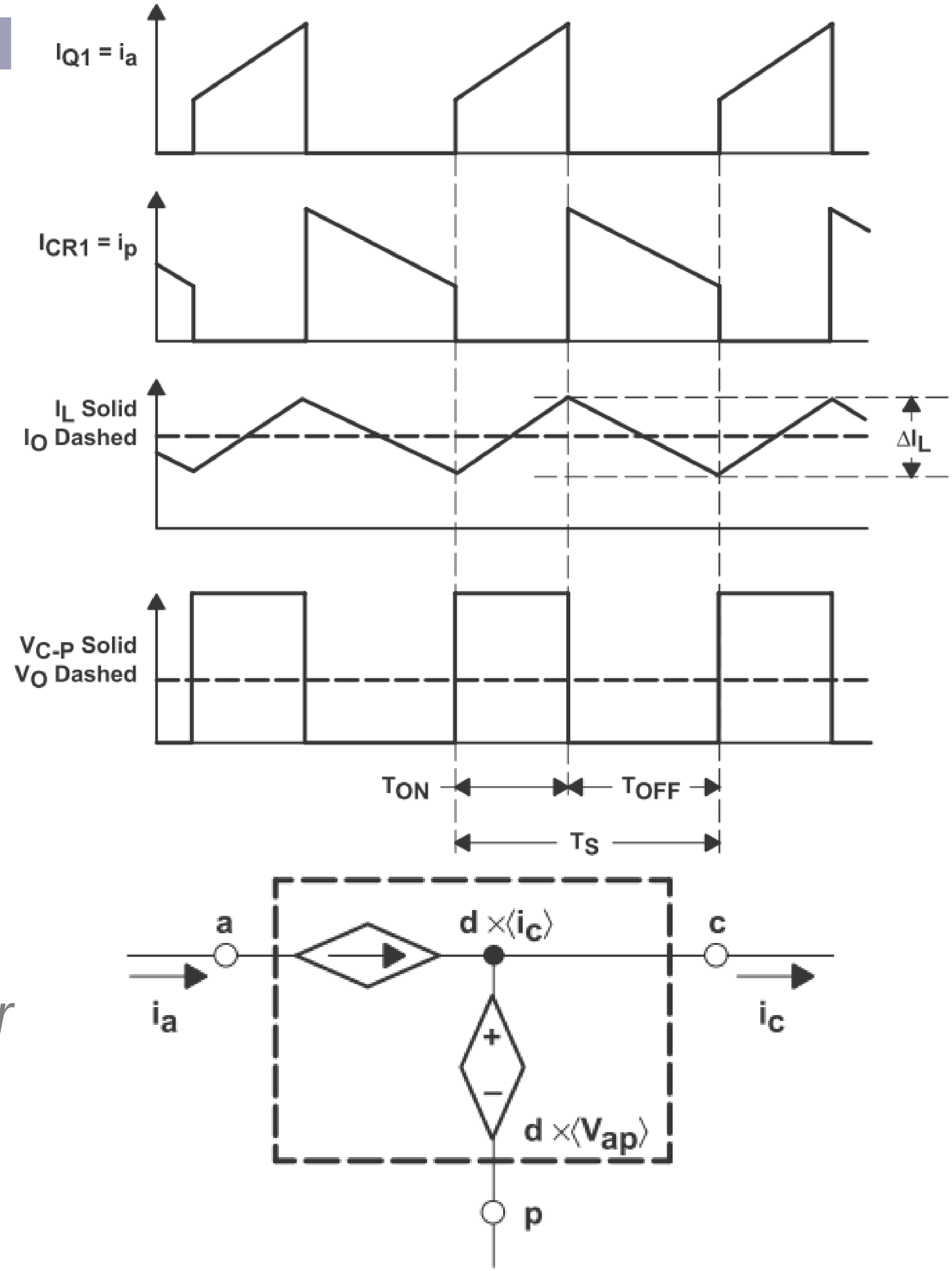
$$v_{cp}(t) = \begin{cases} v_{ap}(t) & during\ d \times T_S \\ 0 & during\ d' \times T_S \end{cases}$$

we get

$$\langle i_a \rangle = d \times \langle i_c \rangle$$

$$\langle v_{cp} \rangle = d \times \langle v_{ap} \rangle$$

and the *large signal nonlinear model* is



CCM PWM switch model

- We now perform perturbation and linearization around the operating point *d=D*:

$$d(t) = D + \hat{d}(t)$$

$$I_a + \hat{i}_a = \left(D + \hat{d}\right) \times \left(I_c + \hat{i}_c\right) = D \times I_c + D \times \hat{i}_c + \hat{d} \times I_c + \hat{d} \times \hat{i}_c$$

$$V_{cp} + \hat{v}_{cp} = \left(D + \hat{d}\right) \times \left(V_{ap} + \hat{v}_{ap}\right) = D \times V_{ap} + D \times \hat{v}_{ap} + \hat{d} \times V_{ap} + \hat{d} \times \hat{v}_{ap}$$

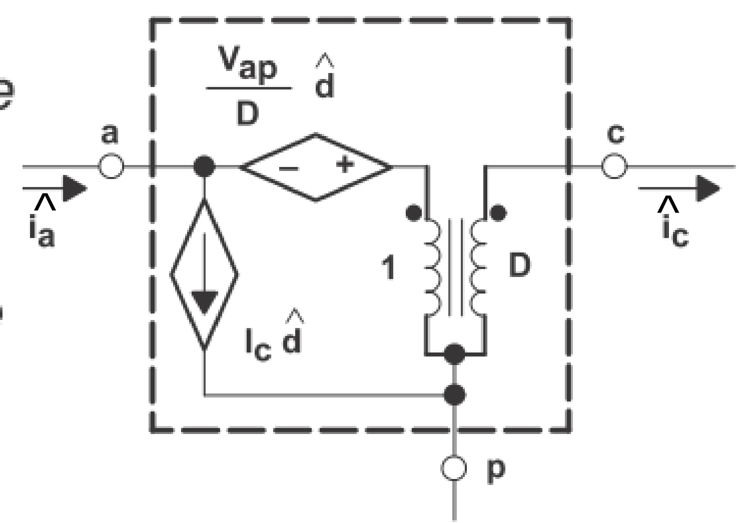
- we separate steady-state quantities from AC quantities and also drop products of AC quantities

$$I_a = D \times I_c \qquad \textit{Steady-state}$$

$$\hat{i}_a = D \times \hat{i}_c + \hat{d} \times I_c \qquad \textit{AC}$$

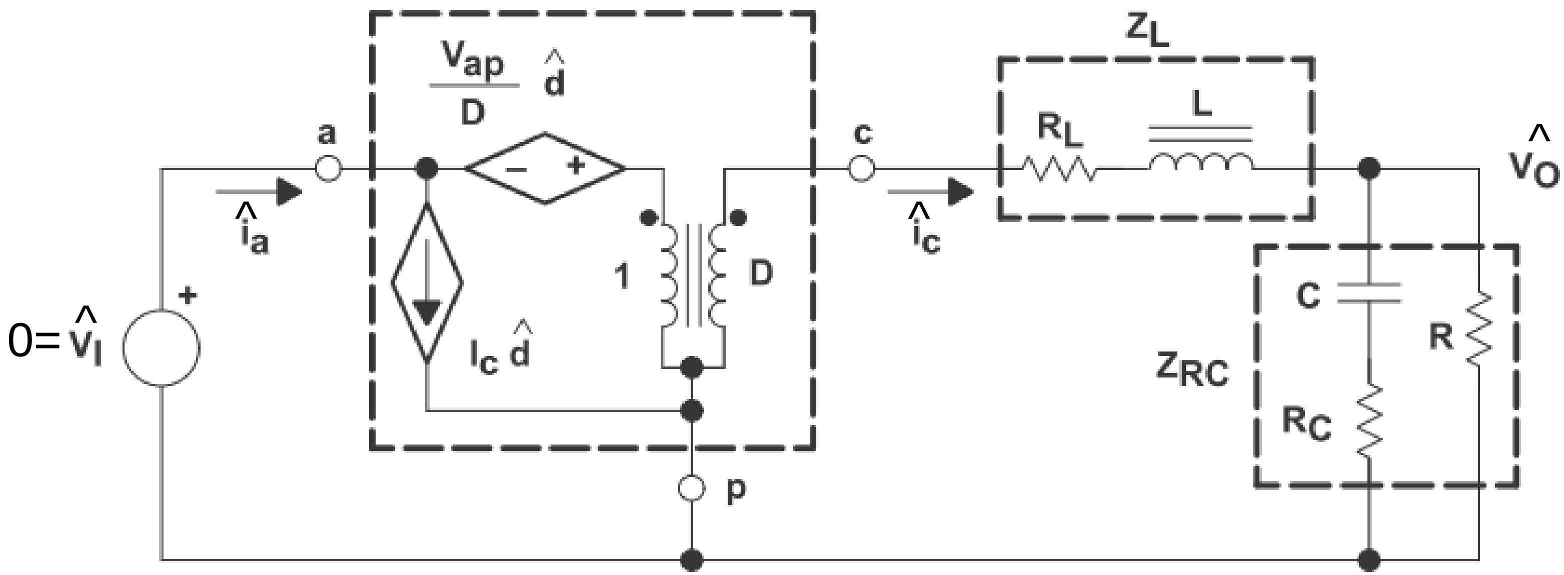
$$V_{cp} = D \times V_{ap} \qquad \textit{Steady-state}$$

$$\hat{v}_{cp} = D \times \hat{v}_{ap} + \hat{d} \times V_{ap} \qquad \textit{AC}$$



CCM PWM switch model

- And adding L and C



- For a DC analysis, $\hat{d}=0$ and $V_I D=V_O$
- For AC analysis, we can compute
  - open-loop line-to-output transfer function
  - open-loop output impedance, and
  - open-loop control-to-output, or *duty-cycle-to-output*, transfer function

CCM: duty-cycle-to-output transfer function

- V_I: for the DC analysis

$$V_I = V_{ap}$$

- while in AC it is zero because we only want the ac component of the transfer function from d to V_O. For the left loop

$$-\frac{V_{ap}}{D} \times \hat{d} + \frac{\hat{v}_{cp}}{D} = 0 \Rightarrow \hat{v}_{cp} = V_{ap} \times \hat{d} \Rightarrow \hat{v}_{cp} = V_I \times \hat{d}$$

- From v_{cp} to v_o we have
- and we get

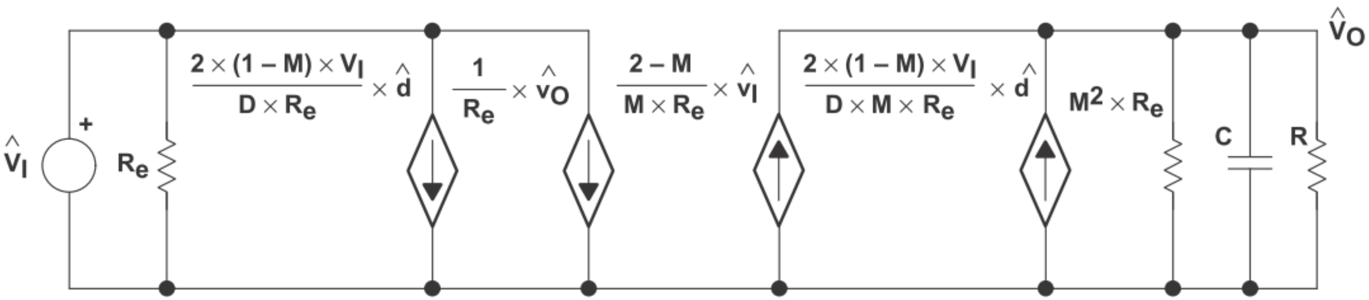
$$\frac{\hat{v}_O}{\hat{v}_{cp}} = \frac{Z_{RC}(s)}{Z_{RC}(s) + Z_L(s)}$$

$$\frac{\hat{v}_O}{\hat{d}}(s) = \frac{\hat{v}_{cp}}{\hat{d}}(s) \times \frac{\hat{v}_O}{\hat{v}_{cp}}(s) = V_I \times \frac{R}{R + R_L}$$

$$\times \frac{1 + R_c \times C}{1 + s \times \left[C \times \left(R_c + \frac{R \times R_L}{R + R_L} \right) + \frac{L}{R + R_L} \right] + s^2 \times L \times C \times \frac{R + R_C}{R + R_L}}$$

DCM: duty-cycle-to-output transfer function

- For DCM, this model may be found



- and the duty-cycle-to-output transfer function is

$$\frac{\hat{v}_O}{\hat{d}} = G_{do} \times \frac{1}{1 + \frac{s}{\omega_p}}$$

with

$$G_{do} = \frac{2 \times V_O}{D} \times \frac{1 - M}{2 - M}$$

$$D = M \times \sqrt{\frac{K}{1 - M}}$$

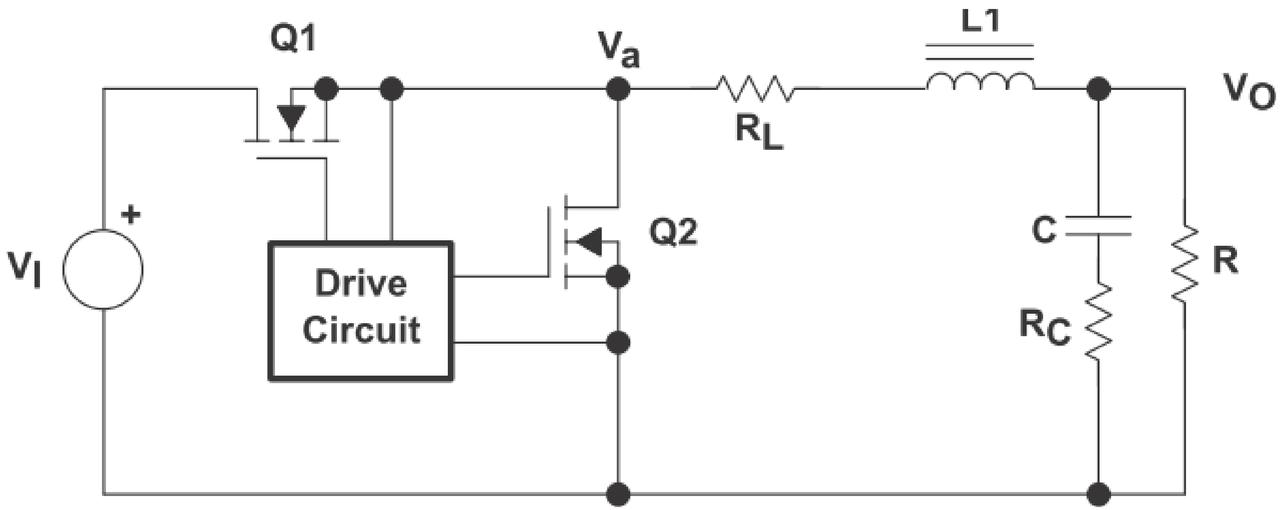
$$M = \frac{V_O}{V_I}$$

$$K = \frac{2 \times L}{R \times T_s}$$

$$\omega_p = \frac{2 - M}{1 - M} \times \frac{1}{R \times C}$$

Synchronous Buck Power Stage

- The buck converters seen up to now are *non-synchronous*
- In *synchronous* converters, an active switch such as another power MOSFET, Q2 in this example, replaces the diode
  - this FET is then selected so that its ON-voltage drop is less than the forward drop of the diode
- either the drive circuit or the controller must insure that both FETs are not on simultaneously
  - a small amount of deadtime is necessary
- it always operates in CCM because current can reverse in Q2



Buck Power Stages: other categories

- Buck switching solutions include
  - *power modules*: integrated FETs and inductor
  - *converters (regulators)*: integrated FET or FETs and external inductor
  - *controllers*: external FETs and inductors
- The compensation of the control loop may be
  - *internal*
  - *external*