

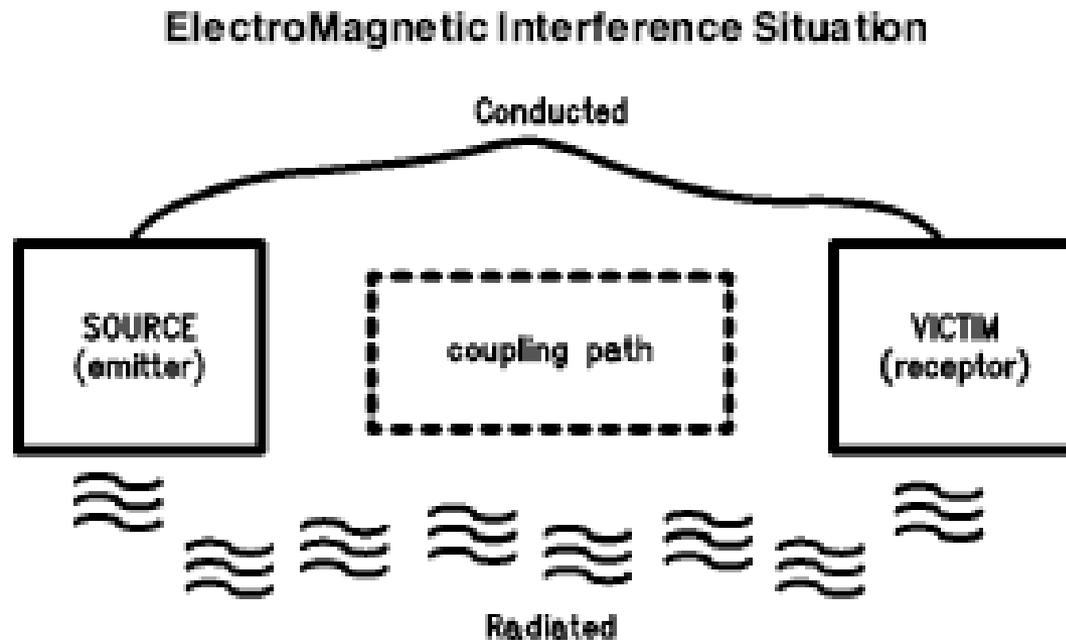


# EMI/RFI board design

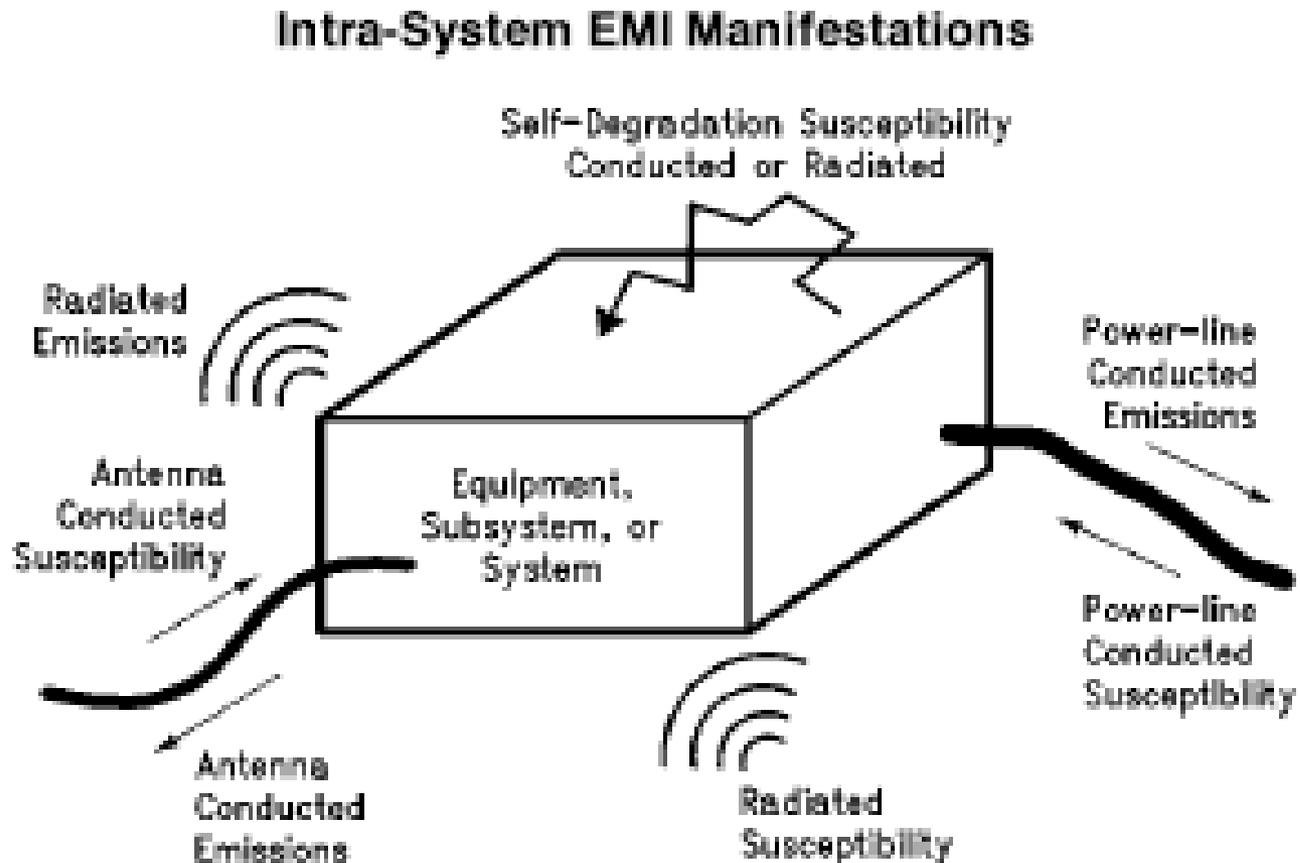
[AN-643]

## Definitions

- EMI: electromagnetic interference
- RFI: radio frequency interference
- EMC: electromagnetic compatibility
- Three categories: *source, coupling path, victim*
- Two connections: *conducted, radiated*



- Inter- ed intra-system interference
- Emissions and susceptibility



## *US FCC regulations:*

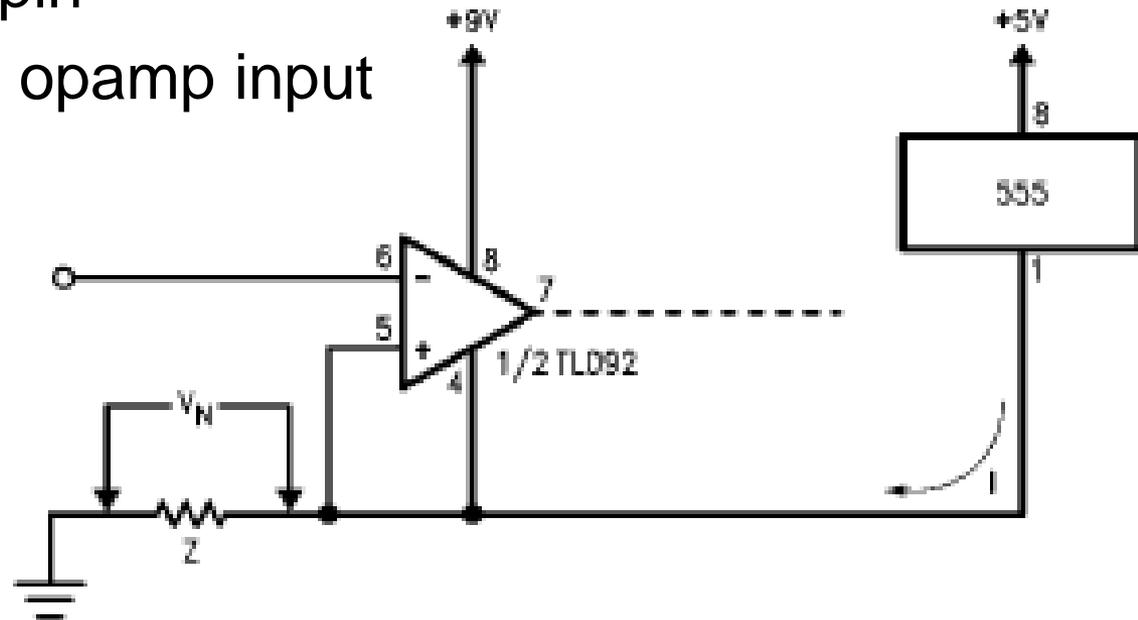
- *radiated emission:* e.g., radiated emission from a PC (class B computing device pursuant to subpart J of part 15 of FCC rules): max

frequency (MHz)	distance (m)	field strength ( $\mu\text{V}/\text{m}$ )
30-88	3	100
88-216	3	150
216-1000	3	200
- *interference fed back onto the power line:* max 250  $\mu\text{V}$  in the 450 kHz - 30 MHz range

## *European regulations*

- EN55022: limits on the noise generated
  - conducted noise (150 kHz – 30 MHz)
  - radiated noise (30 MHz – 1 GHz)
- EN55024: noise immunity

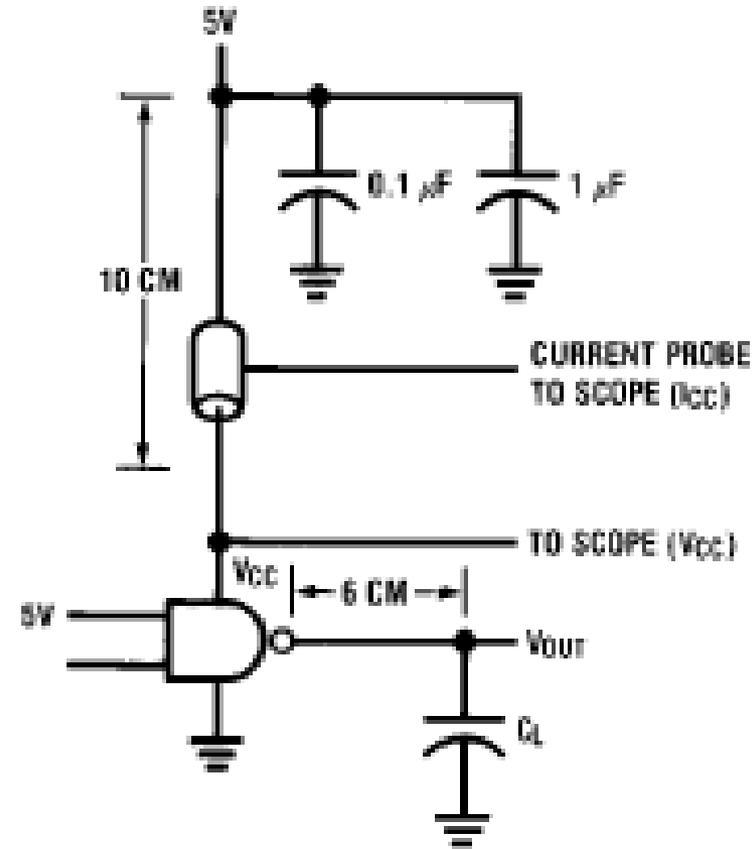
- Common-mode coupling occurs when two circuits share a common bus or wire.
  - here, a voltage  $V_N$  (due to the current from the 555 flowing in  $Z$ ) appears
  - at the opamp  $V_{CC}$ -pin
  - much worse, at the opamp input



(TL092 opamp can work with single supply, and input common mode includes  $V_{CC}$ -)

## Power supply noise

- When any element switches logic states, it generates a current spike that produces a voltage transient.
- Current spikes increase if lines are loaded
- Mostly due to output circuits



## Noise immunity

- describes the device's ability to prevent noise on its input from being transferred to its output
- is the difference between the worst case output levels ( $V_{OH}$  and  $V_{OL}$ ) of the driving circuit and the worst case input voltage requirements ( $V_{IH}$  and  $V_{IL}$ , respectively) of the receiving circuit

E.g. (TTL LS or ALS devices): the worst case noise immunity

- $2.7 - 2.0 \text{ V} = 700 \text{ mV}$  for the high logic level
- $0.8 - 0.5 \text{ V} = 300 \text{ mV}$  for the low logic level

### Logic Family Comparisons

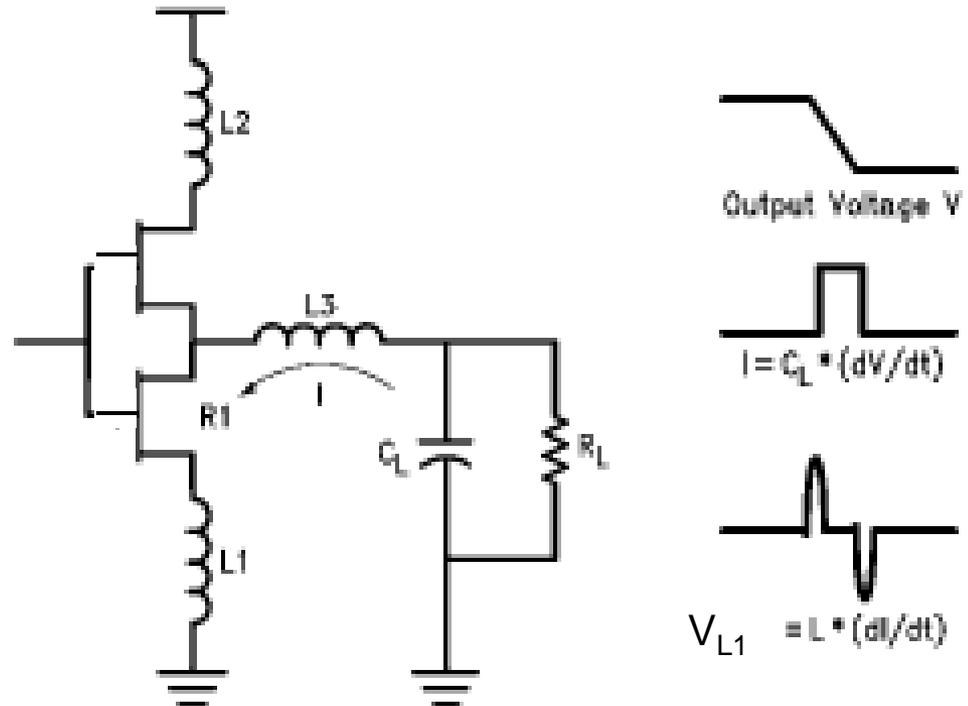
Characteristic	Symbol	LS/ALS TTL	HCMOS	AC	ACT
Input Voltage (Limits)	$V_{IH}$ (Min)	2.0V	3.15V	3.15V	2.0V
	$V_{IL}$ (Max)	0.8V	0.9V	1.35V	0.8V
Output Voltage (Limits)	$V_{OH}$ (Min)	2.7V	$V_{CC} - 0.1$	$V_{CC} - 0.1$	$V_{CC} - 0.1$
	$V_{OL}$ (Max)	0.5V	0.1V	0.1V	0.1V

# Ground bounce

It is the result of the intrinsic characteristics of the leadframes and bondwires of the packages

- edge rates and drive capability increase in the new logic families -> these effects increase
- one of these parasitics: the inductance found in all leadframe materials
- e.g.:

$$V_{L1} = L_1 (di/dt)$$



# Shields

A box's shielding effectiveness in decibels depends on three main factors:

- its skin
- the control of radiation leakage through the box's apertures or open areas (e.g. cooling holes) and
- the use of filters or shields at entry or exit spots of cables

## Shielding: skin

- A box skin is typically fabricated from sheet metal or metallized plastic
- Normally sheet metal skin that is 1 mm thick is more than adequate
  - shielding effectiveness  $> 100$  dB at 1 MHz to 20 GHz
- Alternatively:
  - conductive coatings on plastic boxes
  - plastic filled materials or composites having either conductive powder, flakes, or filaments
  - very different performances!

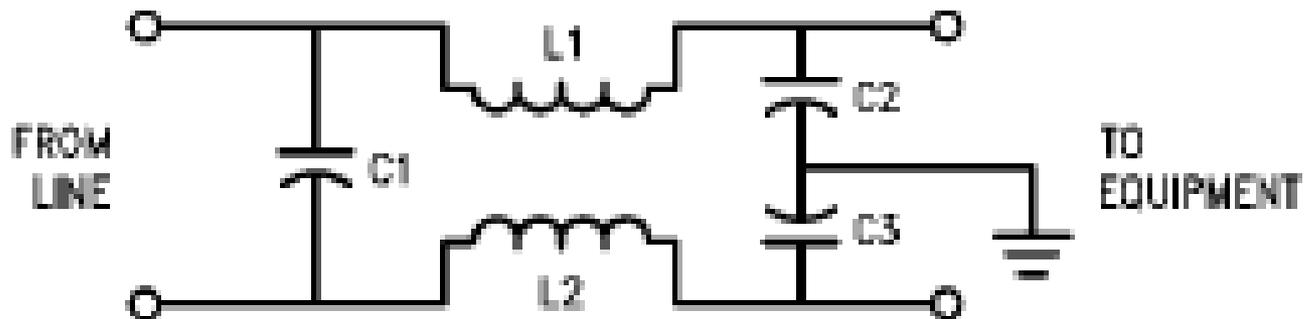
# Shielding

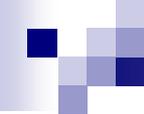
- In many cases shielding effectiveness of at least 40 dB (it's easy!) is required for plastic housings for microcontroller-based equipment to meet FCC (United States) or VDE (Europe) regulations
- The problem is aperture leakage
  - the larger the aperture, the greater its radiation leakage
  - multiple small holes matching the same area as the single large aperture can attain the same amount of cooling with little or no loss of attenuation properties

# Filtering

Example of AC filter on power lines (230 VAC):

- C1 shunts any high-frequency differential mode signals
- C2 and C3 shunt any common mode signal to ground
- L1 and L2, *common mode chokes*, impede any HF common mode currents





## Inter-System EMI Control Techniques

Many EMI control actions may be carried out to enhance the chances of inter-system EMC.

They can be grouped into four categories

- frequency management
- time management
- location management
- direction management

# EMC: design guidelines

- Logic selection
  - use the *slowest* speed logic that will do the job
- Component layout
  - isolate I/O from high speed logic
  - Isolate analog and low speed digital lines from high speed logic
  - put I/O circuitry close to the connectors

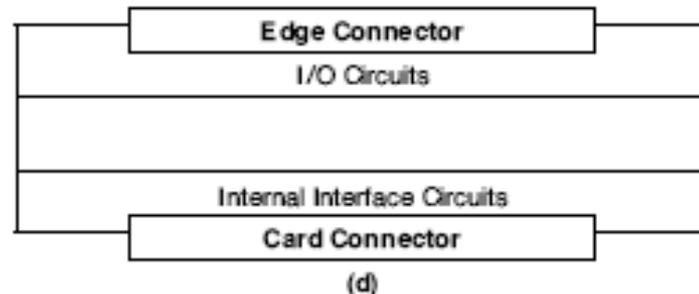
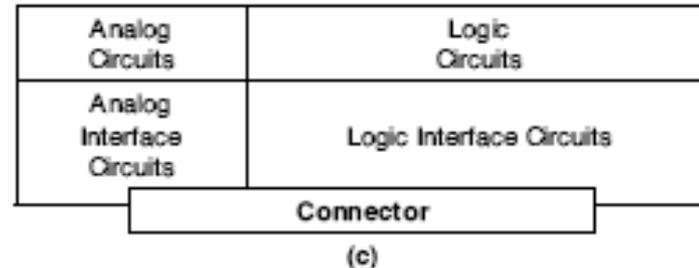
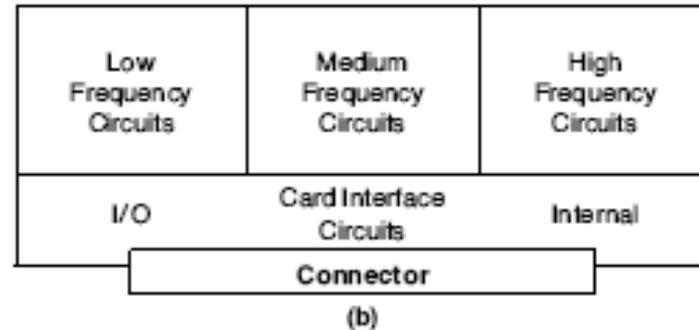
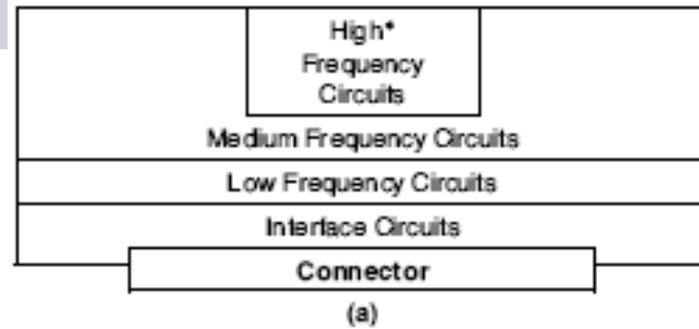


FIGURE 19. Board Layout



- Power supply bussing

- isolated digital and analog power supplies must be used when mixing analog and digital circuitry on a board
- single point common grounding of analog and digital power supplies *at one point and one point only*
  - usually at the motherboard power supply input for multi-card designs, or
  - at the power supply input edge connector on a single card system
- low impedance and good decoupling over a large range of frequencies =>
  - proper power supply and return trace layout and
  - proper use of decoupling capacitors

- Power supply busses behave as transmission lines...
- I want high  $C$ , low  $L \Rightarrow$  low  $Z_0$

e.g.: 16 mA on  $25 \Omega$  makes 400 mV (if no decoupling), ~ TTL noise immunity level: not good!

power and ground planes offer the least overall impedance: good!

all open areas on the PC board should be “landfilled” with a 0 V reference plane  $\Rightarrow$  ground impedance is minimized

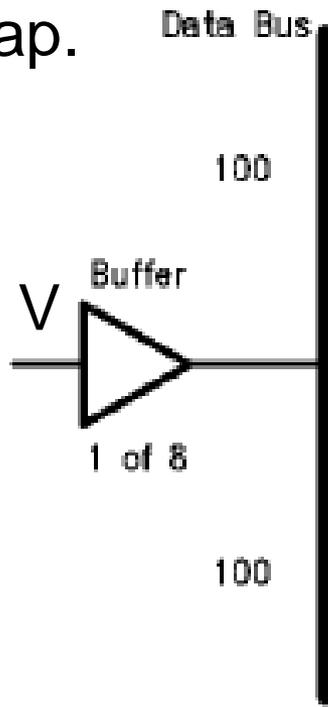
$W/h$ or $D/W$	 #1 $Z_{01}$ Parallel Strips*	 #2 $Z_{02}$ Strip Over Ground Plane*	 #3 $Z_{03}$ Strips Side by Side**
0.5	377	377	NA
0.6	281	281	NA
0.7	241	241	NA
0.8	211	211	NA
0.9	187	187	NA
1.0	169	169	0
1.1	153	153	25
1.2	140	140	34
1.5	112	112	53
1.7	99	99	62
2.0	84	84	73
2.5	67	67	87
3.0	56	56	98
3.5	48	48	107
4.0	42	42	114
5.0	34	34	127
6.0	28	28	137
7.0	24	24	146
8.0	21	21	153
9.0	19	19	160
10.0	17	17	166

- 
- Multi-layer boards:
    - the impedance of a multi-layer power/ground plane bus is very small ( $\sim 1 \Omega$  or less if  $W/h > 100$ )
    - greatly reduced EMI
    - close control of line impedances (where impedance matching is important)
    - shielding benefits can be realized
  - For high-density, high-speed logic applications the use of a multi-layer board is almost mandatory

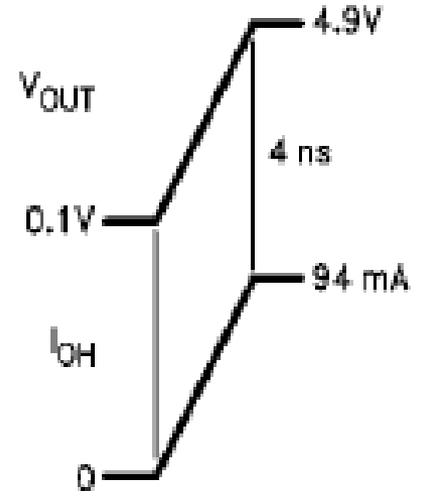
- Local HF decoupling for power supply
  - e.g.: driver in the middle of a 100 Ω bus -> 50 Ω seen
  - for each output: 4.8 V / 50 Ω = 94 mA
  - for all 8 outputs: 750 mA

□ => a decoupling cap. is needed for  $V_{CC}$

- If  $dt = 4 \text{ ns}$ ,  $dV = 0.1 \text{ V}$
- we get  $C > 30 \text{ nF}$



Buffer Output Sees Net 50 ohm Load. 50 ohm Load Line on  $I_{OH}-V_{OH}$  Characteristic shows Low-to-High Step of 4.8V.



Worst Case Octal Drain = 8 x 94 mA = 0.75 Amp

$Q = CV$  charge on capacitor  
 $I = C \text{ d}V/\text{d}t$   
 $C = I \text{ dt}/\text{d}V = 750 \text{ mA} \times 4 \text{ ns} / 0.1\text{V} = 0.030 \mu\text{F}$   
 Select  $C_B = 0.047 \mu\text{F}$  or greater