LVDS

[NS_lvds_ch1, 2, 5]

LVDS (Low Voltage Differential Signaling) benefits

- Low-voltage power supply compatibility
- low noise generation
- high noise rejection
- robust transmission signals
- ability to be integrated into system level ICs

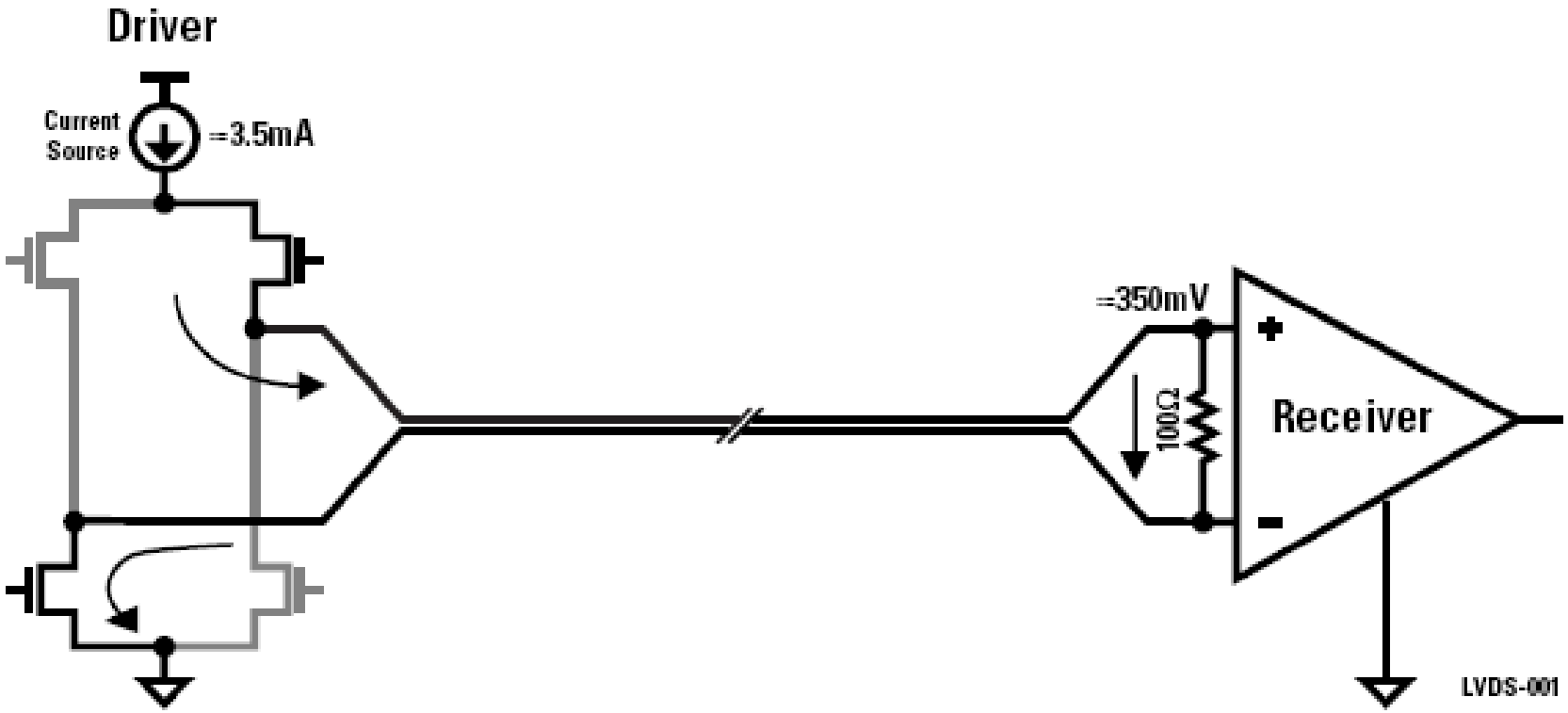


Figure 1.1. Simplified diagram of LVDS Driver and receiver connected via 100Ω differential impedance media

- Nominal current: 3.5 mA
- on 100 Ω: ΔV= 350 mV, centered on 1.25 V

Table 1.1. ANSI/TIA/EIA-644 (LVDS) standards

Parameter	Description	Min	Max	Units
V_{OD}	Differential output voltage	247	454	mV
V_{OS}	Offset voltage	1.125	1.375	V
V_{OD}	|Change to V_{OD}|		50	|mV|
V_{OS}	|Change to V_{OS}|		50	|mV|
I_{SA}, I_{SB}	Short circuit current		24	|mA|
tr/tf	Output rise/fall times (200 Mbps)	0.26	1.5	ns
	Output rise/fall times (<200 Mbps)	0.26	30% of tui†	ns
I_{IN}	Input current		20	|µA|
V_{TH}	Receive threshold voltage		+100	mV
V_{IN}	Input voltage range	0	2.4	V

† tui is unit interval (i.e. bit width).

Note: Actual datasheet specifications may be significantly better.

- Advantage of the differential approach: noise is mostly coupled onto the two wires as common-mode -> it is rejected by the differential receivers
- Differential technologies such as LVDS reduce concerns about noise -> they can use lower signal voltage swings
- Drivers and receivers do not depend on a specific power supply, such as 5V -> easy migration path to lower supply voltages such as 3.3V or even 2.5V

LVDS configurations

Figure 2.3. Point-to-point configuration

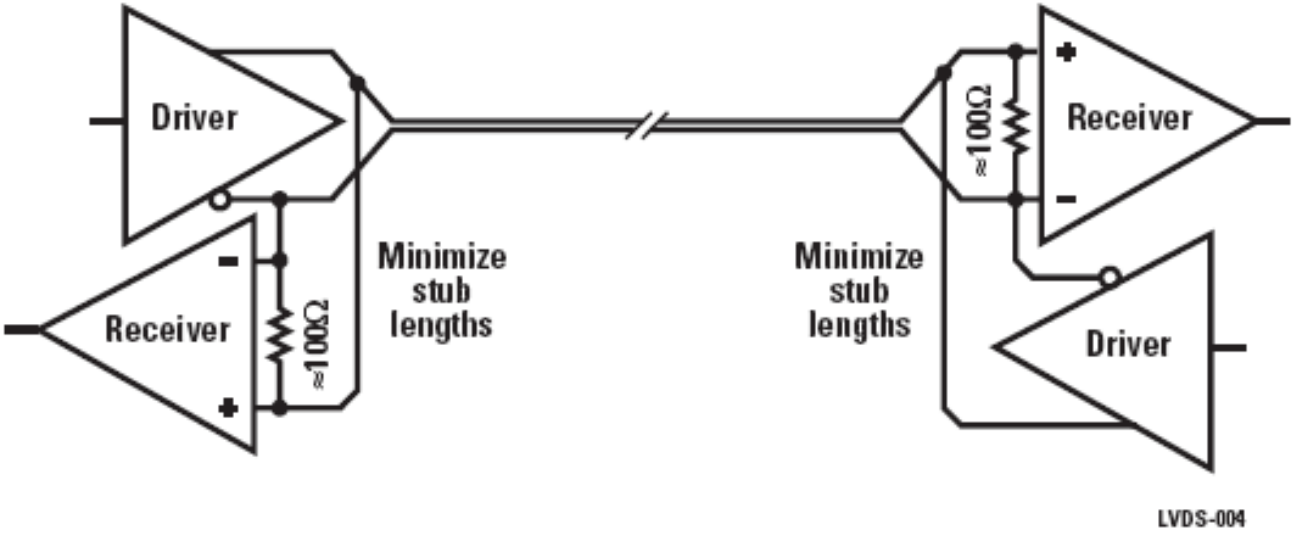


Figure 2.4. Bi-directional half-duplex configuration

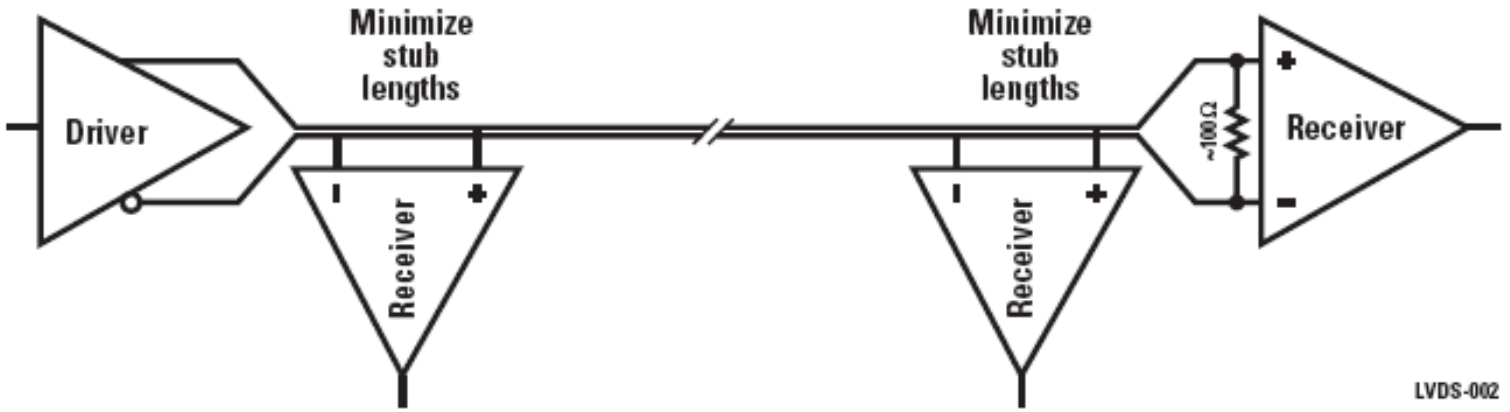


Figure 2.5. Multidrop configuration

SerDes

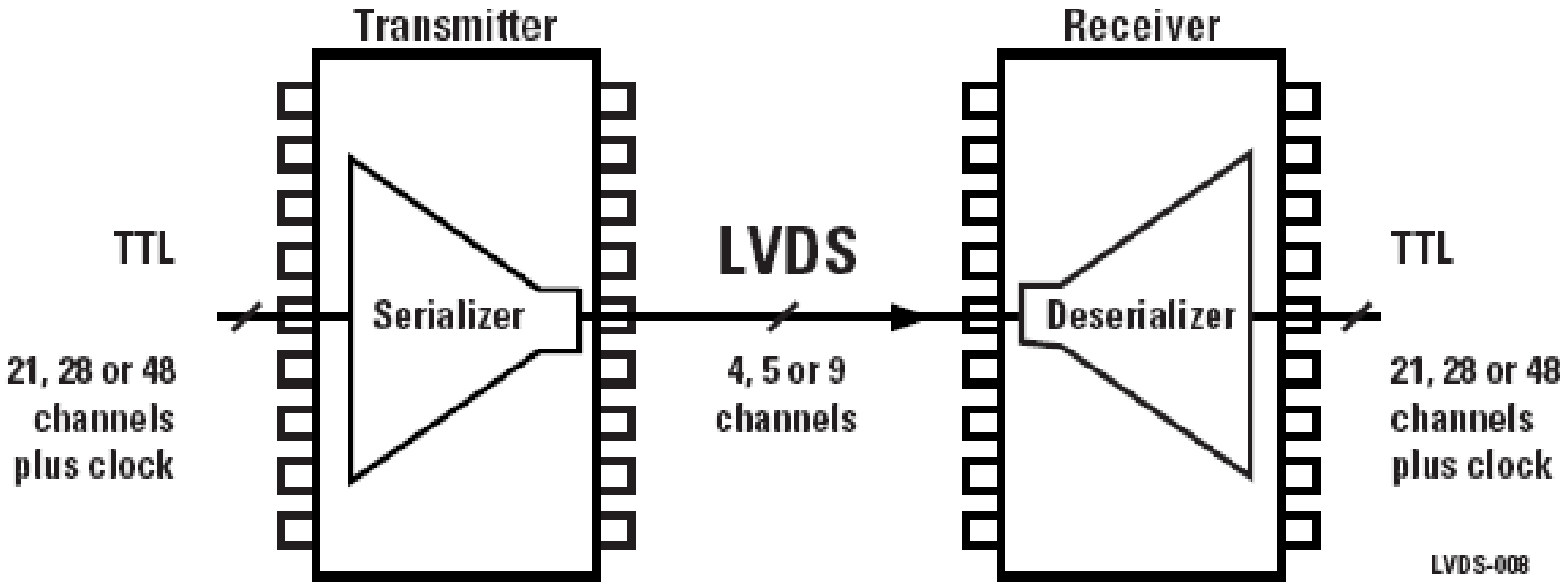
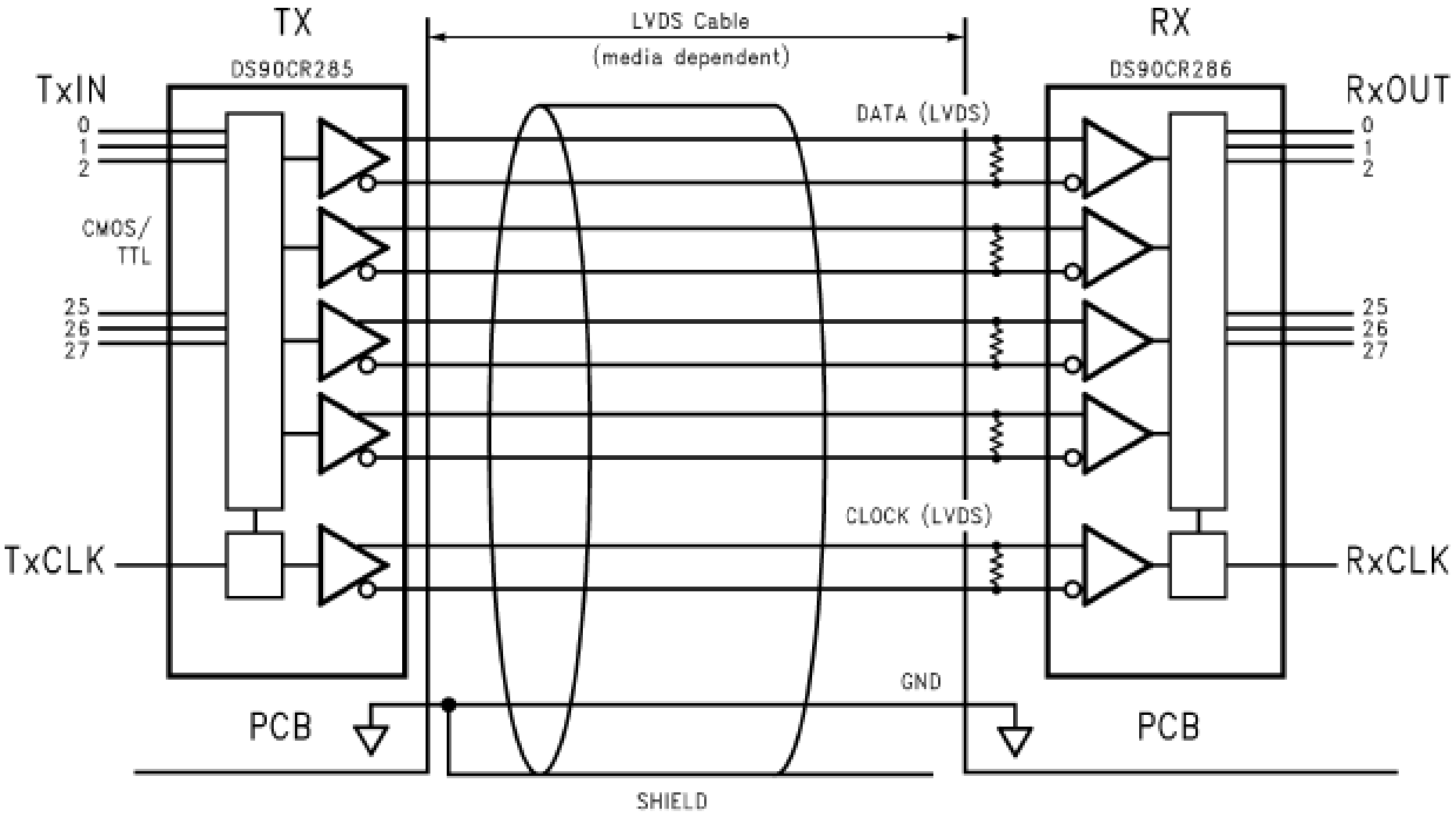


Figure 2.6. National's Channel Link chipsets convert a TTL bus into a compact LVDS data stream and back to TTL

E.g.: DS90CR285/286



- 28+1(clock, 66 MHz) bit, i.e. 28*66= 1.848 Gb/s = 231 MB/s =>
- 4 twisted pairs (462 Mb/s each) + clock

For a robust backplane interface

Pay attention to

- stub length (t_r~0.3 ns -> max 2.5 cm)
- ESD protection
- capacitive loading: for a card inserted on a bus it could be around

  2-3 pF (connector)+

  2-3 pF (trace)+

  4-5 pF (device)

  =~10pF

LVDS and Bus LVDS

- *Standard LVDS*: if terminated on both sides, we get 50 Ω
  - with a standard LVDS (3.5 mA) we get 175 mV: too low
  - depending upon load spacing, effective impedance of the bus may drop further, and for signal quality reasons terminations may be as low as 60 Ω -> 30 Ω
  - with a standard LVDS (3.5 mA) we get 105 mV: too low

- *Bus LVDS, or BLVDS*: new family of bus interface circuits based on LVDS technology, specifically addressing multipoint cable or backplane applications
  - it differs from standard LVDS in providing increased drive current to handle double terminations that are required in multipoint applications
  - 10 mA on 30 Ω -> 300 mV

Configurations for BusLVDS

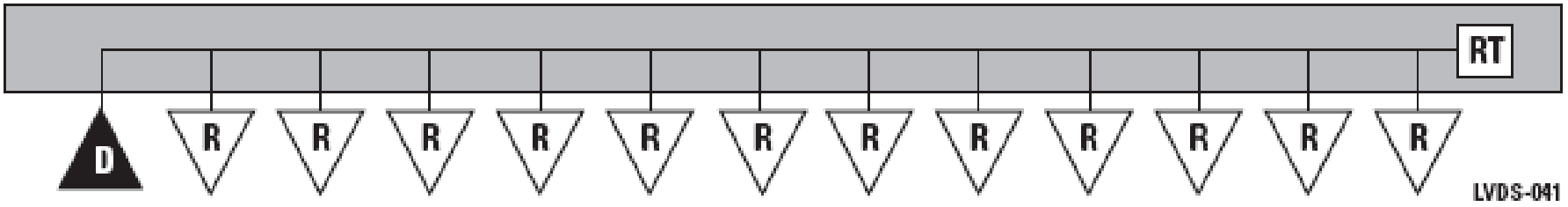


Figure 5.1. Multidrop application with a single termination

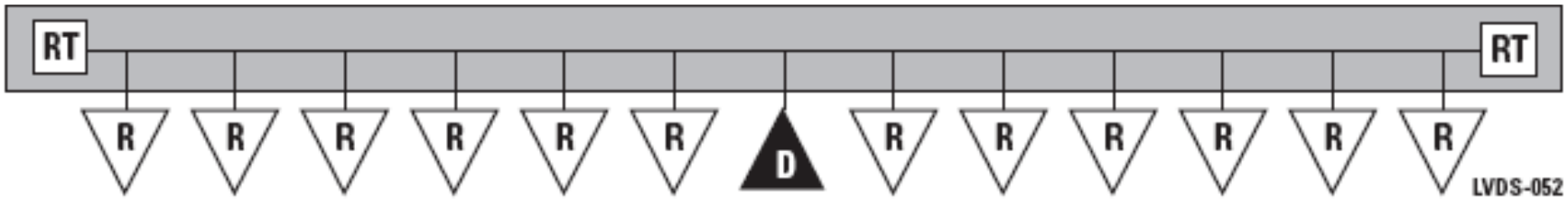


Figure 5.2. Multidrop application with double termination

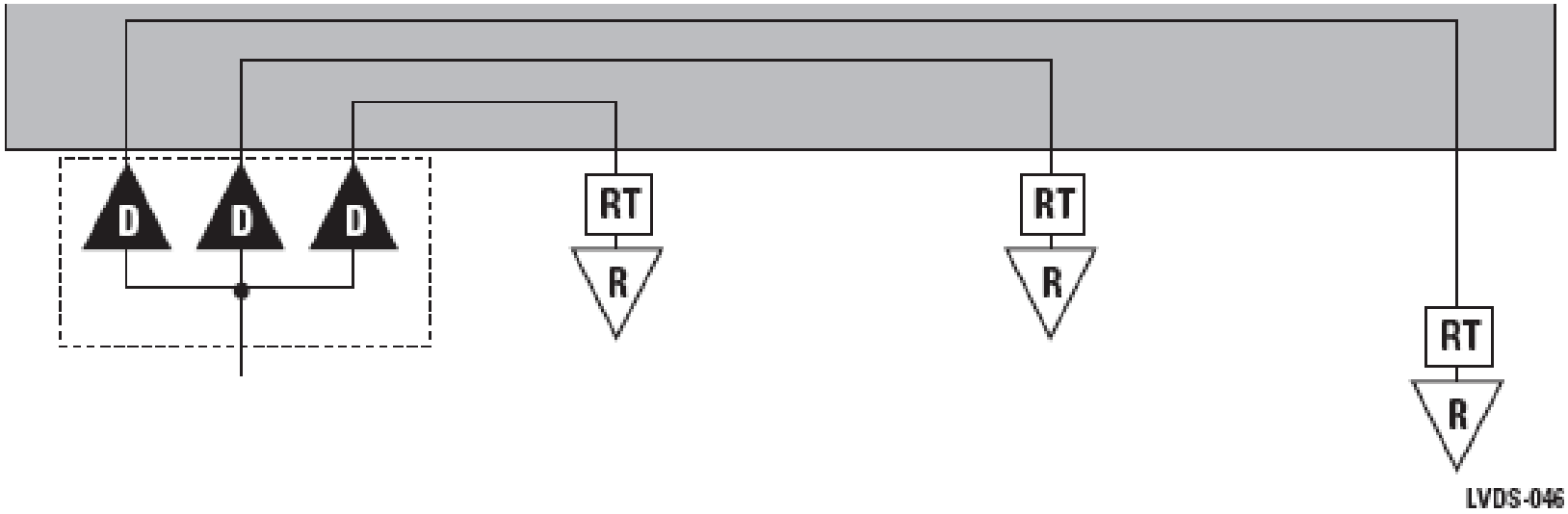


Figure 5.3. Data distribution application

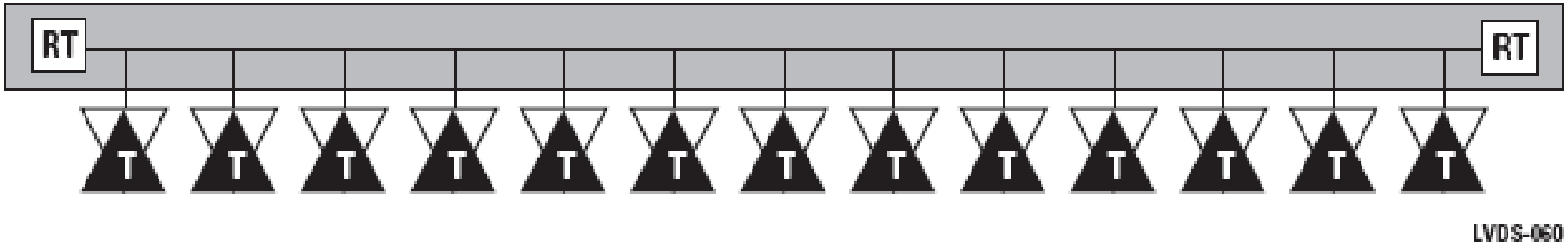


Figure 5.4. Multipoint application

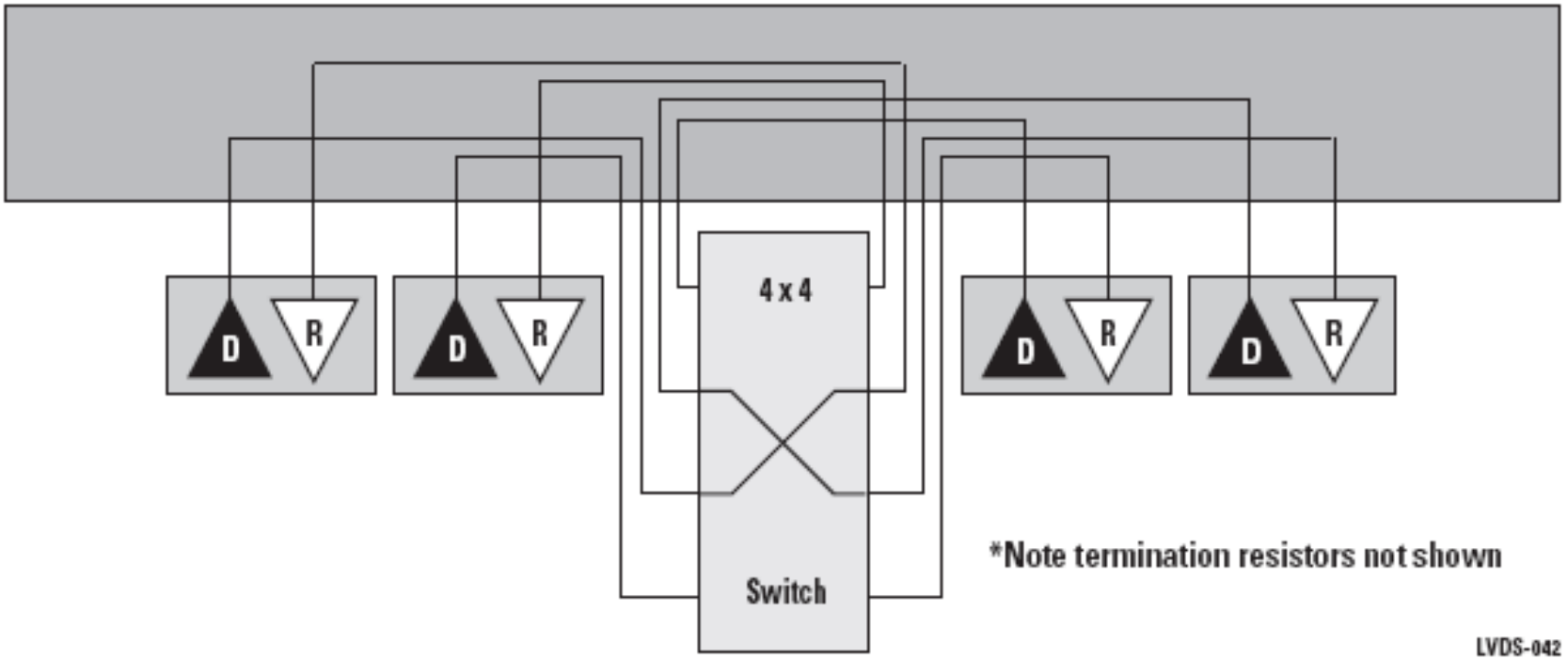


Figure 5.5. Switch application

Connectors

- Special connectors
- Standard, matrix based (3x32), e.g.

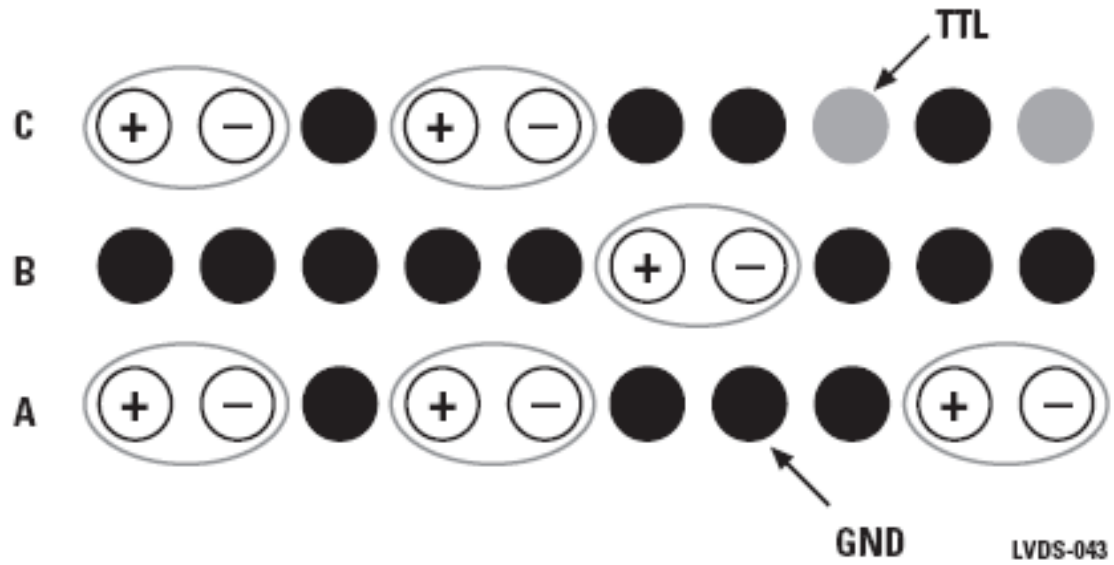


Figure 5.11. Typical connector pinouts

HPC FMC connector

	K	J	H	G	F	E	D	C	B	A
1	VREF_B_M2C	GND	VREF_A_M2C	GND	PG_M2C	GND	PG_C2M	GND	RES1	GND
2	GND	CLK3_M2C_P	PRSNT_M2C_L	CLK1_M2C_P	GND	HA01_P_CC	GND	DP0_C2M_P	GND	DP1_M2C_P
3	GND	CLK3_M2C_N	GND	CLK1_M2C_N	GND	HA01_N_CC	GND	DP0_C2M_N	GND	DP1_M2C_N
4	CLK2_M2C_P	GND	CLK0_M2C_P	GND	HA00_P_CC	GND	GBTCLK0_M2C_P	GND	DP9_M2C_P	GND
5	CLK2_M2C_N	GND	CLK0_M2C_N	GND	HA00_N_CC	GND	GBTCLK0_M2C_N	GND	DP9_M2C_N	GND
6	GND	HA03_P	GND	LA00_P_CC	GND	HA05_P	GND	DP0_M2C_P	GND	DP2_M2C_P
7	HA02_P	HA03_N	LA02_P	LA00_N_CC	HA04_P	HA05_N	GND	DP0_M2C_N	GND	DP2_M2C_N
8	HA02_N	GND	LA02_N	GND	HA04_N	GND	LA01_P_CC	GND	DP8_M2C_P	GND
9	GND	HA07_P	GND	LA03_P	GND	HA09_P	LA01_N_CC	GND	DP8_M2C_N	GND
10	HA06_P	HA07_N	LA04_P	LA03_N	HA08_P	HA09_N	GND	LA06_P	GND	DP3_M2C_P
11	HA06_N	GND	LA04_N	GND	HA08_N	GND	LA05_P	LA06_N	GND	DP3_M2C_N
12	GND	HA11_P	GND	LA08_P	GND	HA13_P	LA05_N	GND	DP7_M2C_P	GND
13	HA10_P	HA11_N	LA07_P	LA08_N	HA12_P	HA13_N	GND	GND	DP7_M2C_N	GND
14	HA10_N	GND	LA07_N	GND	HA12_N	GND	LA09_P	LA10_P	GND	DP4_M2C_P
15	GND	HA14_P	GND	LA12_P	GND	HA16_P	LA09_N	LA10_N	GND	DP4_M2C_N
16	HA17_P_CC	HA14_N	LA11_P	LA12_N	HA15_P	HA16_N	GND	GND	DP6_M2C_P	GND
17	HA17_N_CC	GND	LA11_N	GND	HA15_N	GND	LA13_P	GND	DP6_M2C_N	GND
18	GND	HA18_P	GND	LA16_P	GND	HA20_P	LA13_N	LA14_P	GND	DP5_M2C_P
19	HA21_P	HA18_N	LA15_P	LA16_N	HA19_P	HA20_N	GND	LA14_N	GND	DP5_M2C_N
20	HA21_N	GND	LA15_N	GND	HA19_N	GND	LA17_P_CC	GND	GBTCLK1_M2C_P	GND
21	GND	HA22_P	GND	LA20_P	GND	HB03_P	LA17_N_CC	GND	GBTCLK1_M2C_N	GND
22	HA23_P	HA22_N	LA19_P	LA20_N	HB02_P	HB03_N	GND	LA18_P_CC	GND	DP1_C2M_P
23	HA23_N	GND	LA19_N	GND	HB02_N	GND	LA23_P	LA18_N_CC	GND	DP1_C2M_N
24	GND	HB01_P	GND	LA22_P	GND	HB05_P	LA23_N	GND	DP9_C2M_P	GND
25	HB00_P_CC	HB01_N	LA21_P	LA22_N	HB04_P	HB05_N	GND	GND	DP9_C2M_N	GND
26	HB00_N_CC	GND	LA21_N	GND	HB04_N	GND	LA26_P	LA27_P	GND	DP2_C2M_P
27	GND	HB07_P	GND	LA25_P	GND	HB09_P	LA26_N	LA27_N	GND	DP2_C2M_N
28	HB06_P_CC	HB07_N	LA24_P	LA25_N	HB08_P	HB09_N	GND	GND	DP8_C2M_P	GND
29	HB06_N_CC	GND	LA24_N	GND	HB08_N	GND	TCK	GND	DP8_C2M_N	GND
30	GND	HB11_P	GND	LA29_P	GND	HB13_P	TDI	SCL	GND	DP3_C2M_P
31	HB10_P	HB11_N	LA28_P	LA29_N	HB12_P	HB13_N	TDO	SDA	GND	DP3_C2M_N
32	HB10_N	GND	LA28_N	GND	HB12_N	GND	3P3VAUX	GND	DP7_C2M_P	GND
33	GND	HB15_P	GND	LA31_P	GND	HB19_P	TMS	GND	DP7_C2M_N	GND
34	HB14_P	HB15_N	LA30_P	LA31_N	HB16_P	HB19_N	TRST_L	GA0	GND	DP4_C2M_P
35	HB14_N	GND	LA30_N	GND	HB16_N	GND	GA1	12P0V	GND	DP4_C2M_N
36	GND	HB18_P	GND	LA33_P	GND	HB21_P	3P3V	GND	DP6_C2M_P	GND
37	HB17_P_CC	HB18_N	LA32_P	LA33_N	HB20_P	HB21_N	GND	12P0V	DP6_C2M_N	GND
38	HB17_N_CC	GND	LA32_N	GND	HB20_N	GND	3P3V	GND	GND	DP5_C2M_P
39	GND	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	DP5_C2M_N
40	VIO_B_M2C	GND	VADJ	GND	VADJ	GND	3P3V	GND	RES0	GND

Hot plugging (1/2)

- Live insertion (“hot swapping”) is of particular importance to the telecommunications marketplace
  - in these applications, maintenance, upgrading and repair must be performed without shutting down the entire system or causing disruption to the traffic on the backplane.
- Bus LVDS’s wide common-mode range of ±1V plays a key role in supporting this function
  - upon insertion of a card into a live backplane, the occurrence of abnormalities on the signals are common on both signals -> data is not impacted

Hot plugging (2/2)

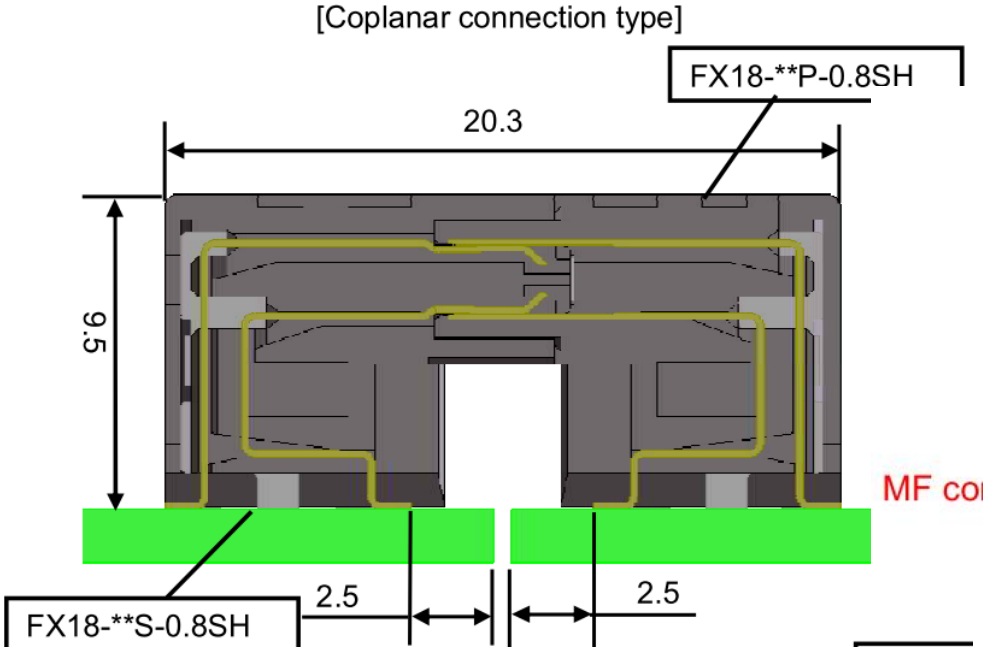
- However, standard power sequencing is still recommended to ensure proper biasing of the devices (substrate)
- for insertion, the following sequence should be guaranteed by hardware design:

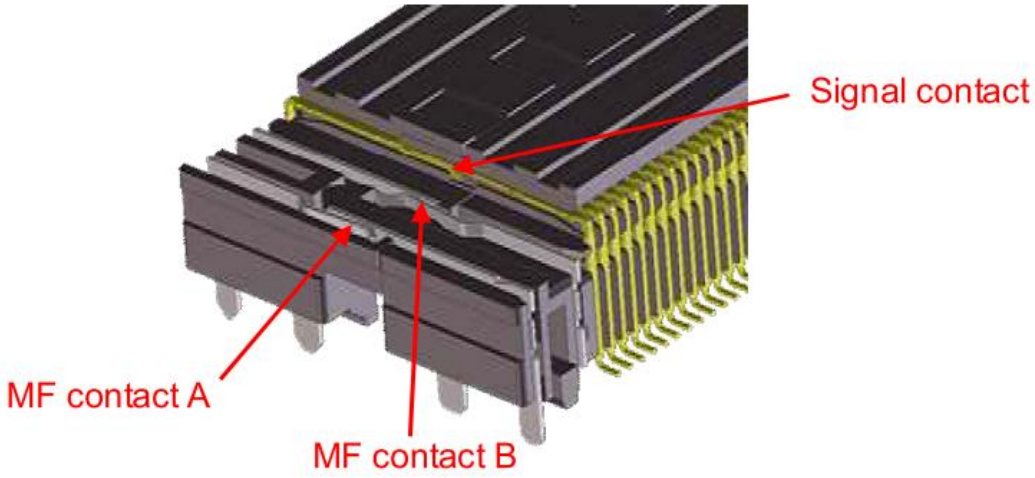
  1. ground
  2. power
  3. I/O pins

- for removal, the reverse is recommended (3-2-1)

Example: Hirose FX18 Series connectors

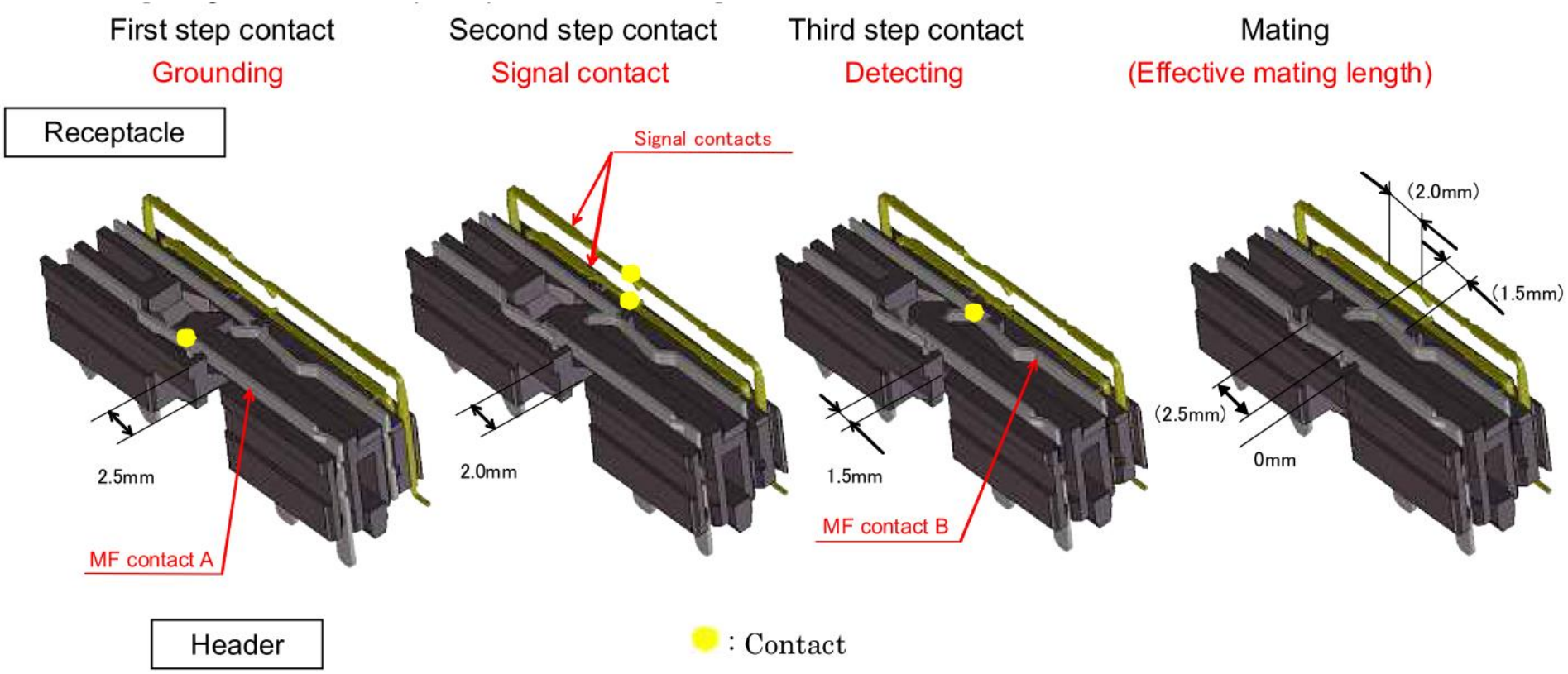
- High speed 0.8mm pitch board to board bonnectors
- 40 to 140 pins





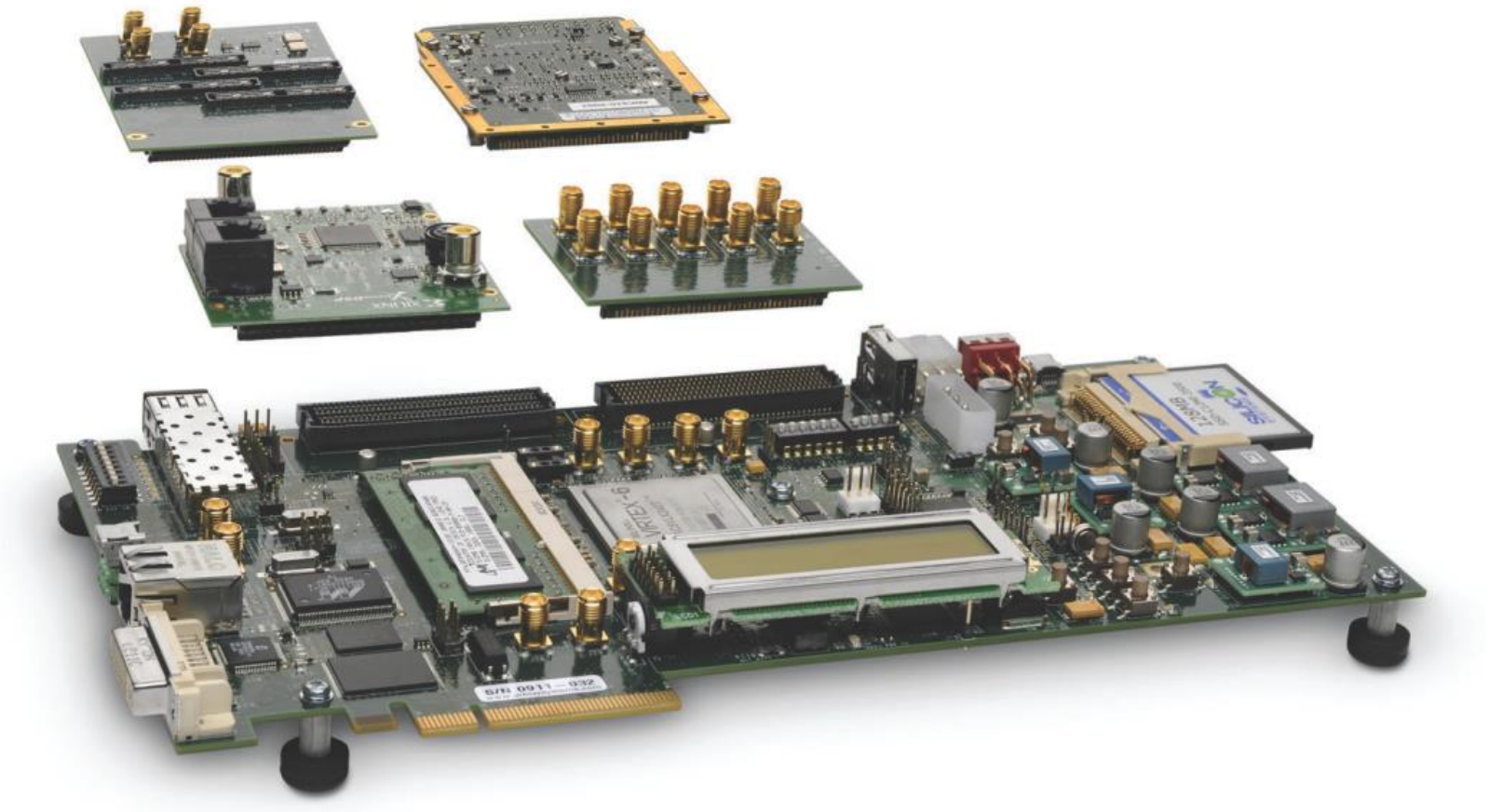
- On the guide posts on both sides of the connector, two rows of multi-functional (MF) contacts are placed for the following uses
  - enhancing ground connection between boards
  - using as a power line (3A/line)
  - three-step sequence structure including signal contact

Example: Hirose FX18 Series connectors

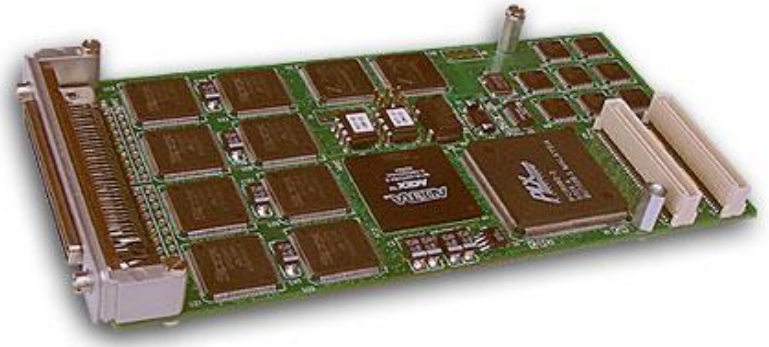


Mezzanine cards

Daughterboard, mezzanine board or *piggyback board*: an expansion card that directly attaches to a system



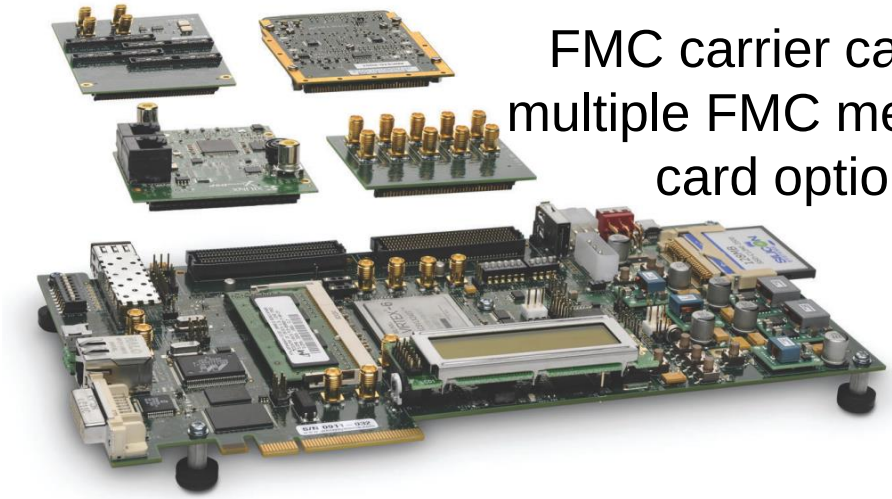
Mezzanine cards



Several standards

- PCI Mezzanine Cards (PMC)

- PCIexpress Mezzanine Card (XMC)



FMC carrier card and multiple FMC mezzanine card options

- FPGA Mezzanine Card (FMC)

Mezzanine cards

- Advanced Mezzanine Cards (AMC)