Balanced lines

[tektronix_8000b, AN1406, NS_lvds_ch3, TI_slla120, smolyansky]

Impedences

- *Characteristic impedance*: impedance between two conductors when there is no coupling to ground

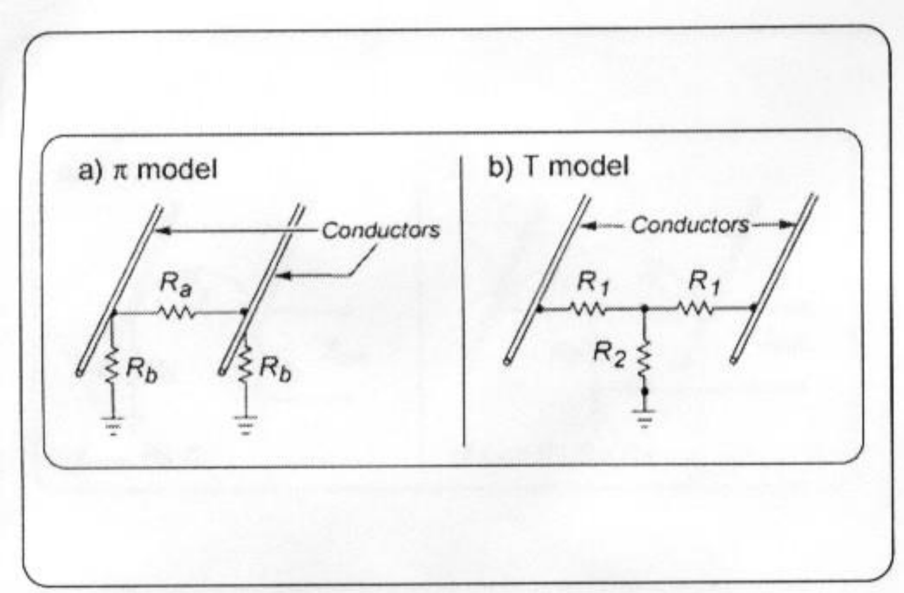


Figure 1. *Models of a differential line.*

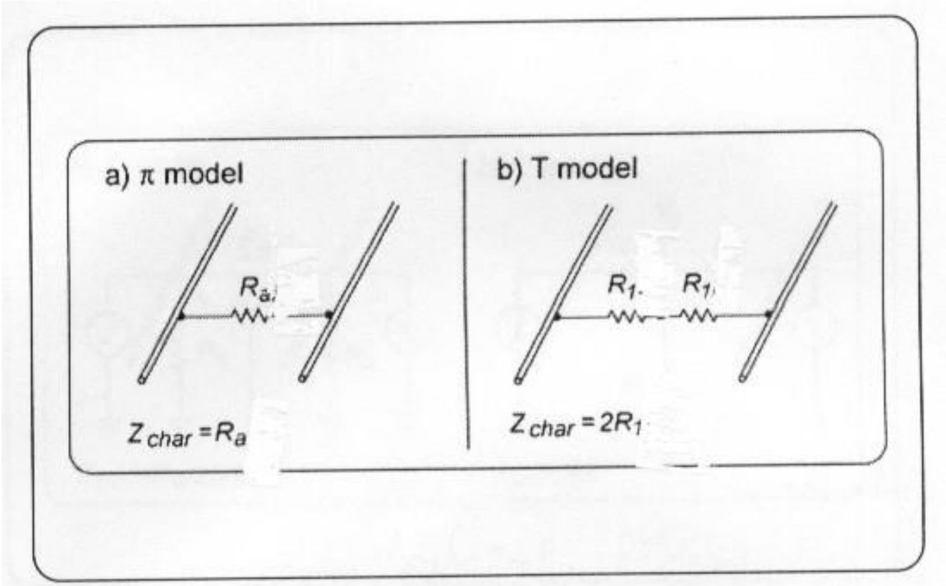


Figure 2. *Models for measuring the Characteristic Impedance.*

- *Odd-mode impedance*: impedance of *one* conductor to ground when the pair is driven differentially
- *Even-mode impedance*: impedance of *one* conductor to ground when the pair is driven with equal polarity signals

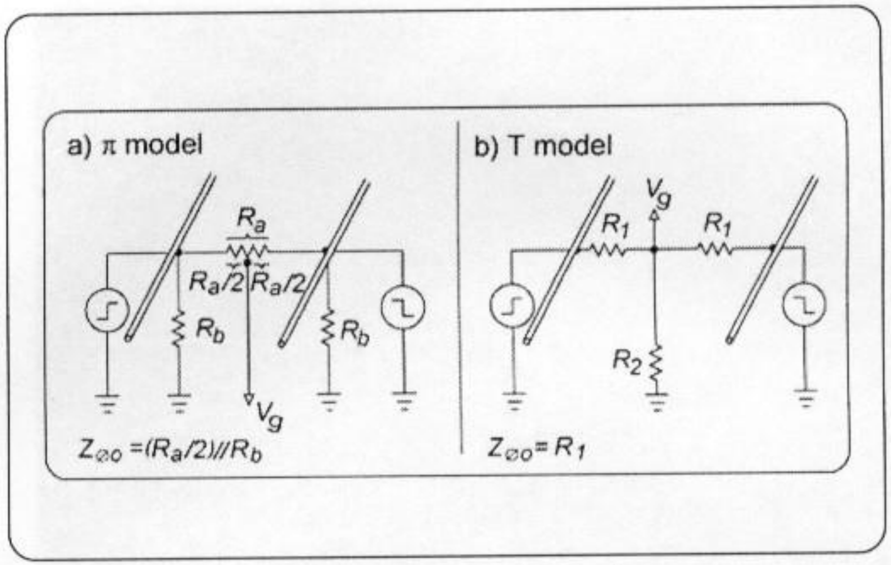


Figure 5. Models for calculating the Odd-mode Impedance.

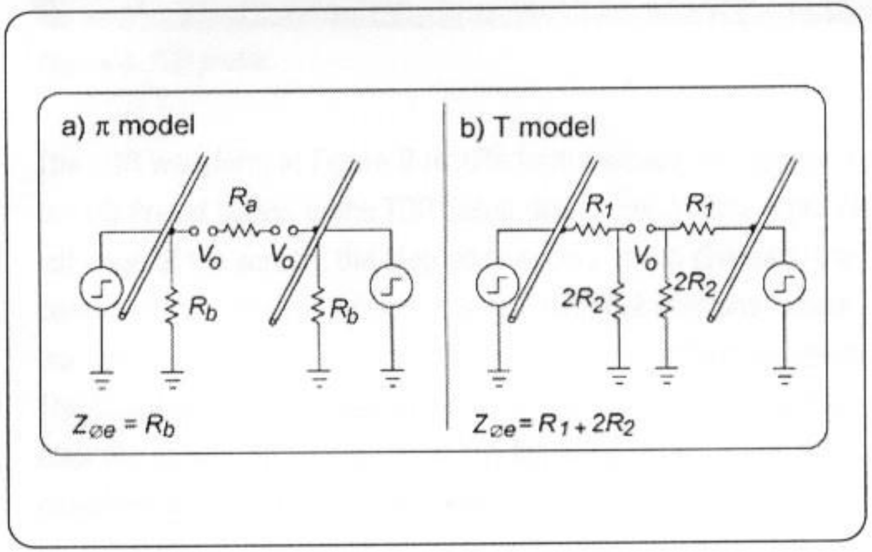


Figure 6. Models for Calculating the Even-mode Impedance.

- *Differential impedance*: impedance between two conductors
  - when there is no coupling to ground, it is equal to the characteristic impedance
- *Common-mode impedance*:
  - impedance between the two conductors (*connected to each other*) and ground

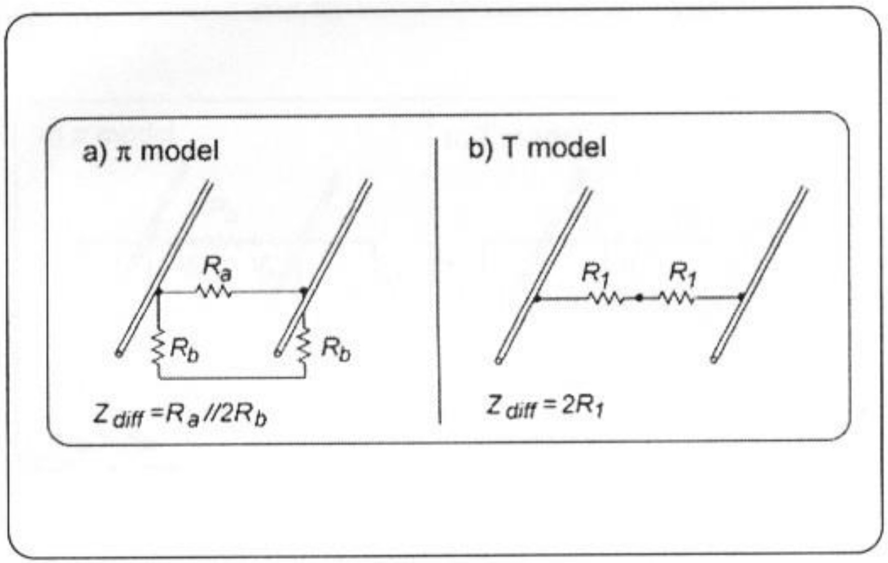


Figure 3. *Models for measuring the Differential Impedance.*

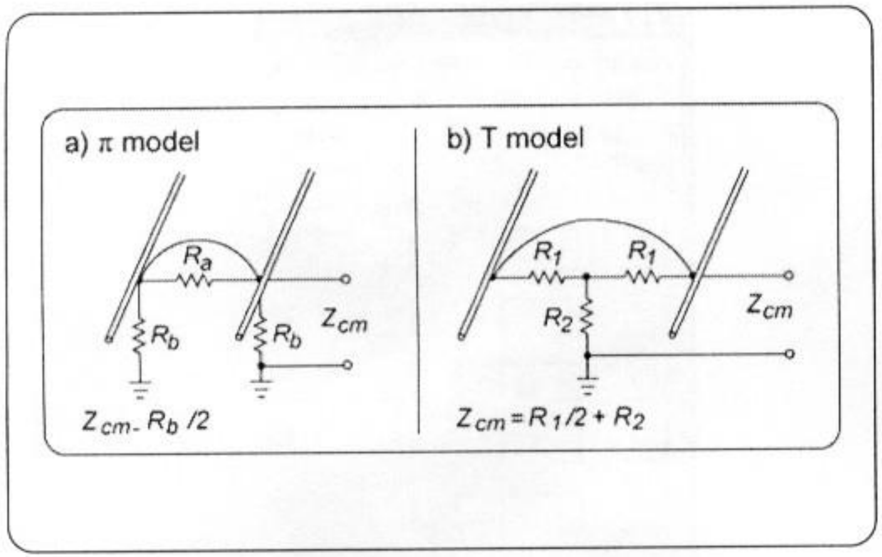


Figure 4. *Models for measuring the Common-mode Impedence.*

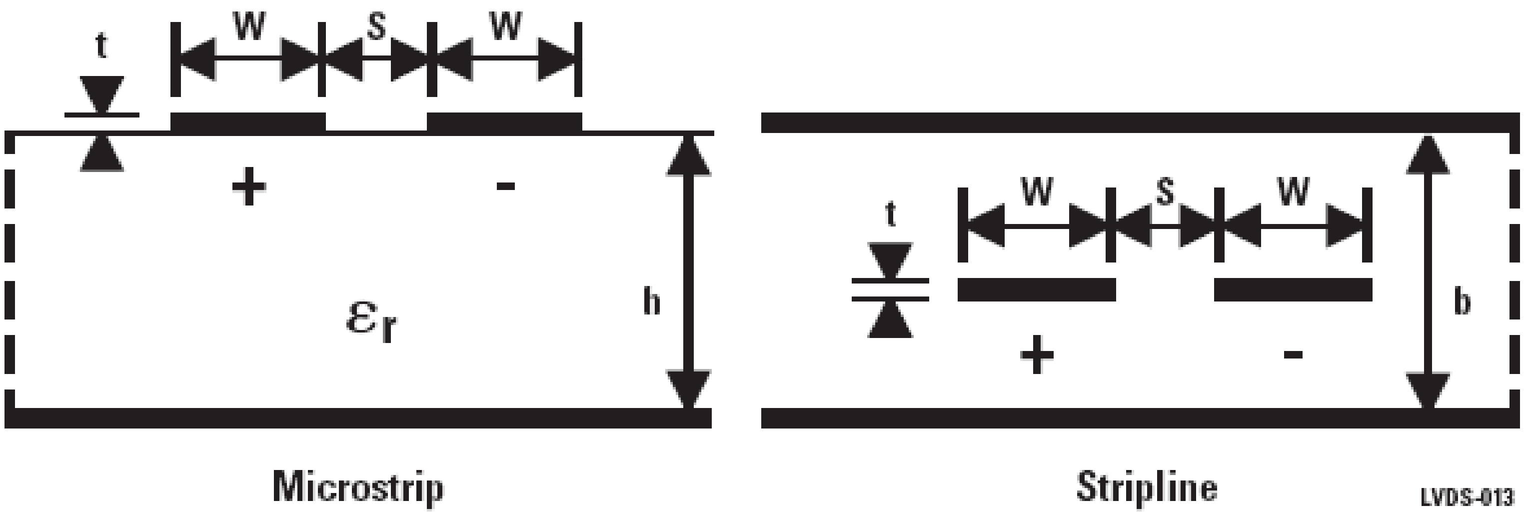
Impedences

- $Z_{odd} = Z_{diff} / 2$
- $Z_{even} = 2\ Z_{common\_mode}$
- if no coupling with ground: $Z_{diff} = Z_{char}$
- Measures: from Z_{odd} and Z_{even} (measured) we can calculate

$Z_{diff} = 2\ Z_{odd} = Z_{odd1} + Z_{odd2}$

$Z_{common\_mode} = Z_{even} / 2 = Z_{even1} // Z_{even2}$

Edge-coupled microstrip and stripline



Microstrip

$$Z_{DIFF} \approx 2 \times Z_0 \left(1 - 0.48e^{-0.96\frac{S}{h}}\right) \Omega$$

Stripline

$$Z_{DIFF} \approx 2 \times Z_0 \left(1 - 0.374e^{-0.29\frac{S}{b}}\right) \Omega$$

Microstrip

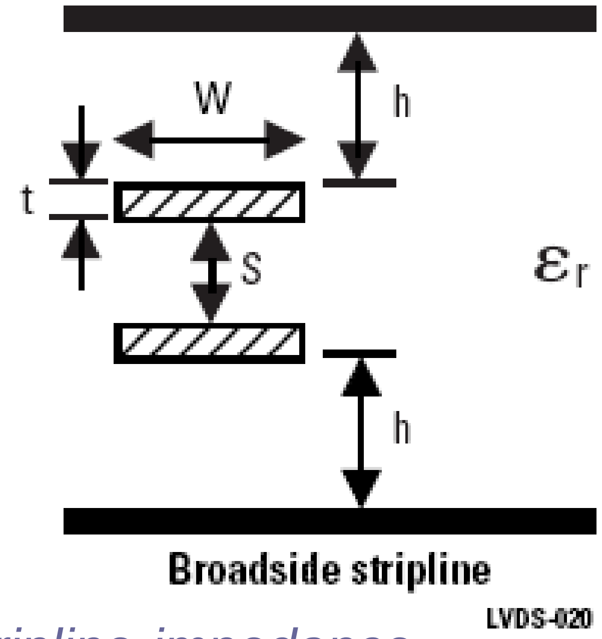
$$Z_0 = \frac{60}{\sqrt{0.457\varepsilon_r + 0.67}} \ell n \left(\frac{4h}{0.67(0.8W + t)}\right) \Omega$$

Stripline

$$Z_0 = \frac{60}{\sqrt{\varepsilon_r}} \ell n \left(\frac{4b}{0.67\pi(0.8W + t)}\right) \Omega$$

Note: For edge-coupled striplines, the term "0.374" may be replaced with "0.748" for lines which are closely coupled (S < 12 mils).

Broad-side striplines



- "Field solver needed to compute Z_{diff}"
- … but a calculator is available e.g. here

https://www.eeweb.com/tools/broadside-coupled-stripline-impedance

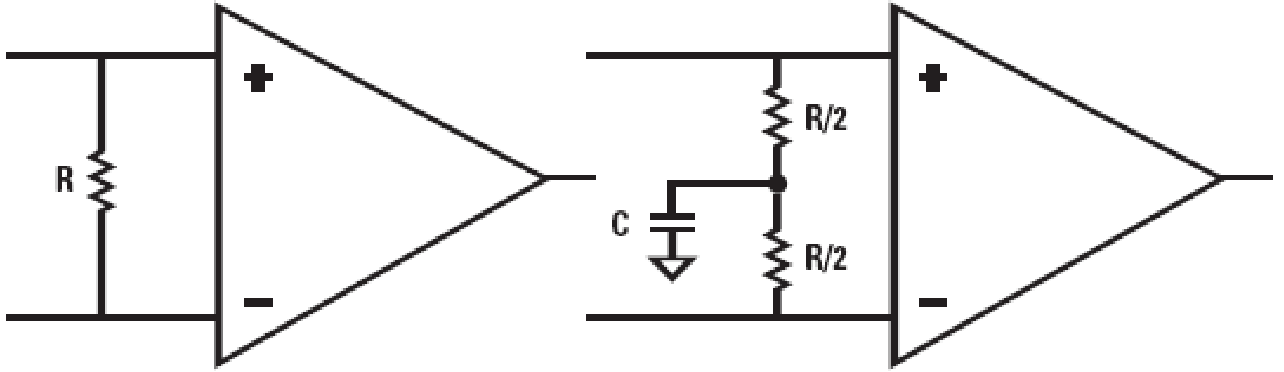
https://www.multekpcb.com/calculators/

$$Z_0 = \frac{80}{\sqrt{\varepsilon_r}} \ln\left(\frac{1.9(2h+t)}{(0.8w+t)}\right)\left(1-\frac{h}{4(h+h_1+t)}\right)$$

Note: valid for (w/h) from 0.1 to 2.0 and (t/h) less than 0.25

- *Please note: different sites may use slightly different formulas ☹*

Termination (e.g. for LVDS)



Where R = Z_{DIFF} (between 100Ω and 120Ω), C ≈ 50 pF

- Center tap capacitance termination may also be used in conjunction with two 50 ohm resistors to filter common-mode noise at the expense of extra components

The “S” Rule

Using the edge-to-edge *S* distance between the traces of a pair, other separations can be defined:

- The distance between two pairs should be >2*S*.
- The distance between a pair and a TTL/CMOS signal should be >3*S*. Even better,
  - locate the TTL/CMOS signals on a different plane isolated by a ground plane
- If a guard ground trace or ground fill is used, it should be >2*S* away.

Various standards (1/2)

- LVDS (see later)
- CML (current mode logic)
  - CML drivers provide several design features, including high-speed capabilities, adjustable logic output swing, level adjustment, and adjustable slew rate
  - the outputs (Output+ and Output–) require pullup resistors to V_{DD}

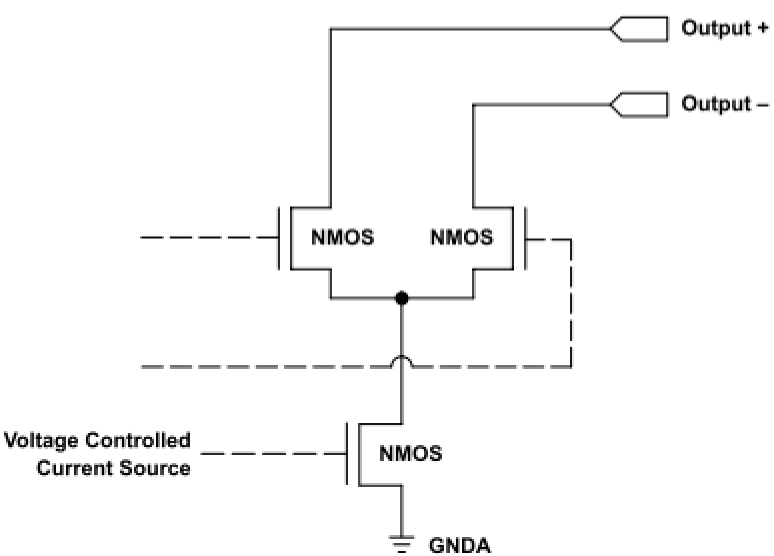


Figure 4. Typical Structure for a CML Output Stage

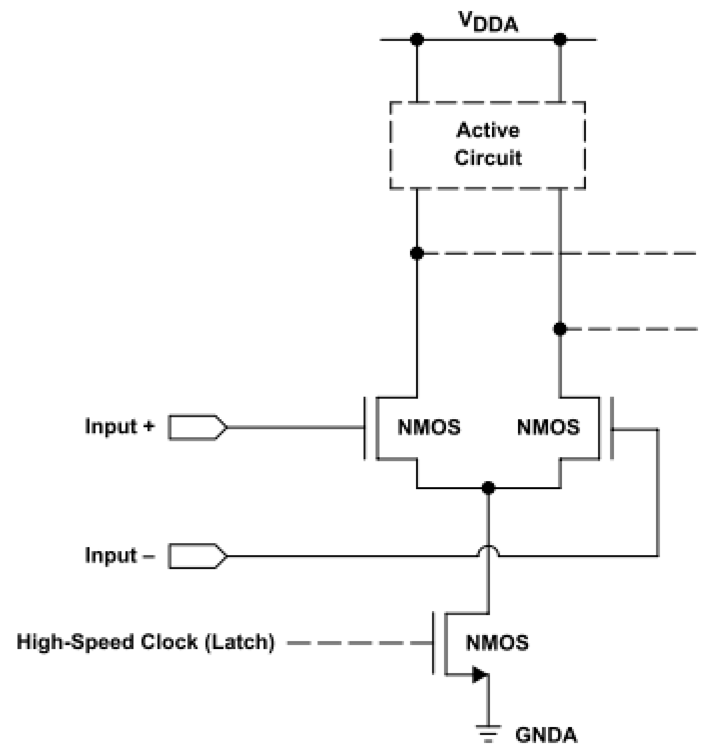


Figure 5. Input Stage for Devices Requiring CML Signaling Levels

Various standards (2/2)

- LVPECL (Low-voltage positive/pseudo emitter–coupled logic)
  - LVPECL is derived from ECL and PECL and typically uses 3.3 V and ground supply voltage
- …

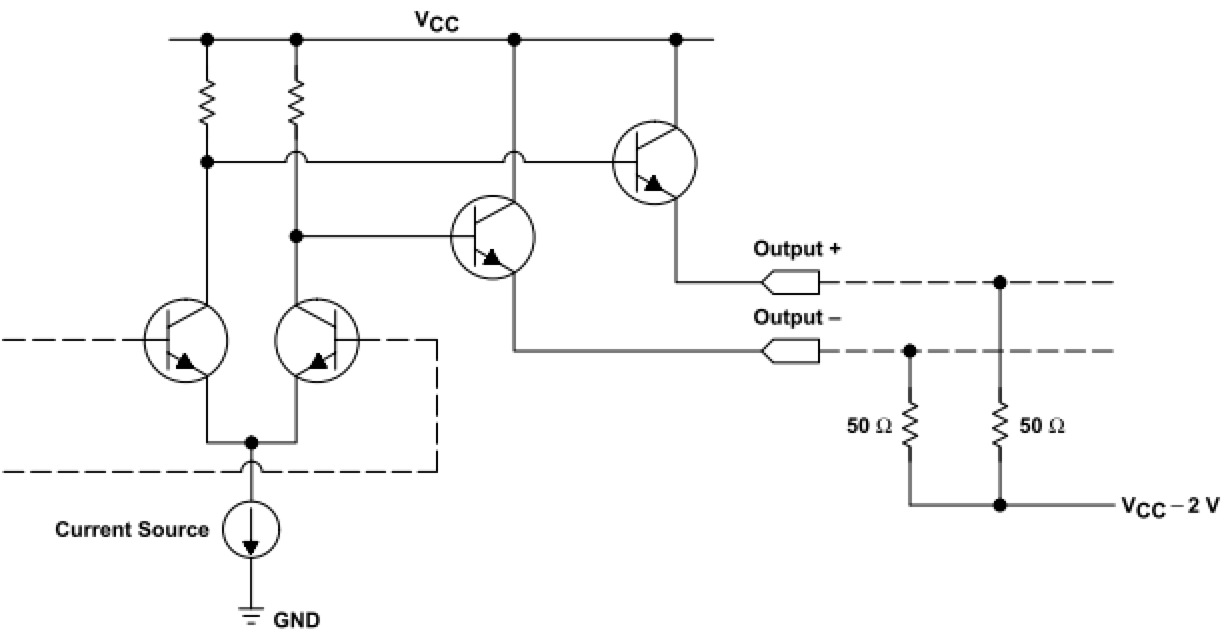


Figure 2. Typical Structure for an LVPECL Output Stage

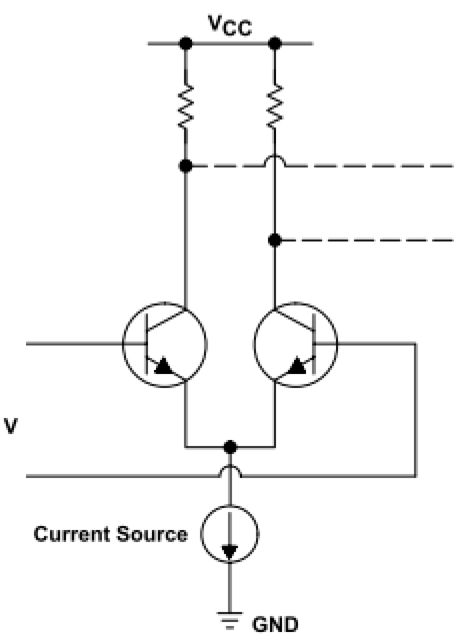


Figure 3. Input Stage for Devices Requiring LVPECL Signaling Levels

Various cable standards

Differential cables are

- often/normally twisted
- sometimes/often shielded
  - e.g., both unshielded and shielded Ethernet cables do exist
  - e.g., *twinaxial* is shielded
    - used e.g. in 100 Gbit ethernet and SATA 3.0

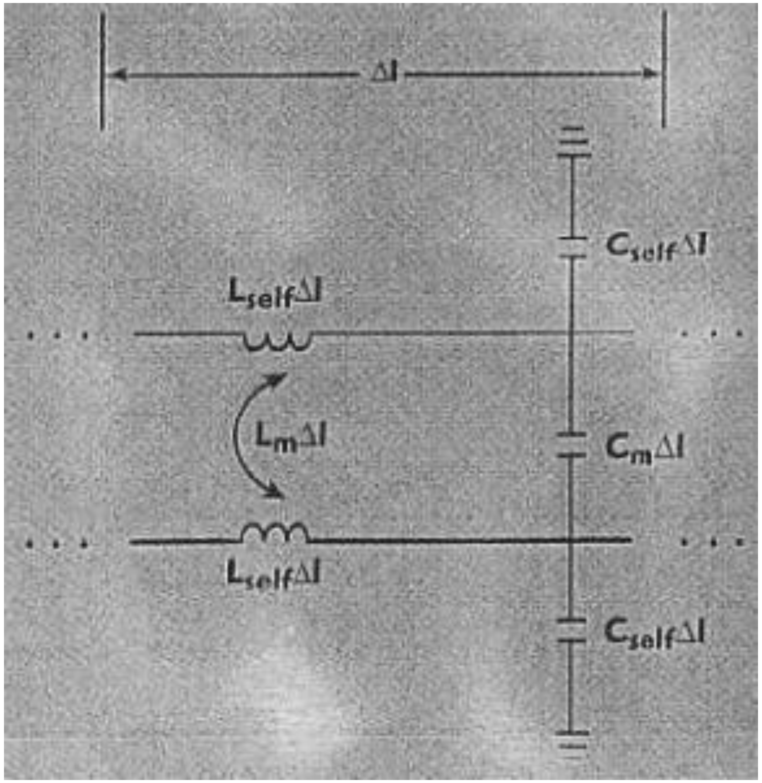
Differential line modelling

- Due to coupling between the two lines, propagation is described by a couple of L and C matrices:

$$L = \begin{bmatrix} L_{self} & L_m \\ L_m & L_{self} \end{bmatrix}$$

$$C = \begin{bmatrix} C_{tot} & -C_m \\ -C_m & C_{tot} \end{bmatrix}$$

- with $C_{tot} = C_{self} + C_m$



Differential line modelling

It may be found that

$$t_{odd} = l\sqrt{(L_{self} - L_m)(C_{tot} + C_m)}$$
$$t_{even} = l\sqrt{(L_{self} + L_m)(C_{tot} - C_m)}$$

$$Z_{odd} = \sqrt{\frac{L_{self} - L_m}{C_{tot} + C_m}}$$
$$Z_{even} = \sqrt{\frac{L_{self} + L_m}{C_{tot} - C_m}}$$

Note that

- for $L_m=0$ and $C_m=0$ we get the usual values for a transmission line
- for $L_m \neq 0$ and $C_m \neq 0$ we have $Z_{even} > Z_{odd}$
- for $L_m \neq 0$ and $C_m \neq 0$ normally we have $t_{even} \neq t_{odd}$
  - if a significant amount of common mode energy is present in the signal, we'll observe signal splitting -> bit errors