High speed design: the clock

[AN1091, altera_wp_dpa2]

Example

CLOCK TRACE LINE LENGTHS: A — 9.4 INCHES
B — 8.6 INCHES
C — 9.6 INCHES
D — 7.8 INCHES

— TERMINATION SYMBOL

— DEVICE INPUT CONNECTION

MC88914
CLOCK DRIVER

A

D

C

B

PROPRIETARY
ASIC

PROPRIETARY
ASIC

MC88100
CPU

MC88200
CMMU
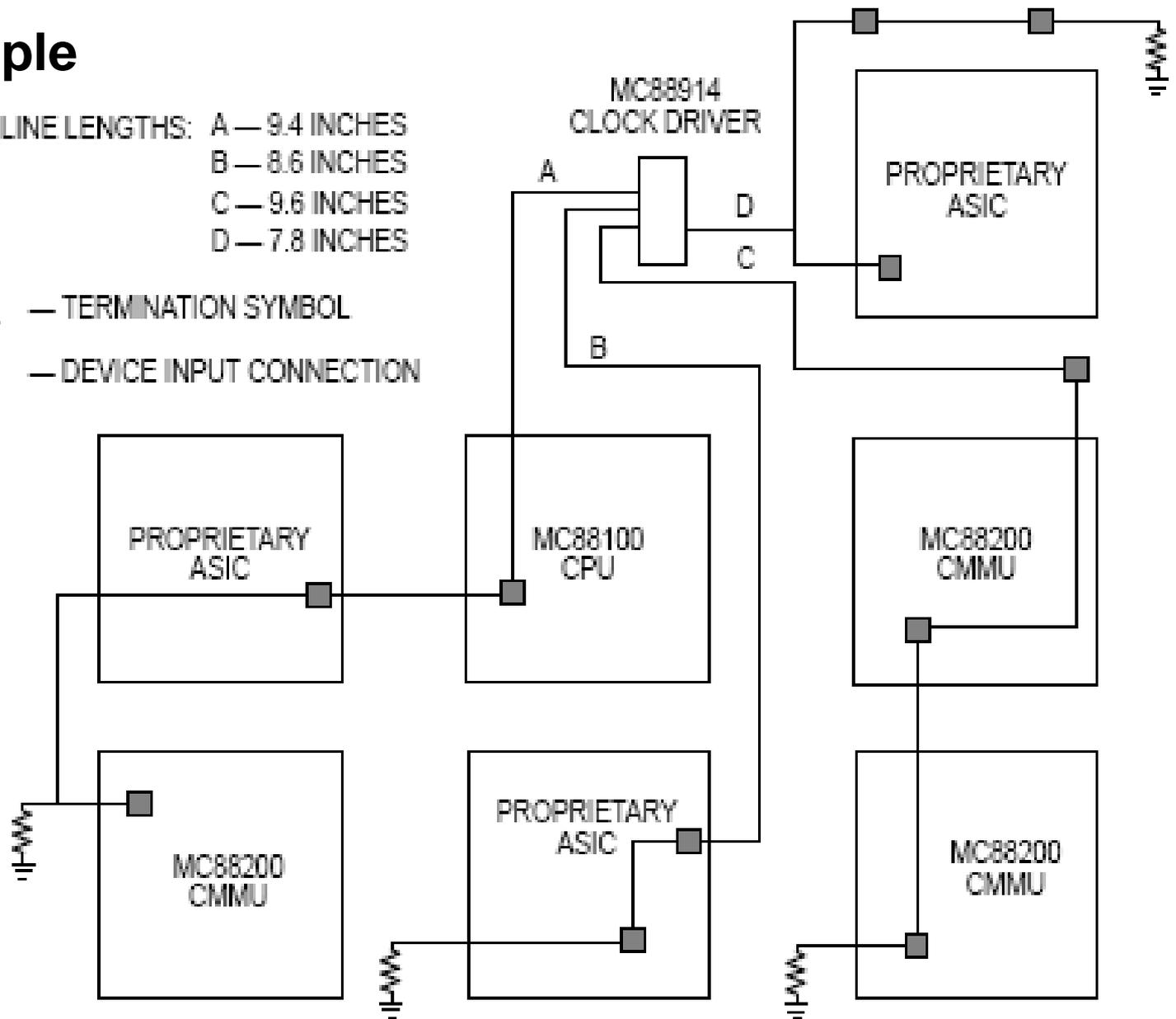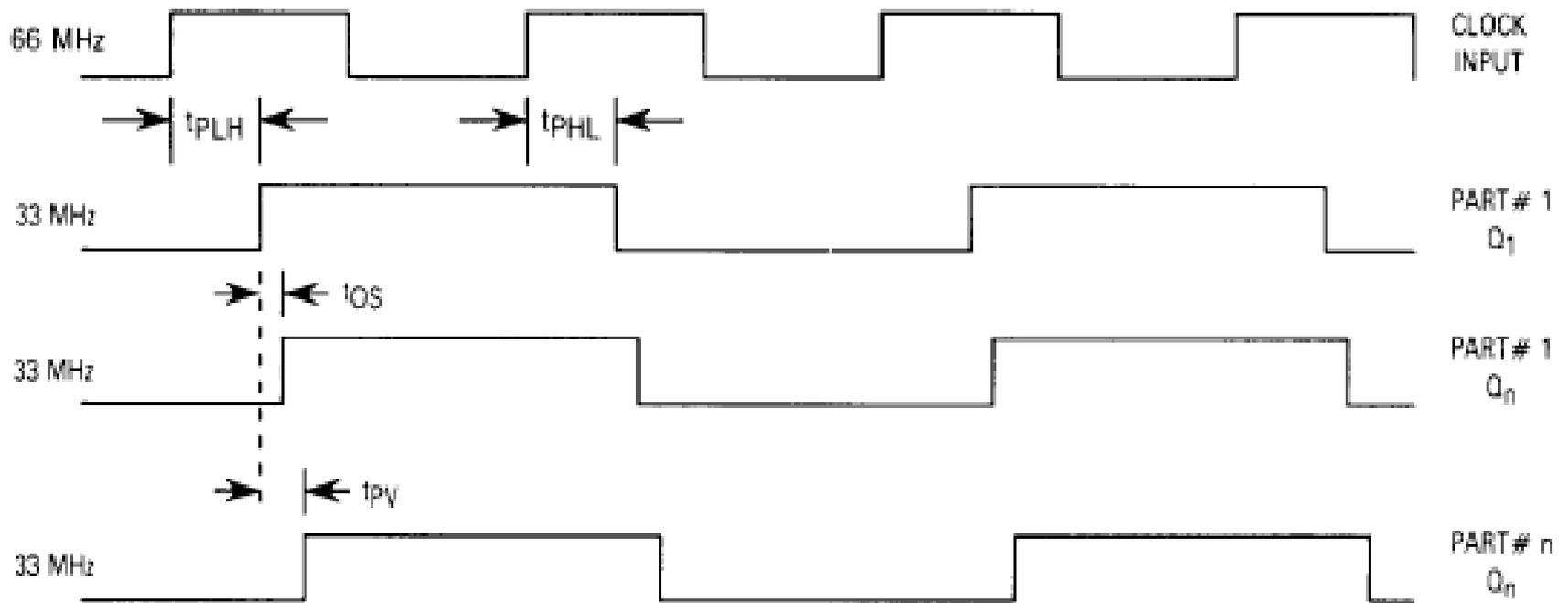
MC88200
CMMU

PROPRIETARY
ASIC

MC88200
CMMU

Figure 2. Scale Representation of an Actual 88000 System PCB Layout
(Only sections of the board related to the clock driver outputs are shown.)

Skew

- One more problem (besides terminations, noise...): the *skew*, i.e. the *clock uncertainty*
- For what concerns the clock generation (see next page):

  - t_{PS} :difference between the high-to-low and low-to-high transition for a single output (pin): $|t_{PLH}\text{-}t_{PHL}|$

    - defines how close to a 50% duty cycle the clock is

    - easily made ~ 0 using a divider

  - t_{OS} :difference between the fastest and slowest propagation delays (any transition) *between the outputs of a single part*

  - t_{PV} :maximum propagation delay delta *between any given pin on any part,* due to parameters dispersion among the devices of the same type

- Then, there is the skew due to the PCB traces

66 MHz

t_{PLH} t_{PHL}

CLOCK INPUT

33 MHz

PART# 1
Q_1

t_{OS}

33 MHz

PART# 1
Q_n

t_{PV}

33 MHz

PART# n
Q_n

Notes: 1) t_{PS} measures $|t_{PLH} - t_{PHL}|$ for any single output on a part.
2) t_{OS} measures the maximum difference between any t_{PHL} or t_{PLH} between any output on a single part.
3) t_{PV} measures the maximum difference between any t_{PHL} or t_{PLH} between any output on any part.

Figure 1. Timing Diagram Depicting Clock Skew Specs Within One Part and Between Any Two Parts

Example

- Given
  - for the generator: clock at 33 MHz => T= 33 ns,

    t_{OS} < 1 ns (t_{PV} not needed, we have just one driver here)
  - for the PCB: Z_0=69.4 ohm, τ_{prop}=0.144 ns/in =>
    C_0= τ_{prop}/Z_0=2.075 pF/in
  - and with the loads: Z'_0=41 ohm, τ'_{prop}=0.243 ns/in
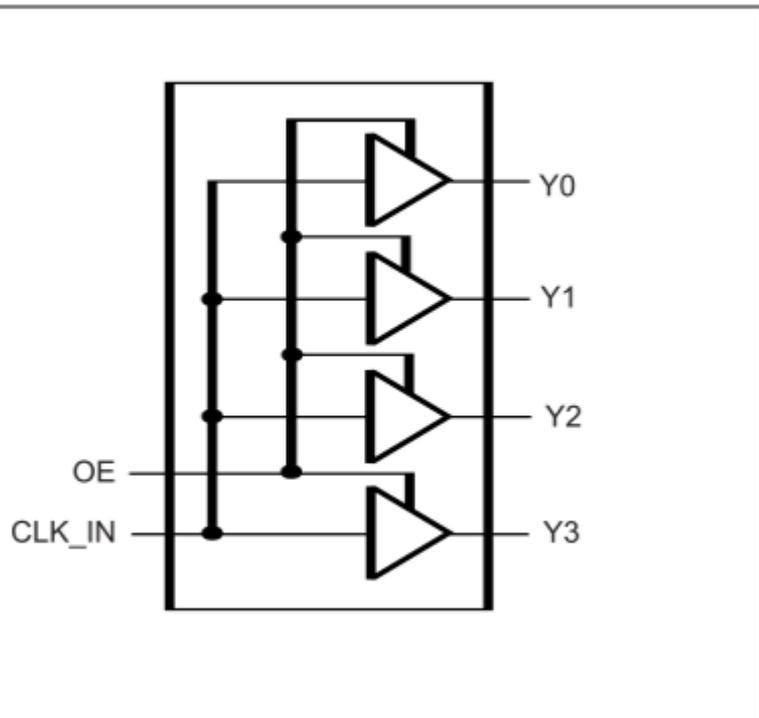- Maximum distance between any two MC88K devices on the same trace: 4.5 in => skew= 4.5*0.243=1.1 ns
- The two devices farthest away from the clock driver (trace a and c) are ~ the same distance -> neglectable skew (much less than t_{OS})
- Worst case: 1+1.1=2.1 ns (7% of the period)

Example

- PI6CV304: 160 MHz clock buffer

Block Diagram

Features

- 140MHz operation (PI6CV2304)
- 160 MHz operation (PI6CV304)
- Low noise, low skew: 150ps max
- Fast rise/fall time: 1.0ns typ.
- Fast propagation delay: 2.0ns typ.
- 5V I/O tolerant input
- Industrial temperature ($-40°C$ to $85°C$)
- 3.3V power supply
- Packaging (Pb-free & Green available)
 - 8-pin TSSOP (L)
  - 8-pin SOIC (W)

Example

- Si5340/1: Low-Jitter, 10 or 4-Output, Any-Frequency, Any-Output Clock Generator
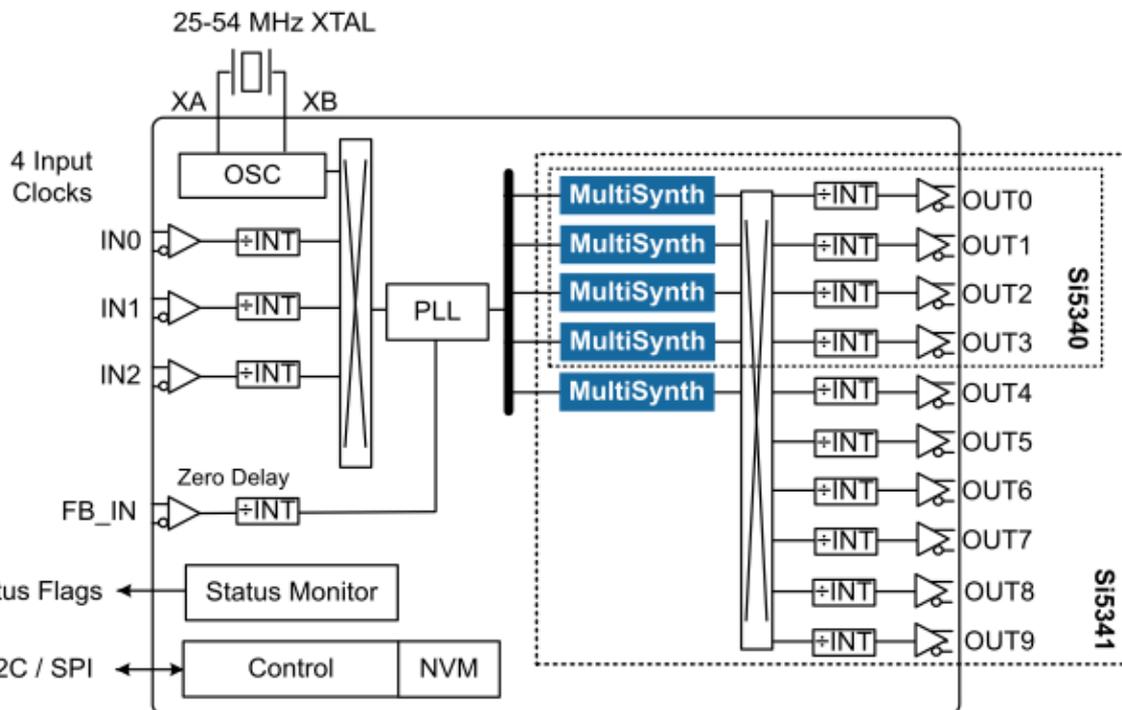
KEY FEATURES

- Generates any combination of output frequencies from any input frequency
- Ultra-low jitter of 90 fs rms
- Input frequency range:
  - External crystal: 25 to 54 MHz
  - Differential clock: 10 to 750 MHz
  - LVCMOS clock: 10 to 250 MHz
- Output frequency range:
  - Differential: 100 Hz to 1028 MHz
  - LVCMOS: 100 Hz to 250 MHz
- Highly configurable outputs compatible with LVDS, LVPECL, LVCMOS, CML, and HCSL with programmable signal amplitude
- Si5341: 4 input, 10 output, 64-QFN 9x9 mm
- Si5340: 4 input, 4 output, 44-QFN 7x7 mm

Terminations
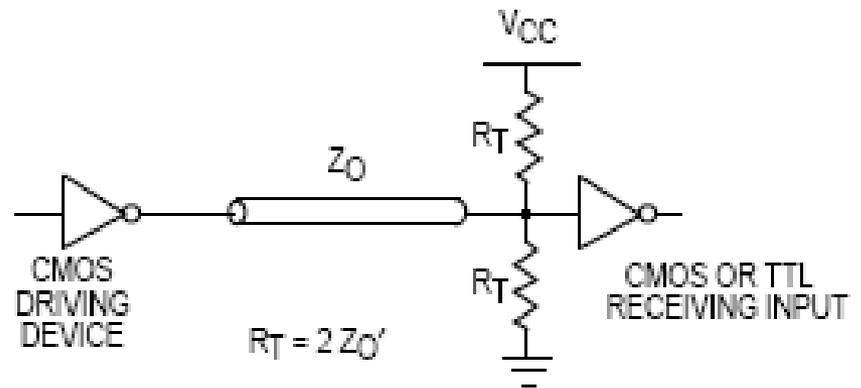
D. TRANSMISSION LINE WITH THEVENIN TERMINATION

- Series: if there is only one load (*not realistic for a clock signal...*)
- parallel: not recommended, "pushes" towards GND
- Thevenin: recommended (power consumption is not a problem: clock always exists -> consumption is mainly in AC)
- AC: so and so, "the waveform walks out slightly toward the end of the transition"

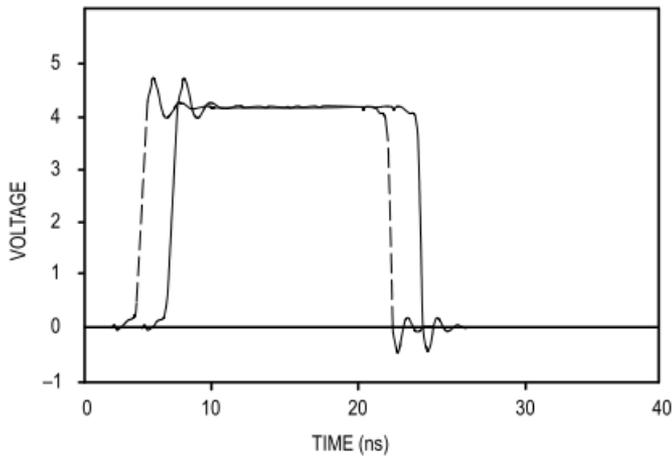# Terminations

A. SERIES TERMINATION
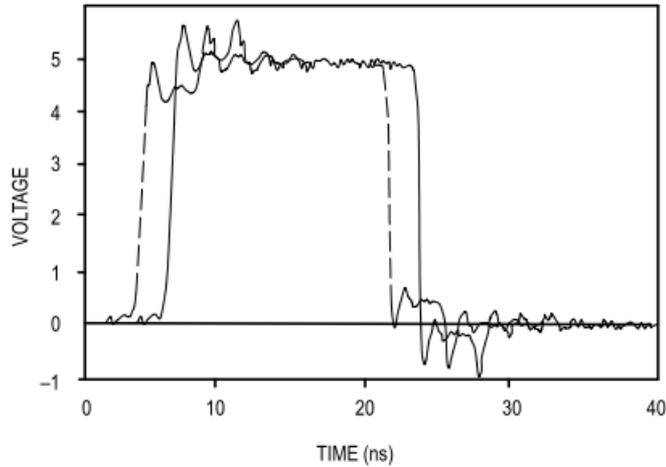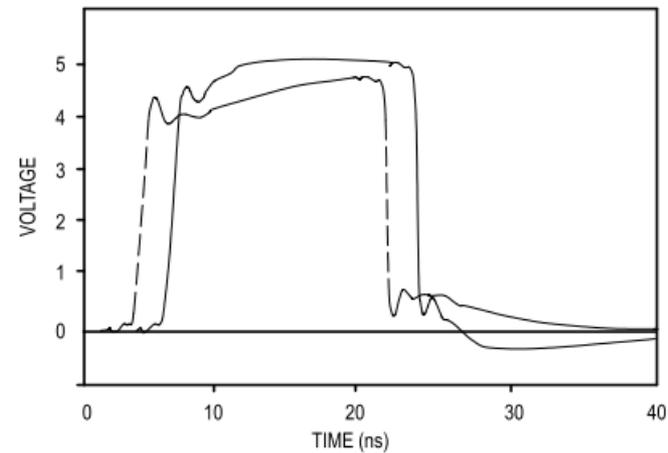
B. PARALLEL TERMINATION
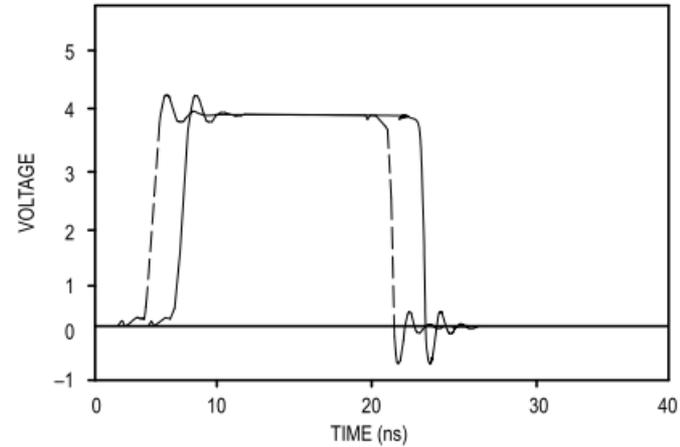
DRIVER OUTPUT WAVEFORM

RECEIVER INPUT WAVEFORM

C. THEVENIN TERMINATION

D. AC TERMINATION

Clock: phase alignment

- Clock-data recovery (CDR) transceiver implementations combine clock and data into a single signal
- alternatively, a number of chip-to-chip interface standards are source-synchronous, i.e. require a separate clock
  - for these source-synchronous interfaces, keeping clock and data signals in phase can be difficult due to board- and device-level effects:
    - skew (difference in arrival time of bits transmitted at the same time)
    - jitter (deviation from the ideal timing of an event)
    - noise

Clock: phase alignment

Sources of Skew, Noise, & Jitter in a Digital System

Transmission Output	←	Clock-Data Skew PVT & Parasitic Skew *Clock Jitter* *Duty Cycle Distortion* *Data Dependent Jitter*

Trace Length Mismatch Parasitic Capacitances *Data Jitter/Noise* *Clock Jitter/Noise*	→	Board

Static Effects
Dynamic Effects

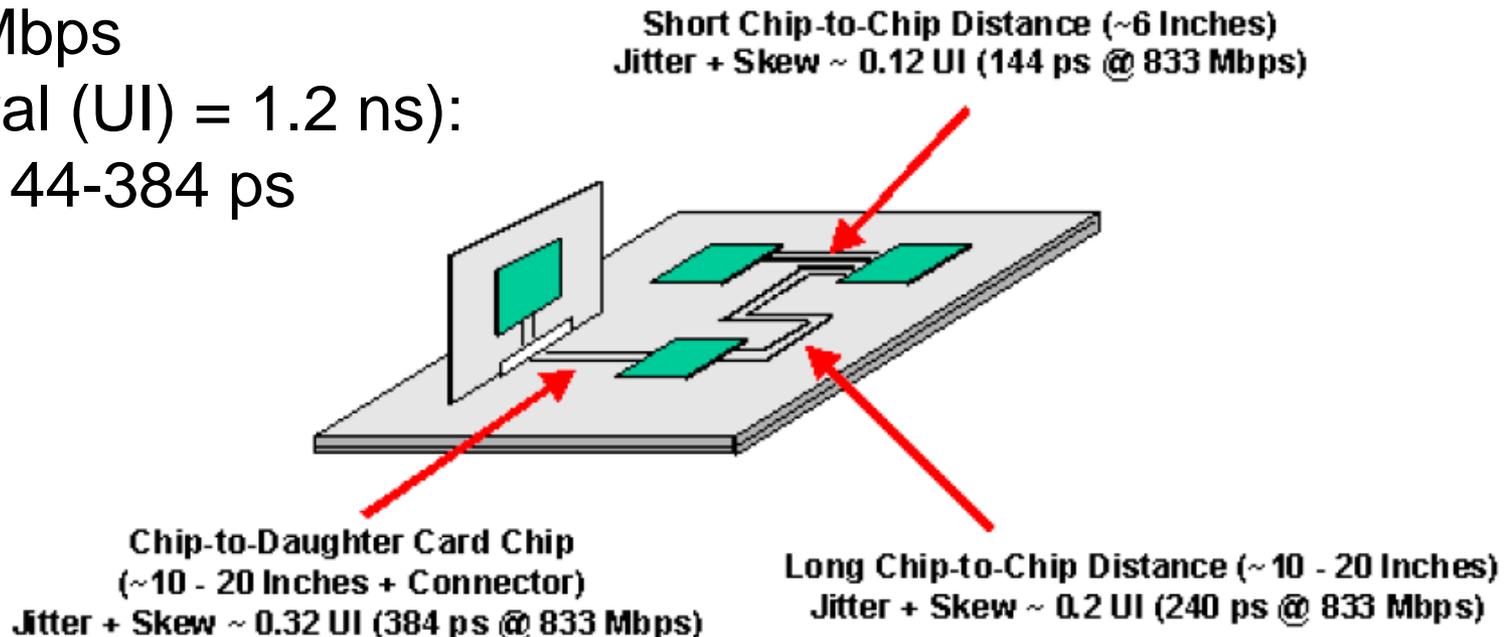| Receiver Sampling Window	←	Sampling Error PVT & Parasitic Skew Clock Skew *Duty Cycle Distortion* *Data Dependent Jitter*
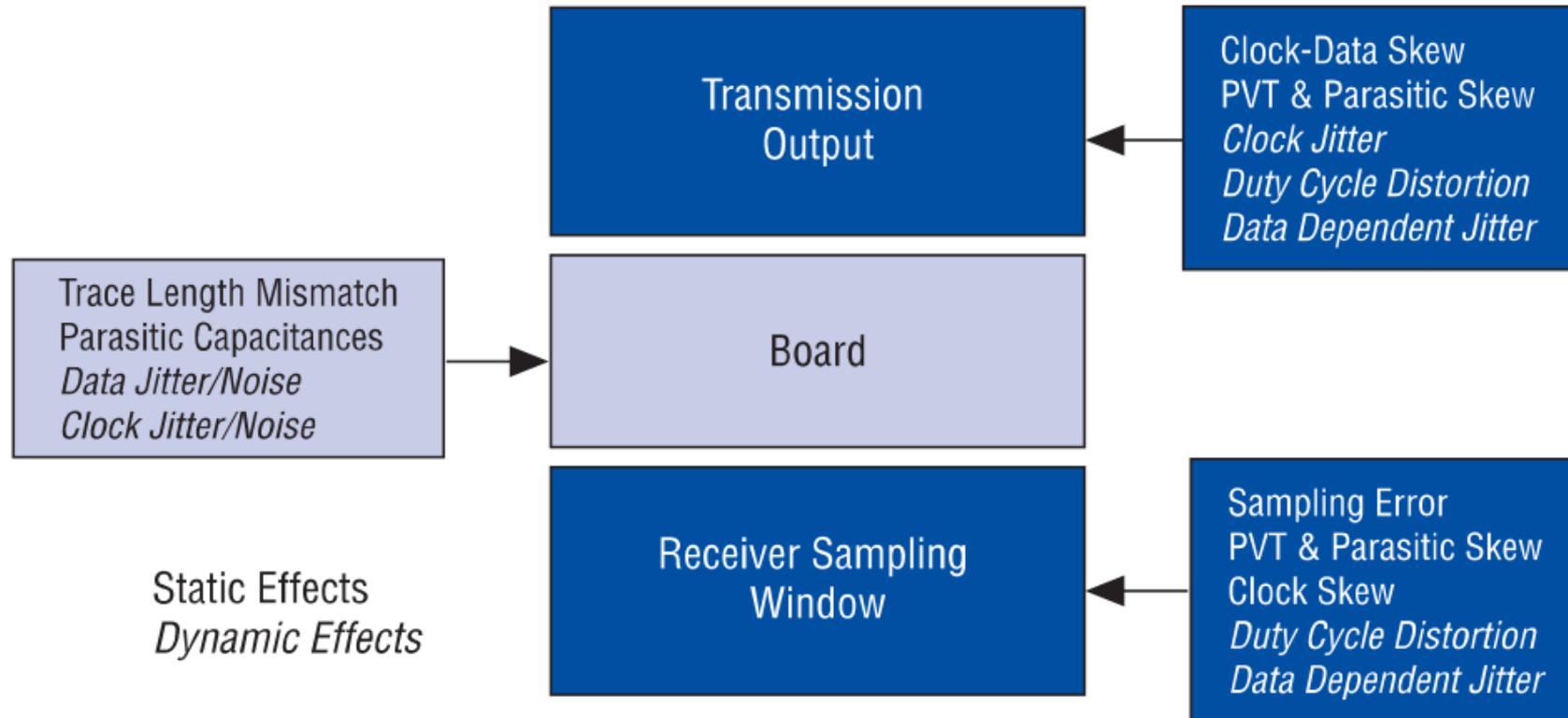
Clock: phase alignment

- Several methods exist for reducing or eliminating the effects of skew, jitter, and noise via *static phase alignment*
  - matching of clock and data traces length during board layout
  - accurate analog simulation of the board
  - some IC's can shift clock phase by a fixed, or adjustable (at start-up), amount on transmit/receive side to align it with data
- These techniques do not protect against long-term variations in skew due to process, voltage, and temperature changes

Clock: phase alignment

- Static phase alignment methods is insufficient for higher-speed designs (≥700 Mbps)
- increased clock frequencies reduced the data window ("eye") for setup times => it is difficult to maintain reliable operation
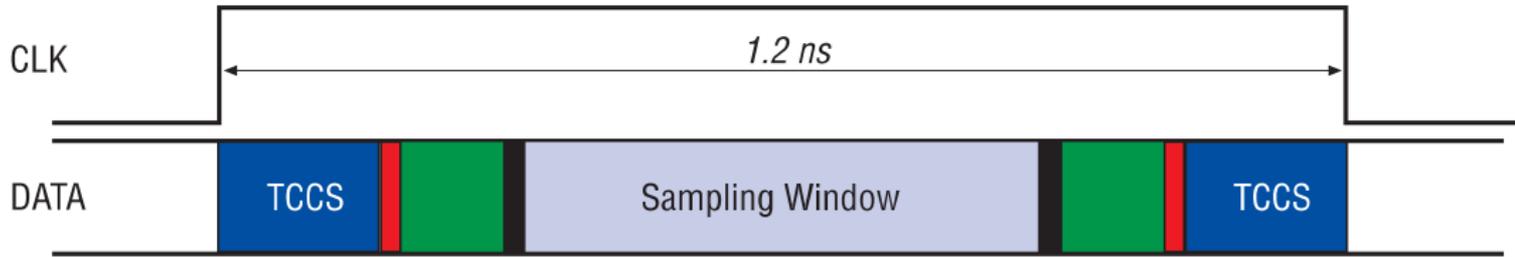
Quantifying Skew & Jitter in a Typical System

E.g., for 833 Mbps
(i.e. unit interval (UI) = 1.2 ns):
jitter+skew ≈ 144-384 ps

Short Chip-to-Chip Distance (~6 Inches)
Jitter + Skew ~ 0.12 UI (144 ps @ 833 Mbps)

Chip-to-Daughter Card Chip
(~10 - 20 Inches + Connector)
Jitter + Skew ~ 0.32 UI (384 ps @ 833 Mbps)

Long Chip-to-Chip Distance (~10 - 20 Inches)
Jitter + Skew ~ 0.2 UI (240 ps @ 833 Mbps)

Clock: phase alignment

Timing Budget Analysis of 833-Mbps System

CLK — 1.2 ns

DATA — TCCS | Sampling Window | TCCS

■ Blue	Transmit Channel-to-Channel Skew (TCCS)	≈ 400 ps
■ Red	Clock Duty Cycle Distortion	≈ 50 ps
■ Black	PLL Output Jitter	≈ 40 ps
■ Light blue	Sampling Window	≈ 440 ps
■ Green	Allowance for Board Skew	

Only 270 ps left for board skew: not enough!

Clock: phase alignment

- *Dynamic phase alignment* (DPA) technology has been developed to address the inadequacies of static phase alignment methods
- devices actively respond to changes in operational board skew
  - they continuously check the incoming data and adjust the phase of the clock to align with it
- DPA circuitry relies on transitions in data stream in order to adjust clock phase
  - during long run lengths in which the data do not change, DPA circuitry remains locked on the last chosen phase