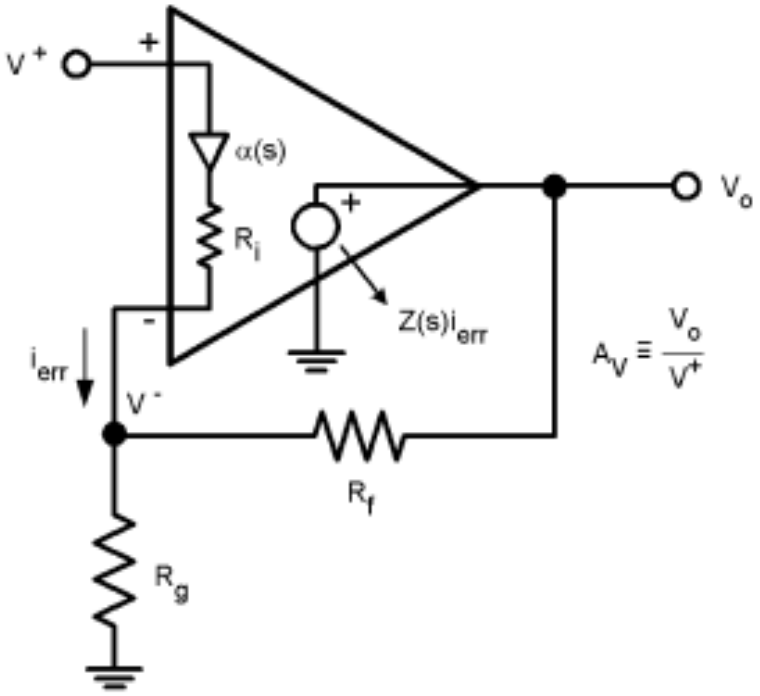
CFA3

[OA-13, AD_faq_ask23, OA-30, OA-07]

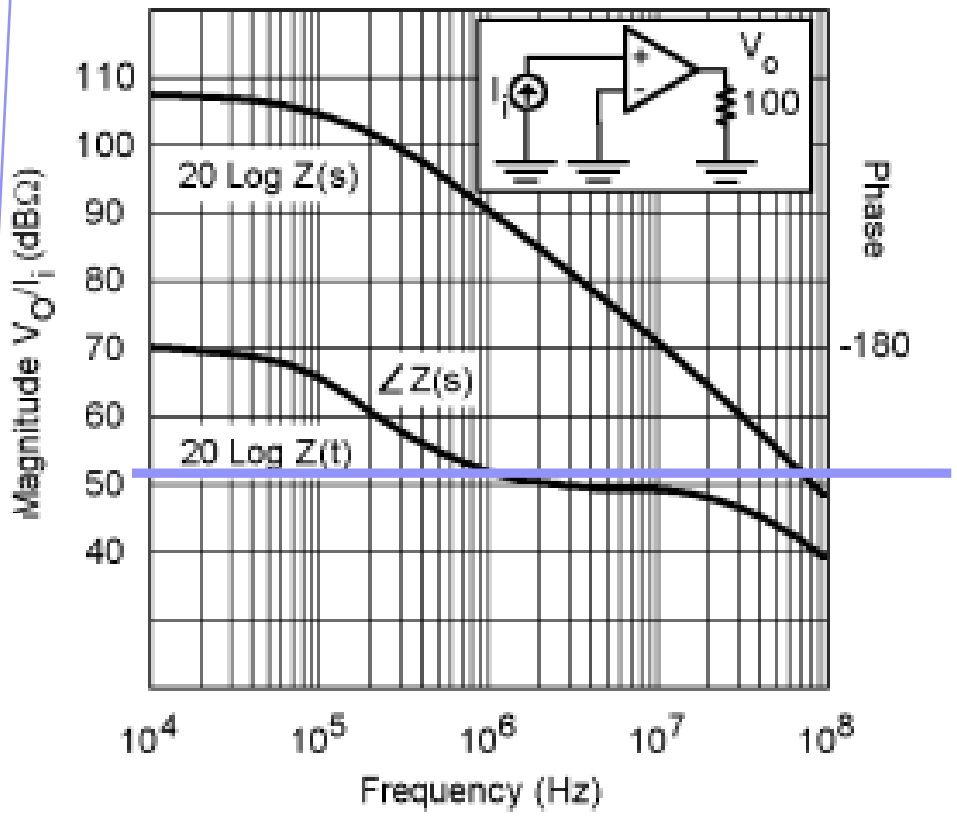
Understanding the loop gain [OA-13]



CLC400: in nominal conditions

- R_f=R_g=250 Ω, A_v=2; R_i=50 Ω
- Z_t=250+50*2=350 Ω ~ 50.9 dB

  Z_t here is the name of the "old" Z_2
- [or R_i=40 Ω -> Z_t=330]



$$\text{Hence, Loop Gain (LG)} = \frac{Z(s)}{R_f + R_i\left(1 + \frac{R_f}{R_g}\right)}$$

$$= \frac{\text{internal forward transimpedance}}{\text{feedback transimpedance}}$$

Understanding the loop gain [OA-13]

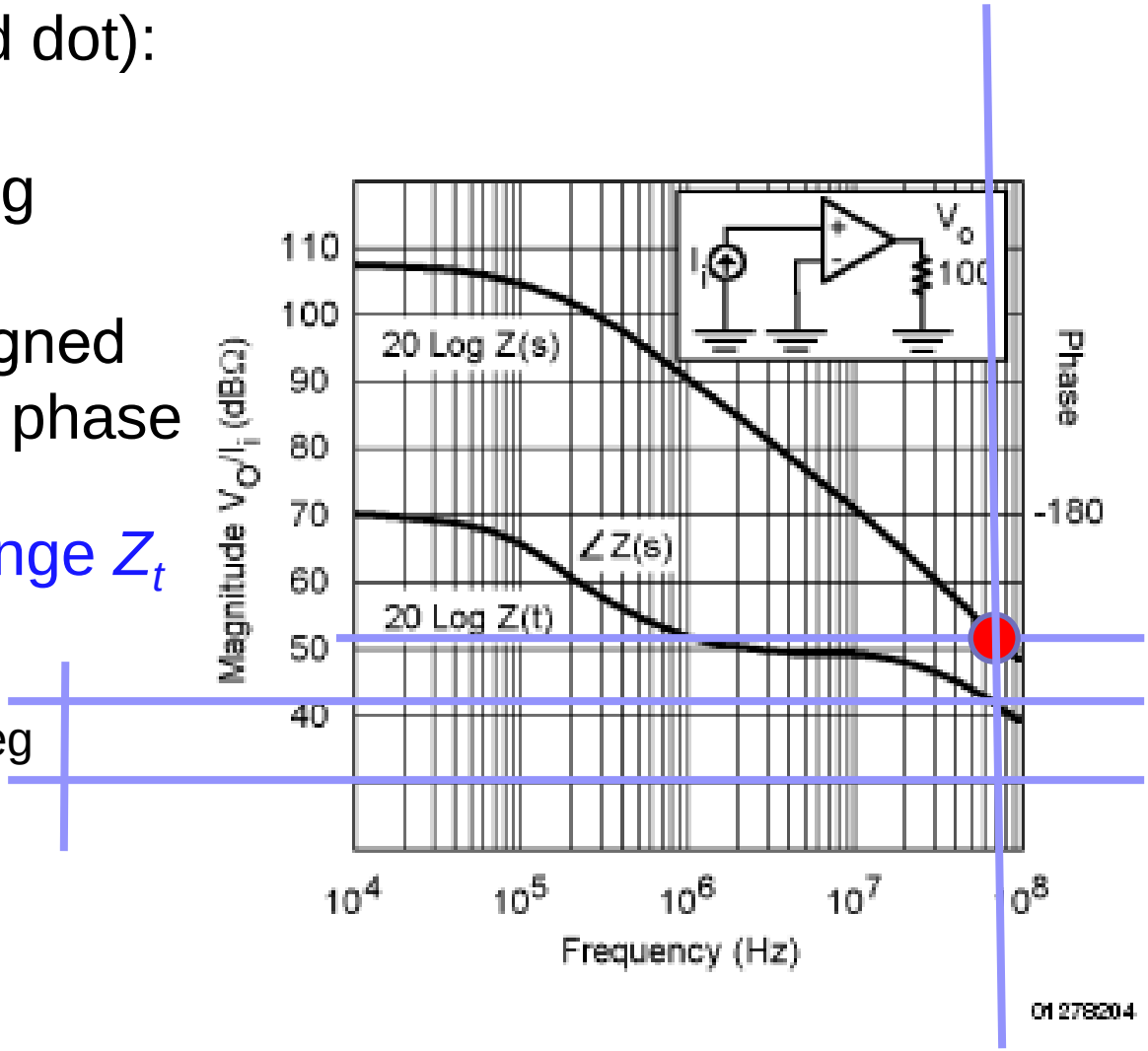
*

Where loop gain = 1 (red dot):

- arg(-*Z*)~-300
- phase margin ~ 60 deg

CFA's are normally designed to work with at least that phase margin ->

it is advisable *not* to change Z_t



approx. 60 deg

Controlling the loop gain

If a different A_v from the nominal one is need?
Try to use the optimal *feedback transimpedance* Z^*_t

- Using the nominal values, compute Z^*_t

$$R_f + R_i\,(1 + R_f/R_g) = Z_t^*$$

- For the desired A_v , compute R_f

$$R_f = Z_t^* - R_i A_v$$

- and finally get R_g from

$$A_v = 1 + R_f/R_g$$

  - e.g, for the CLC400, Z^*_t=250+50*2=350 Ω
  - e.g, for the CLC406, Z^*_t=500+60*6=860 Ω

(from OA13)

TABLE 1. Comlinear Monolithic, Current Feedback, Amplifier Optimum Feedback Transimpedance and Operating Point Information

Part #	Design Point Information				Operating Current		comments
	A_v	R_f (Ω)	R_I (Ω)	Z_t* (Ω)	I_c (mA)	I_c/I_{cc}	
CLC400	+2	250	40	330	.67	.045	
CLC401	+20	1500	50	2500	.52	.035	
CLC402	+2	250	16	282	.82	.055	
CLC404	+6	500	30	680	.87	.080	
CLC406	+6	500	60	860	.43	.09	
CLC409	+2	250	25	300	1.05	.08	
CLC410	+2	250	35	320	.74	.05	disable left open
CLC411	+2	301	50	400	.52	.05	disable left open
CLC414	+6	500	250	2000	.105	.05	each amplifier of quad
CLC415	+6	500	60	860	.43	.09	each amplifier of quad
CLC430	+2	750	60	870	.43	.04	disable left open
CLC500	+2	250	32	314	.82	.05	
CLC501	+20	1500	30	2100	.86	.05	see (Note 3)
CLC505	+6	1000	50	1300	.52	.06	I_{cc} = 9.0mA R_p = 33kΩ
CLC505	+6	1000	150	1900	.175	.06	I_{cc} = 3.3mA R_p = 33kΩ
CLC505	+6	1000	490	3950	.053	.06	I_{cc} = 1.0mA R_p = 33kΩ

Note 1: Power supplies at ±5V

Note 2: 25°C temperature assumed: yields kT/q = .26V

Note 3: CLC501 specification point at A_v = +32, R_f = 1500Ω Design point, however is at A_v = +20, R_f = 1500Ω

Controlling the loop gain

This example: for the CLC 404

- nominal values are

  A_v=+6

  R_f=500 Ω

  R_i=30 Ω

- so that (A_v=2, 6, 11)

  Z_t^*=500+30*6=680 Ω

  (above): with fixed R_f

  (below) with $Z_t = Z^*_t$: better!

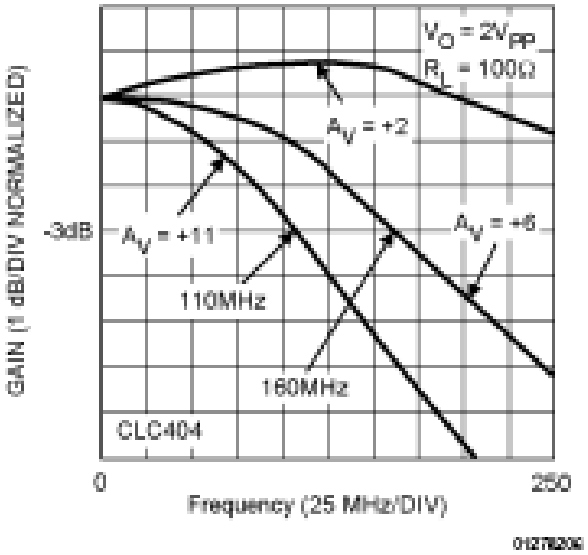


FIGURE 4. Frequency Response vs. Gain for R_f Fixed = 500Ω

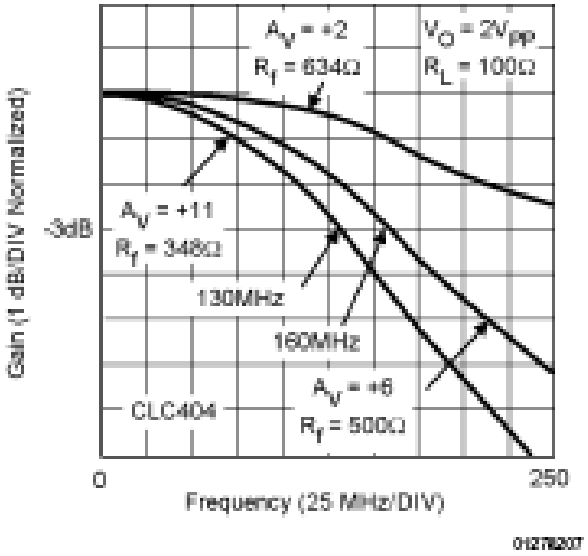
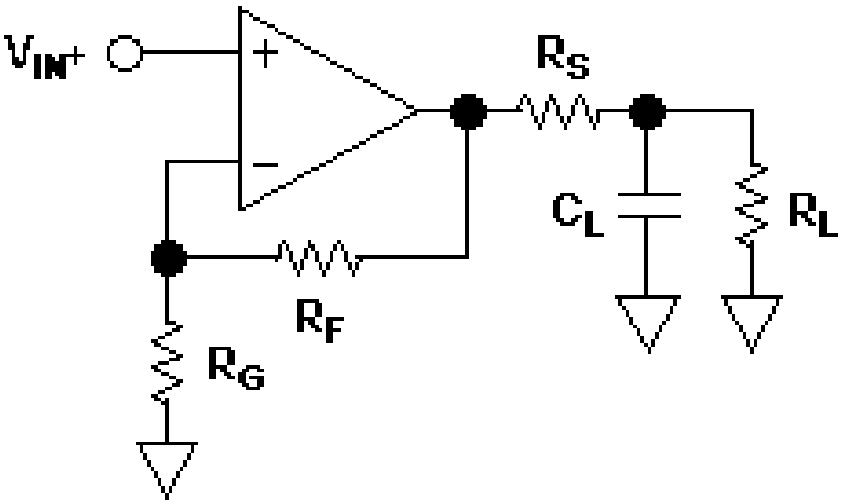


FIGURE 5. Frequency Response vs. Gain for Fixed Z_t = Z_t^* = 680Ω

To drive a capacitive load [AD_faq/ask2, p. 2.9]

- A capacitor on the output increases the phase -> possible instability.
- The easiest solution:

  - resistor in series



VFA / CFA comparison [OA-30]

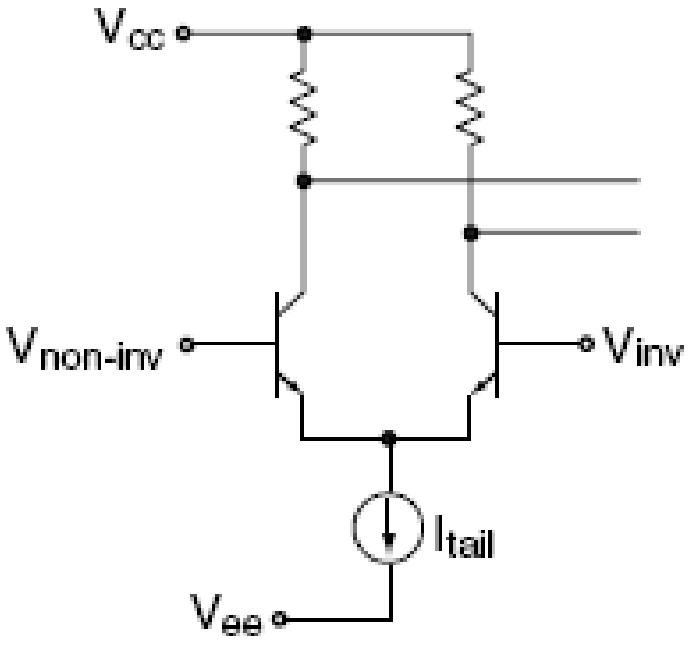


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FIGURE 5. Typical VFB Input Stage

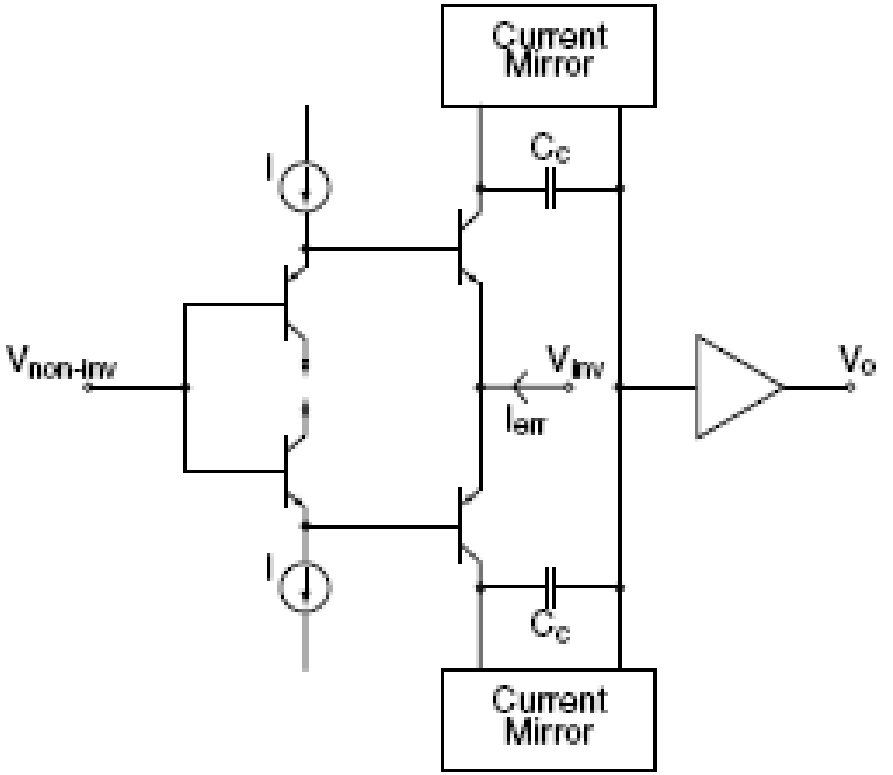

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FIGURE 7. Basic CFB Topology

VFA / CFA comparison [OA-30]

- Normally, the input stage of a VFB is a differential stage -> two equally biased, matched transistors -> error compensation ->

  - low input offest voltage V_{io}
  - matched input bias current I_b
  - high PSRR
  - good CMRR

Moreover, lower noise and feedback freedom

VFA / CFA comparison [OA-30]

- Normally, the CFA input stage is a push-pull stage -> an NPN and a PNP -> no matching ->

  - higher V_{io}
  - unmatched I_b
  - worse PSRR and CMRR
  - higher noise; limited feedback freedom

CFA

- No gain-bandwidth trade-off
- Often, the CFA is simpler (an input buffer, a gain stage and an output buffer) -> fewer stages -> faster
- *I* in *C* is not limited -> no slew rate limitation, apart from

  - saturation effects [AD_faq/ask1, p. 2.9]

  - transistor current gain degradation at high current levels [AN-NS92, p. 5.b.6]

  - capacitive effects

Some modern VFAs (e.g. AD9632) have similar characteristics

CFA

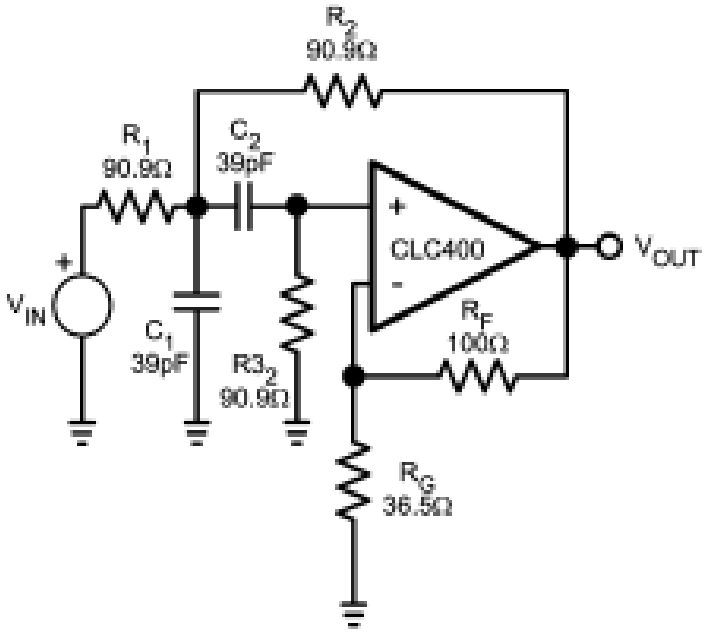
- Distortions are normally due to asymmetries and limited speed

  - complementary symmetry -> lower distortion

  - being faster, at high speed the loop gain is higher -> lower distortion

Application circuit guide

- see OA-07
- E.g.: high pass: KRC (i.e. Sallen-Key)



CFA params modeled by the National SPICE models [OA-18]

- **DC EFFECTS**
  - • V_{IO}, I_{BI}, I_{BN}
  - • Supply current vs. supply voltages
  - • Common mode input/output voltage range
  - • Load current from supplies
  - • CMRR
- **AC EFFECTS < 500 MHz**
  - • Frequency response vs. gain & load
  - • Open loop gain & phase
  - • Noise
  - • Small signal input/output impedance
- **TIME DOMAIN**
  - • Rise/fall times
  - • Slew rates
- **SPECIAL FEATURES (WHERE APPLICABLE)**
  - • Output clamping
  - • Supply current adjustment
  - • Offset voltage adjust
  - • Disable/enable times
  - • External compensation

CFA parameters *not* modeled by the National SPICE models

- • Differential gain and phase
- • PSRR
- • Harmonic distortion
- • Fine scale settling performance
- • Thermal tail

LMH6714

- Suggested operation: A_V=+2, R_f=300 Ω
- see data sheets...
- R_i ~ 180 Ω
- slew rate: 1800 V/us
- improved replacement for CLC 400, 401, 402, 404, 406
- suggested R_f values are provided for different values of A_V (p. 9, figure 2)
- for gains > 5 it behaves as a GBP limited OA

LT1206 and LT 1210

- High output current drive capability (250 mA and 1.1 A, resp.)
- stable with large capacitive load (up to 10 nF)
- suggested values of R_F and R_G are provided for different gains (and loads and power supply)

AD8009

- Ultrahigh speed current feedback amplifier with a phenomenal 5,500 V/ μ s slew rate
- suggested R_F also depends on the IC package!