Silicon Carbide:
Material and Power Devices

Tutorial Sponsored by EPSRC Centre of Power Electronics

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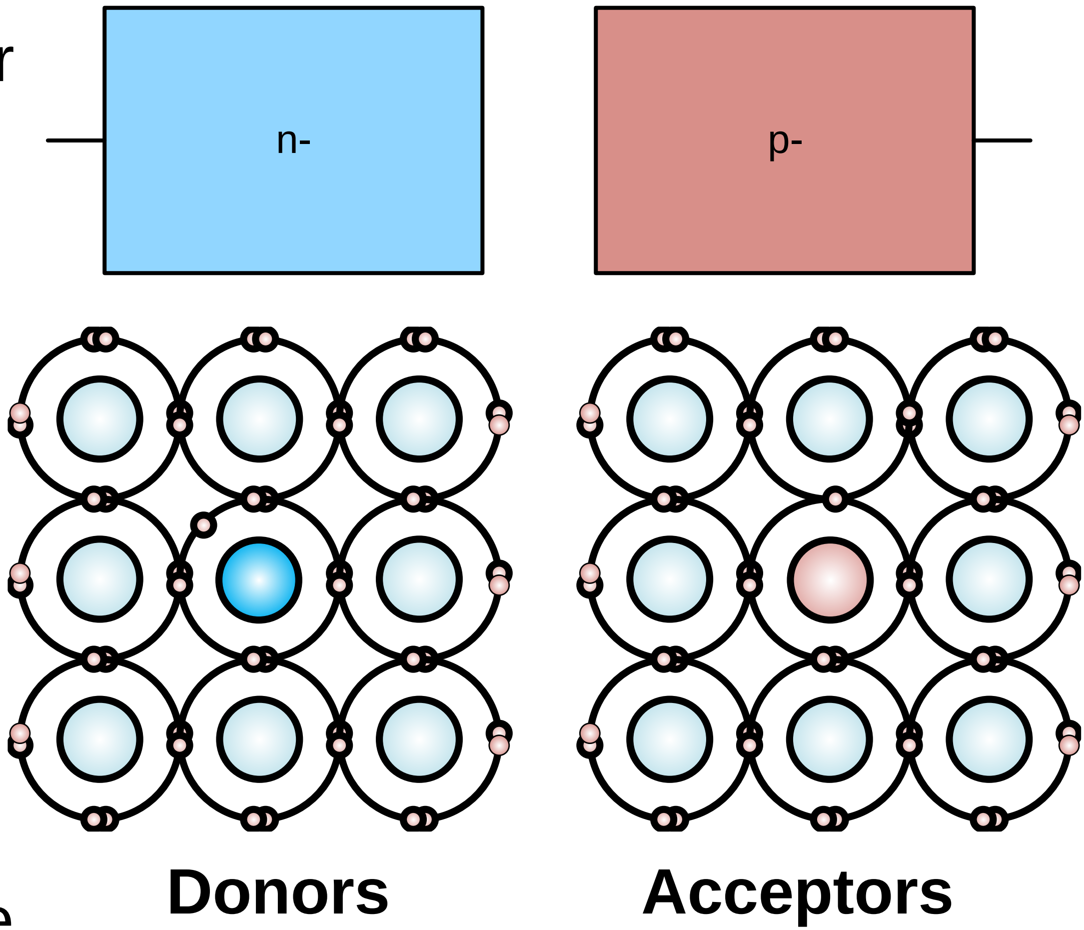
Semiconductor Devices: PN Junctions

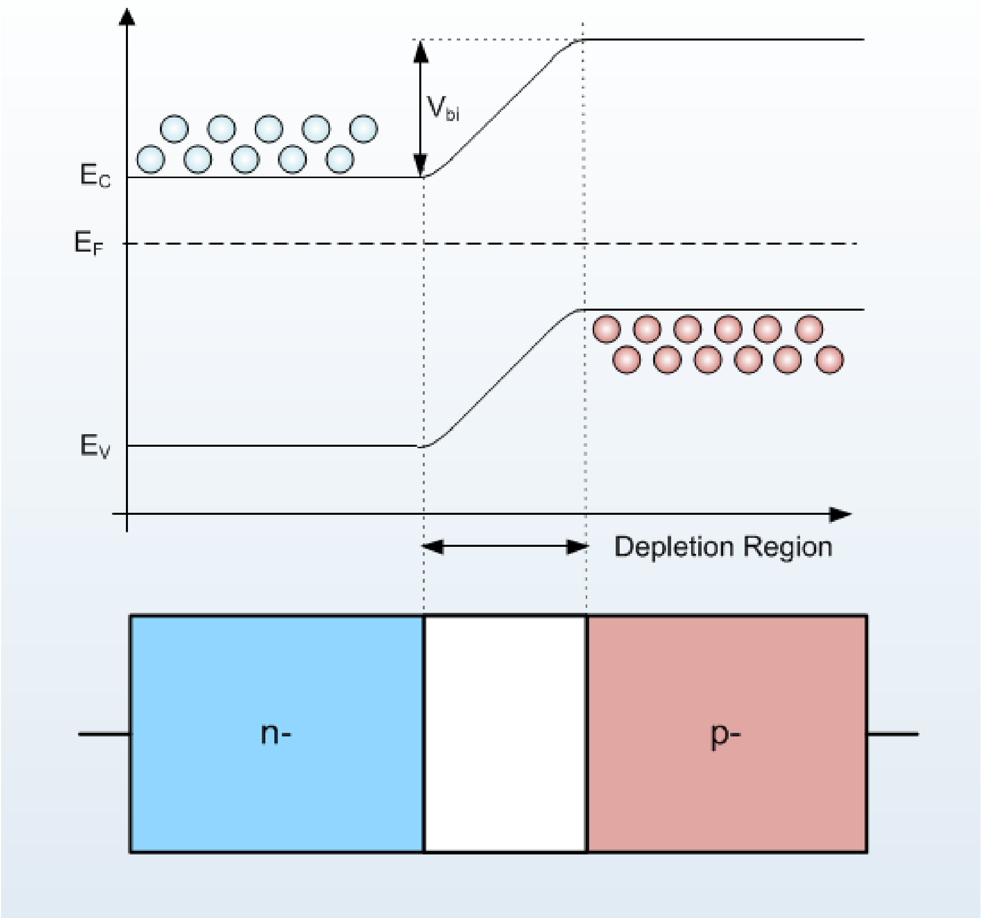
- Semiconductors are doped positive (p-type), or negative (n-type) by adding dopants.
- p-type dopants are typically boron, aluminium
- n-type dopants are typically nitrogen, phosphorous
- In power electronics, semiconductor devices are usually n-type as it has a higher electron mobility meaning a lower resistance is possible.



Semiconductor Devices: PN Junctions

- Bringing the p and n regions into contact, electrons and holes diffuse and recombine, forming a region at the interface that is ‘deplete’ of carriers.

- In steady state, a potential barrier (V_{bi}) exists at the depletion region that prevents carriers from diffusing across it.



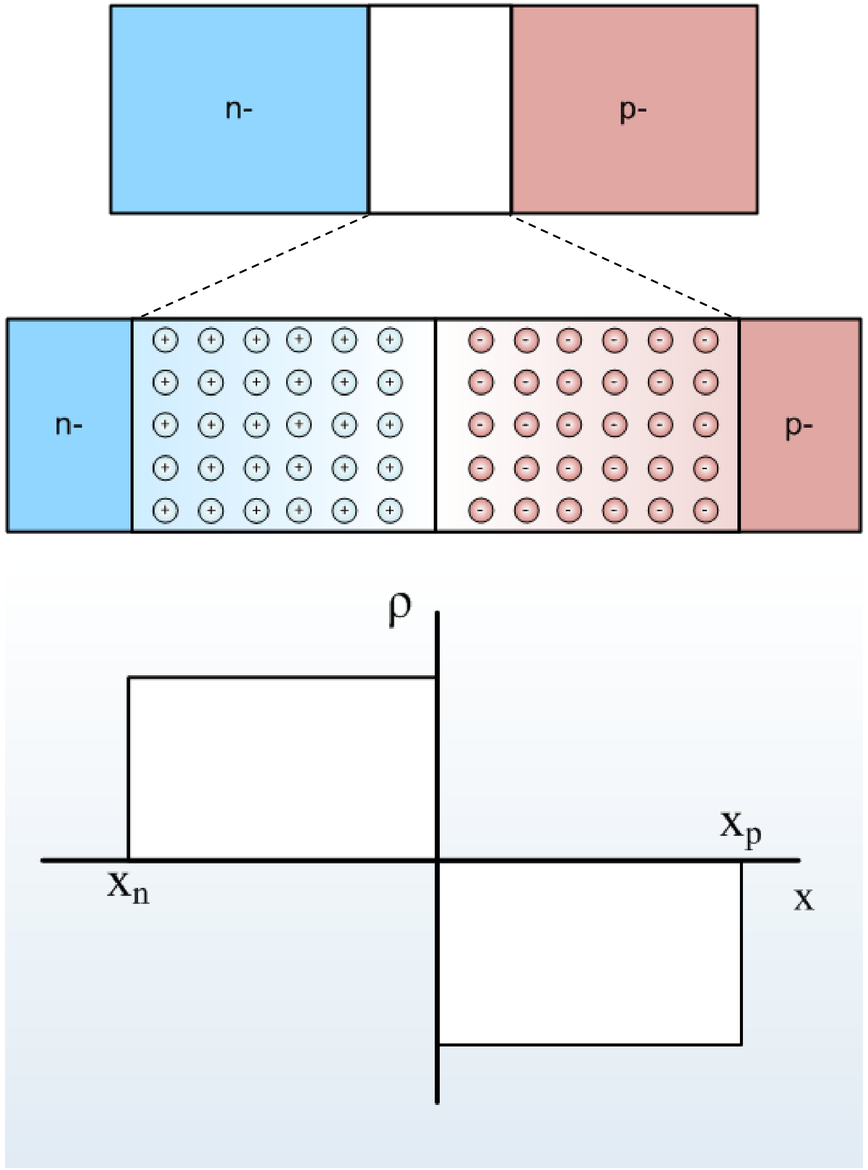
Semiconductor Devices: PN Junctions

In the depletion region between the p- and n-type regions, ionised dopants remain, free of their extra carrier. They have an associated *charge density* (ρ), given by:

$\rho = qN_D$ (Units = C/cm^3)

q = Charge of an electron, Coulombs

N_D = N-type doping, cm^{-3}



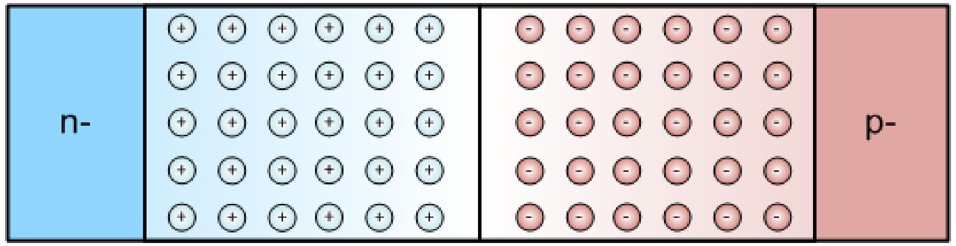
Semiconductor Devices: PN Junctions

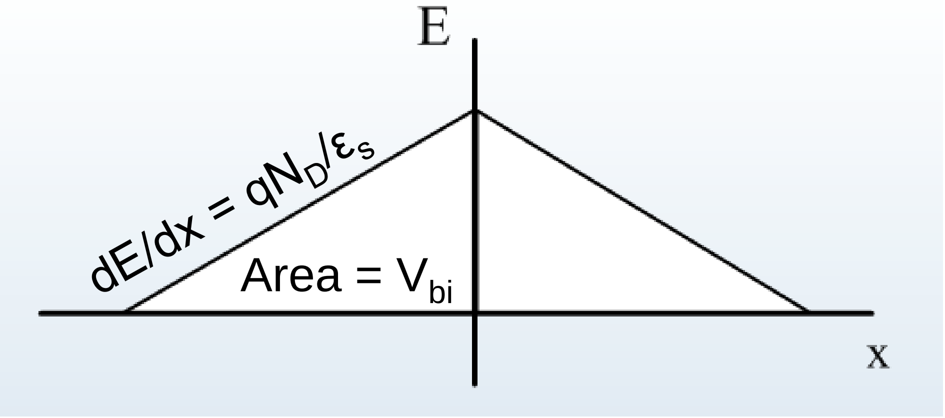
Knowing the amount of charge at the interface, we can learn the amount of force this exerts on carriers within the semiconductor.

This **electric field** (V/cm) is calculated from the charge density as follows:

$$\frac{dE}{dx} = \frac{\rho}{\varepsilon_s} = \frac{qN_D}{\varepsilon_s}$$

ε_s= Semiconductor Permittivity, F/cm





Semiconductor Devices: PN Junctions

The voltage dropped across the depletion region may be found as:

$$\frac{d^2V}{dx^2} = \frac{dE}{dx} = \frac{\rho}{\varepsilon_s} = \frac{qN_D}{\varepsilon_s}$$

V_{bi}, the **built-in potential**, will have to be overcome to turn on the device (~0.7 V in Si)

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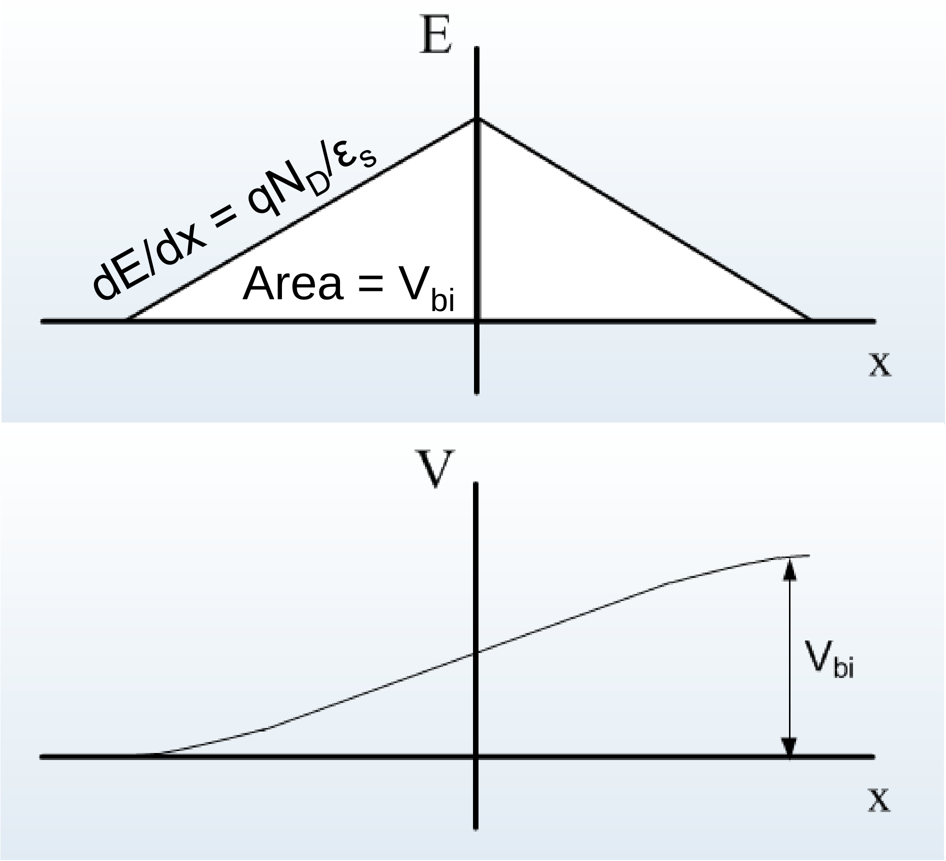

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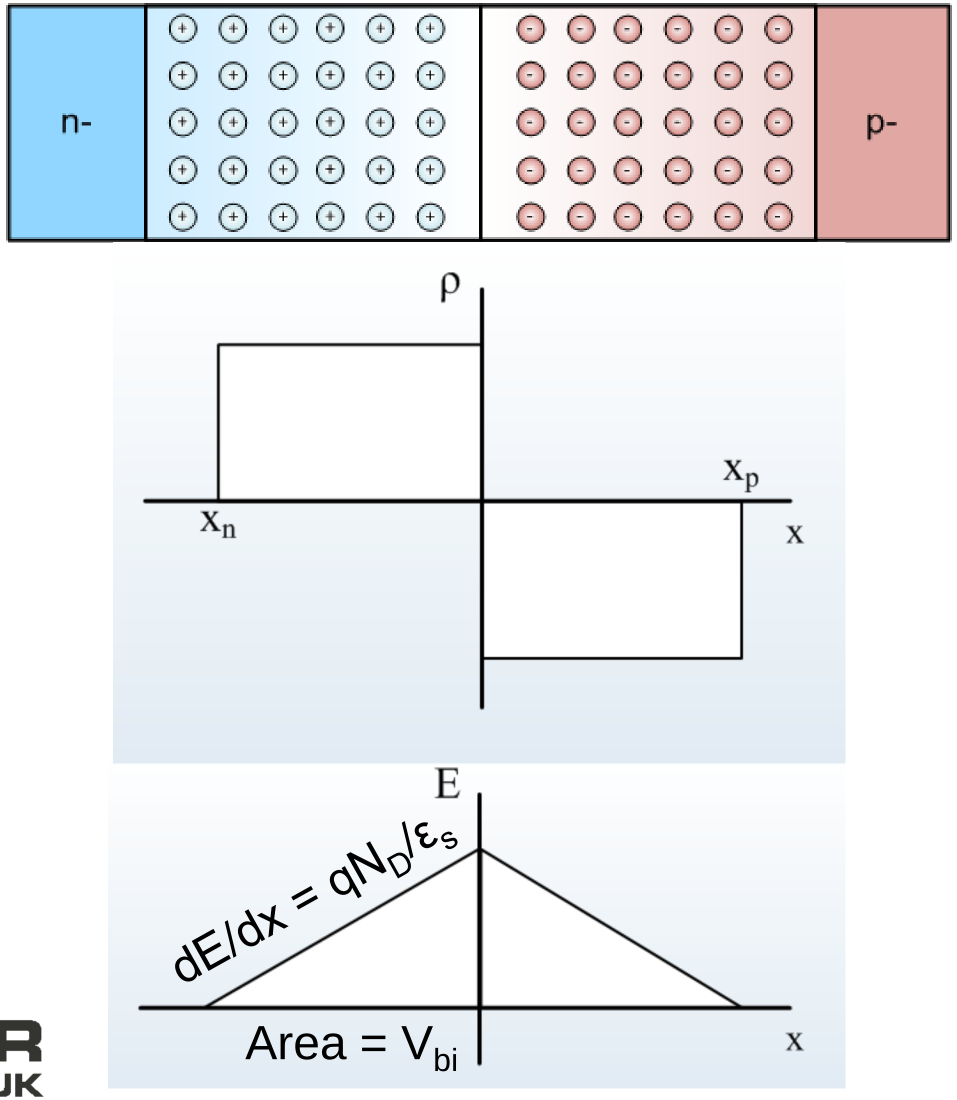
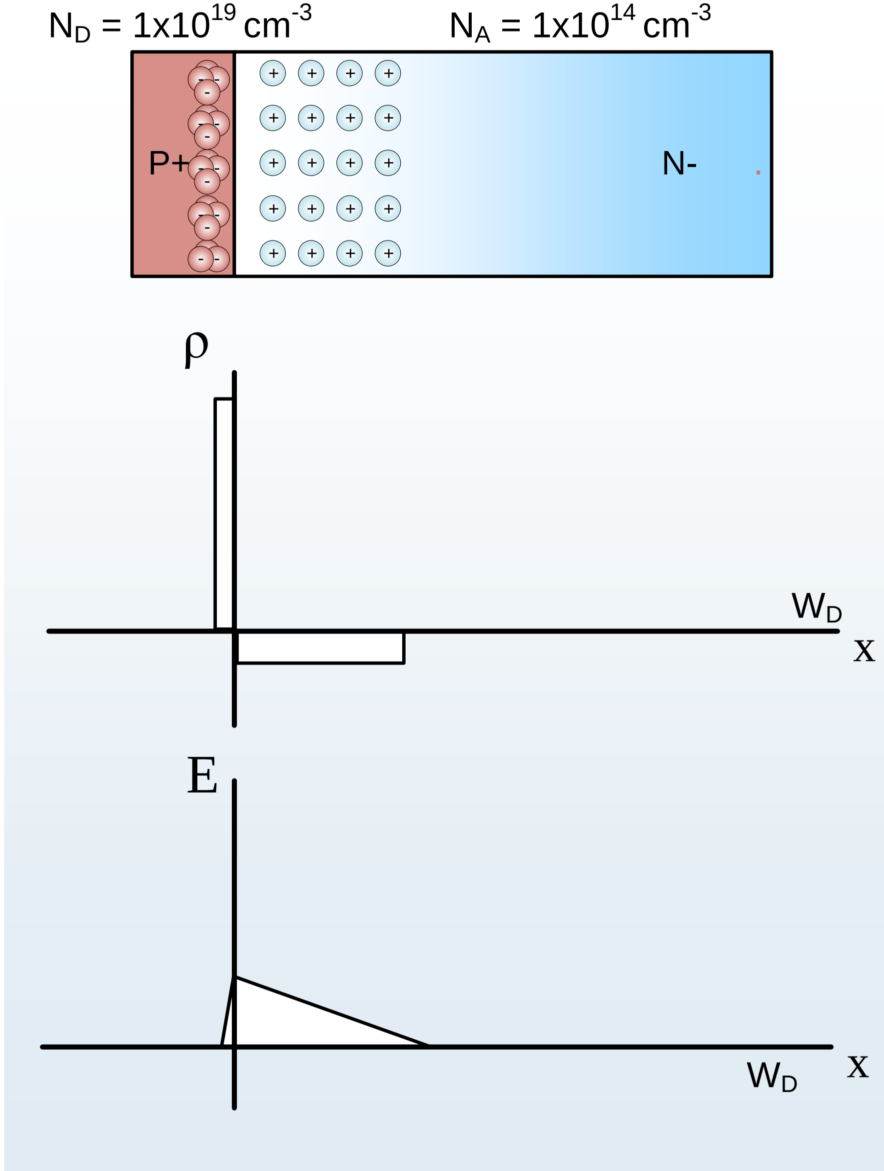
Semiconductor Devices: PN Junctions

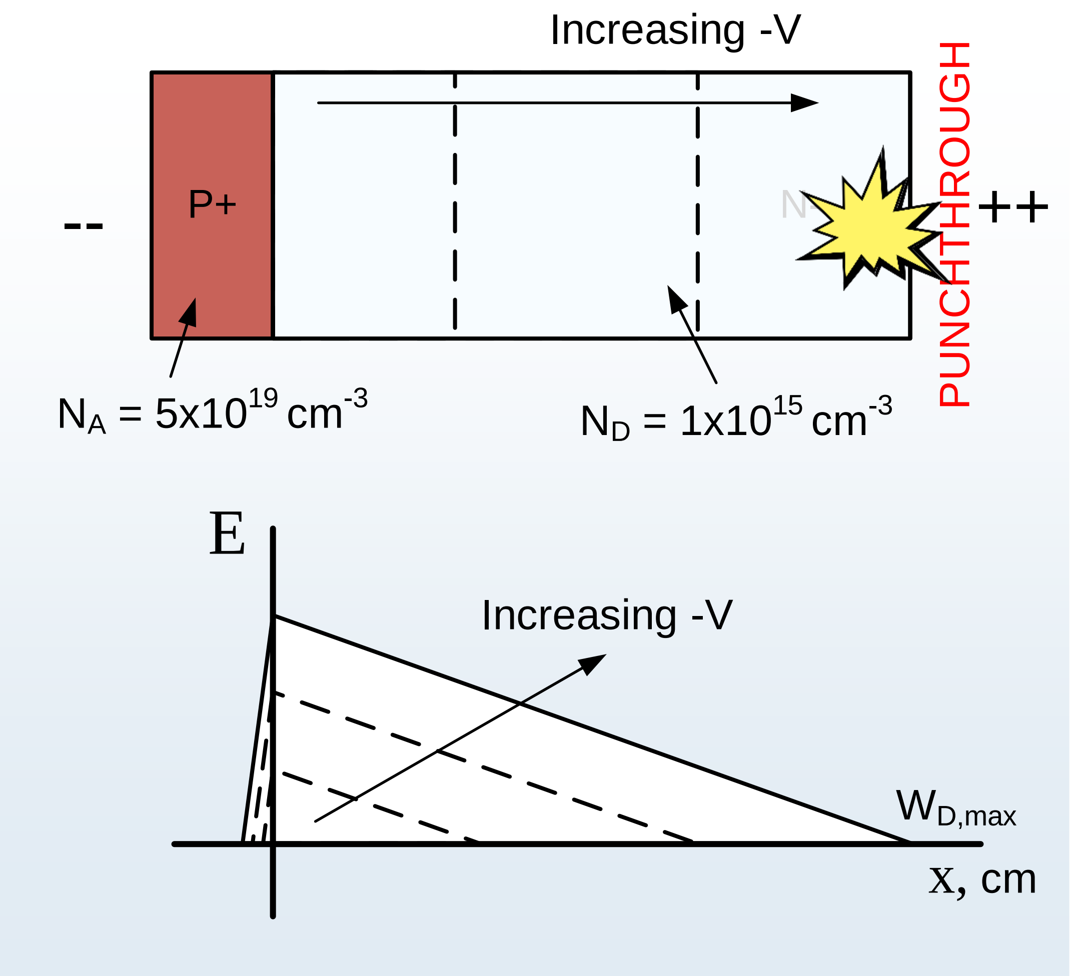




Semiconductor Devices: Diodes and Breakdown

- Reverse biasing a p-n junction extracts more electrons and holes n and p regions, widening the depletion region

- If the voltage is high enough the depletion region will punch through the entire drift region



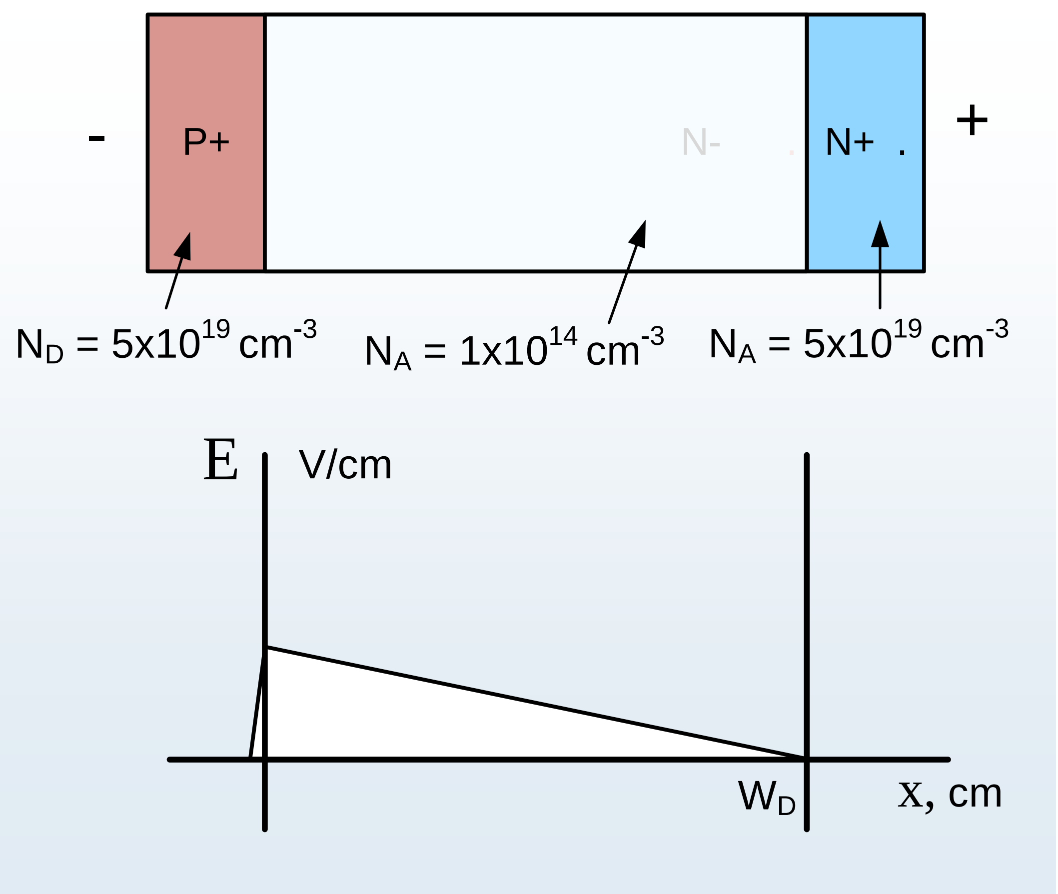
Semiconductor Devices: PiN Diodes

- In reality, punchthrough is easily prevented, and is not an issue in actual diodes (though it is in some IGBTs).

- Capping the p-region with a P+ region prevents the depletion region reaching the end of the device.

  A *PiN* structure is then formed.

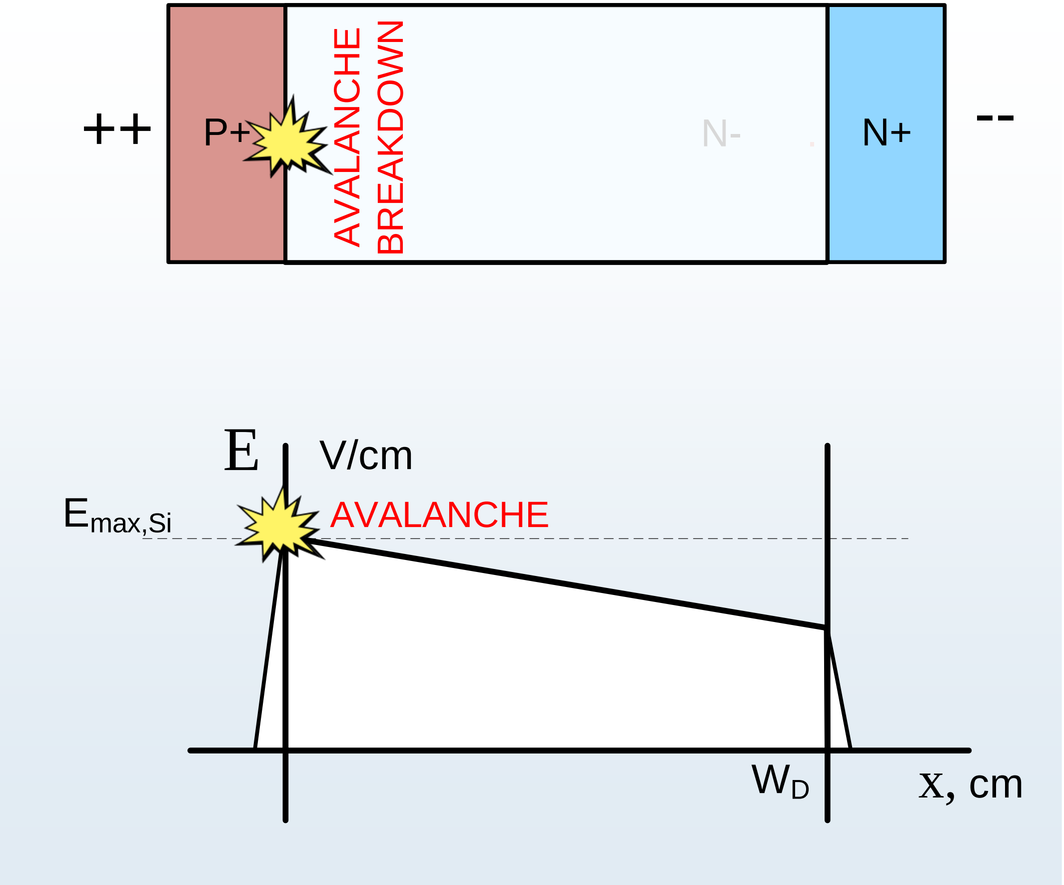
- A depletion region forms at the P+/N- interface as before, then spreading with V_R.



Semiconductor Devices: PiN Diodes

- Increasing the voltage further, causes an increase in the electric field but the P+ cap does not allow the depletion region to spread further.

- **Avalanche breakdown will occur when $E_{np} > E_{max,Si}$.**



Semiconductor Devices: Diodes and Breakdown

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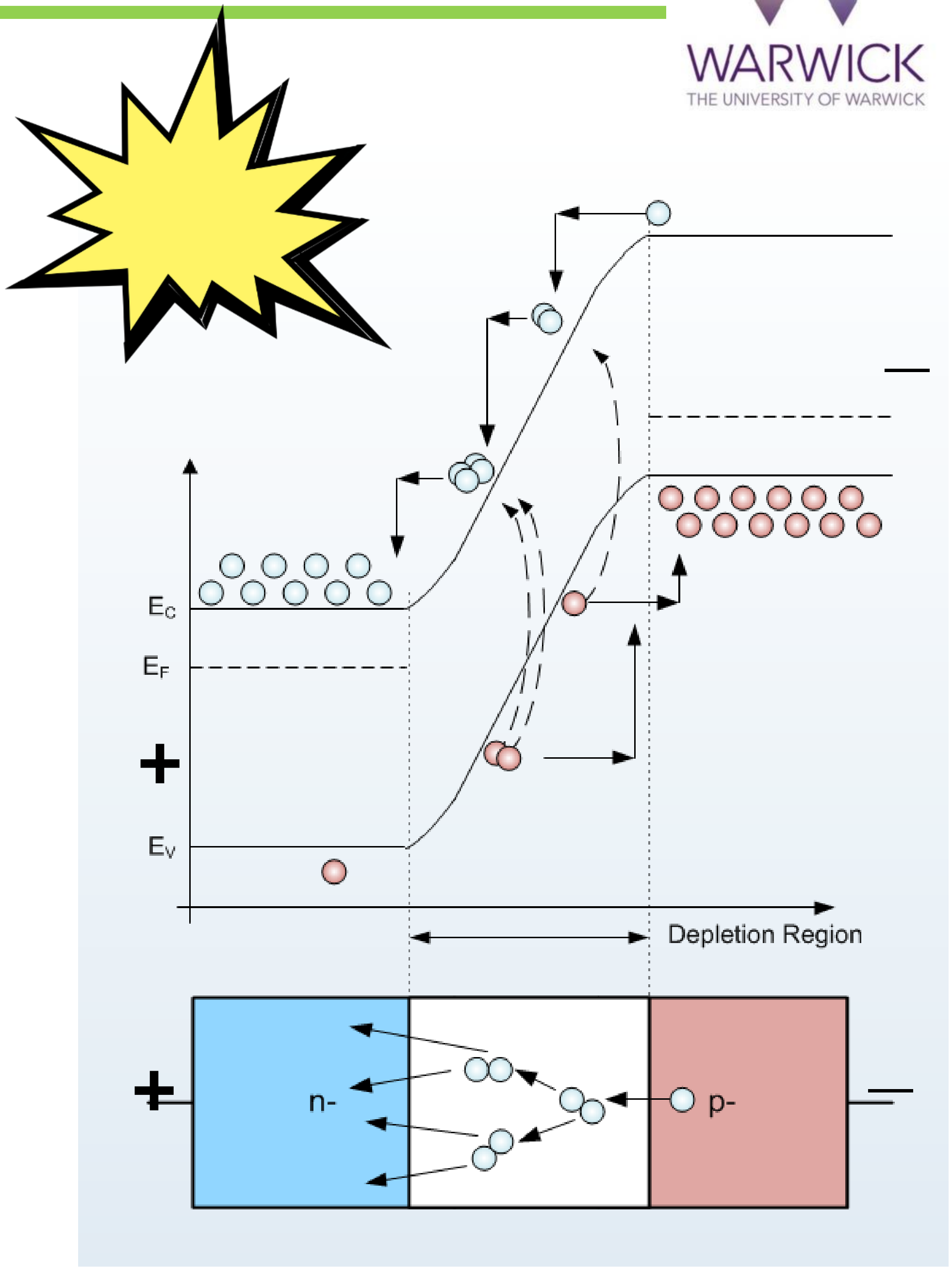


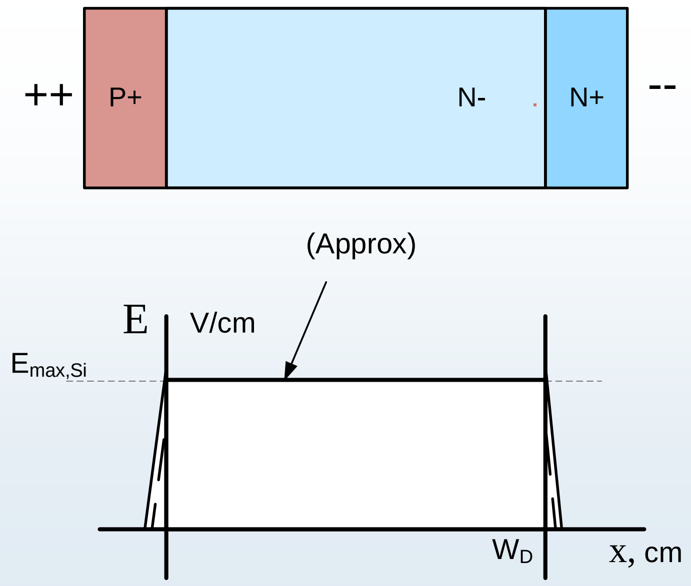
Semiconductor Devices: Diodes and Breakdown

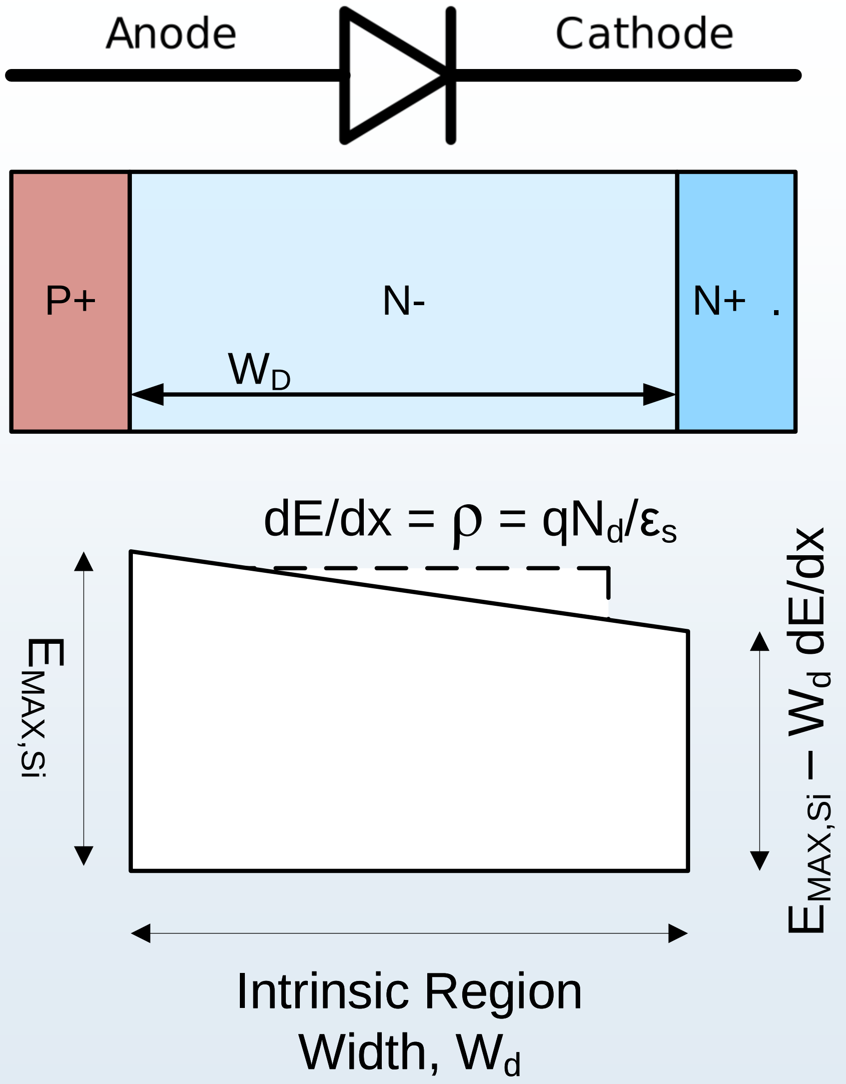
Avalanche is the cause of breakdown in power diodes and in MOSFETs and some IGBTs. To calculate the Breakdown Voltage (V_{BD}):

$$V_{BD} = W_D\left(E_{max,Si} - W_D\frac{qN_D}{2\varepsilon_s}\right)$$

Or….. (cheating….)

$$V_{BD} < W_D E_{max,Si}$$





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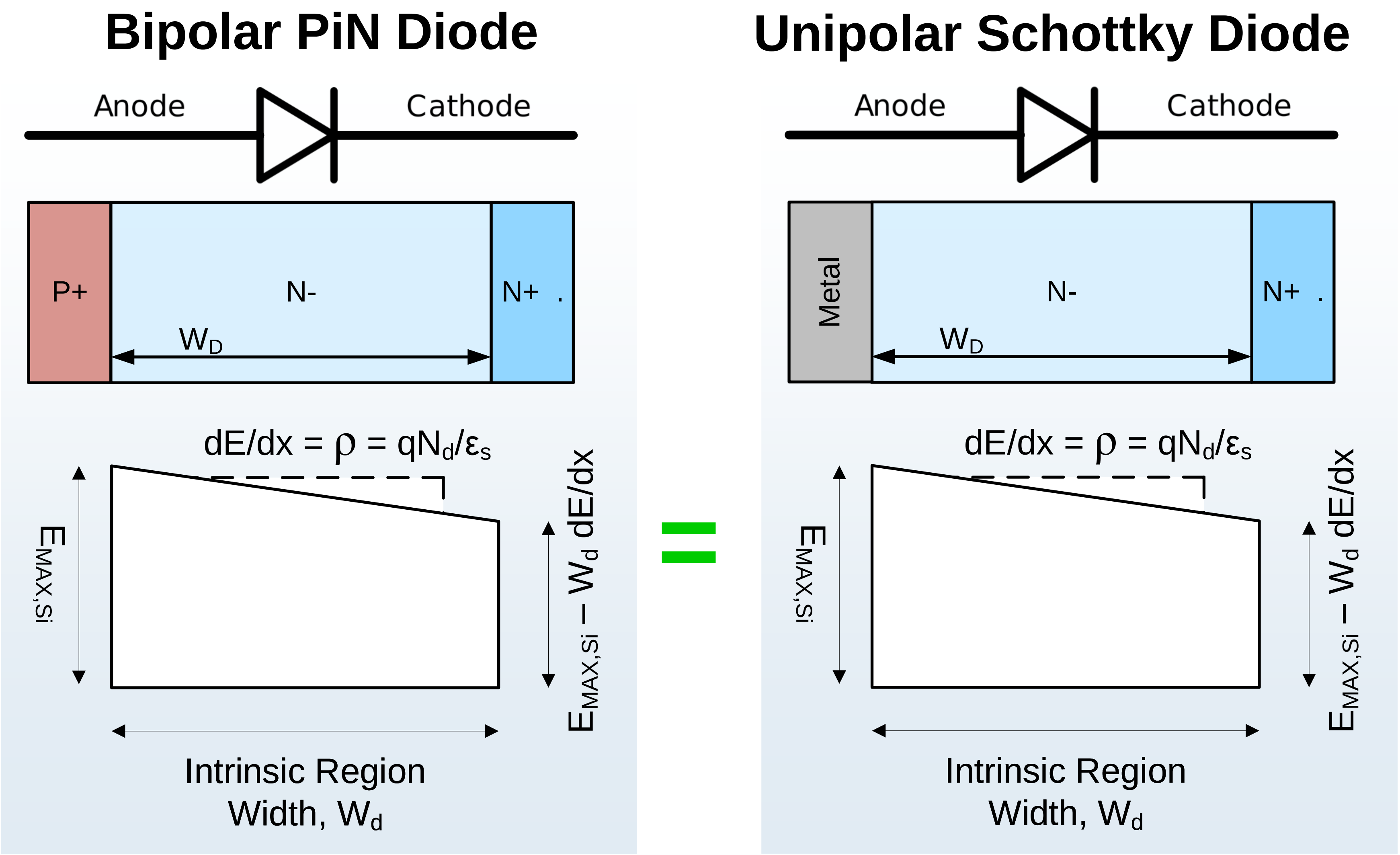
Semiconductor Devices: Schottky Diodes off-state

For Reverse Breakdown, the metal of a Schottky diode can be regarded as a source of holes, the same as the P+ region in a PiN diode.



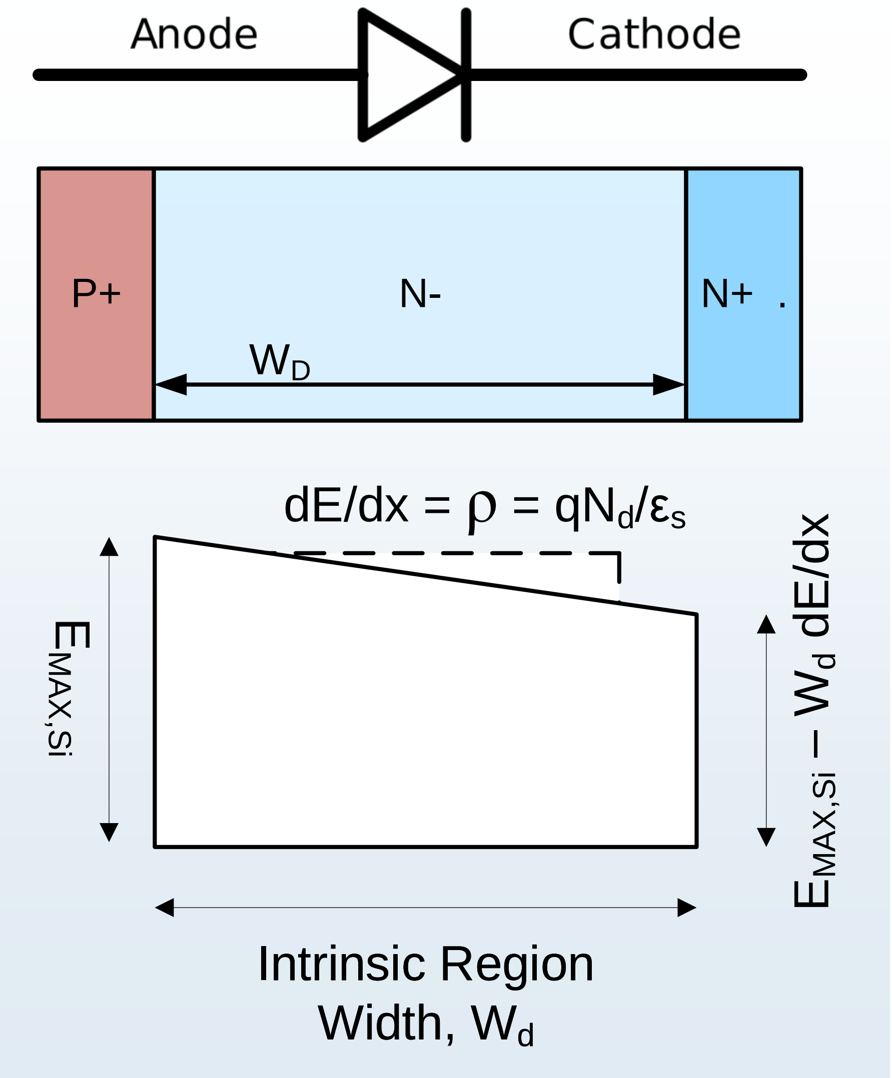
Semiconductor Devices: Optimising Breakdown Voltage

To optimise Breakdown voltage:

$$V_{BD} = W_D\left(E_{max,Si} - W_D\frac{qN_D}{2\varepsilon_s}\right)$$

Maximise Drift Region Width (W_D)

Minimise Drift Region Doping (N_D)

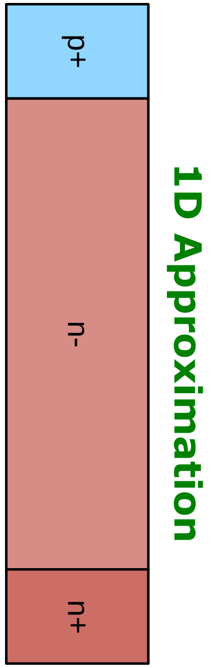


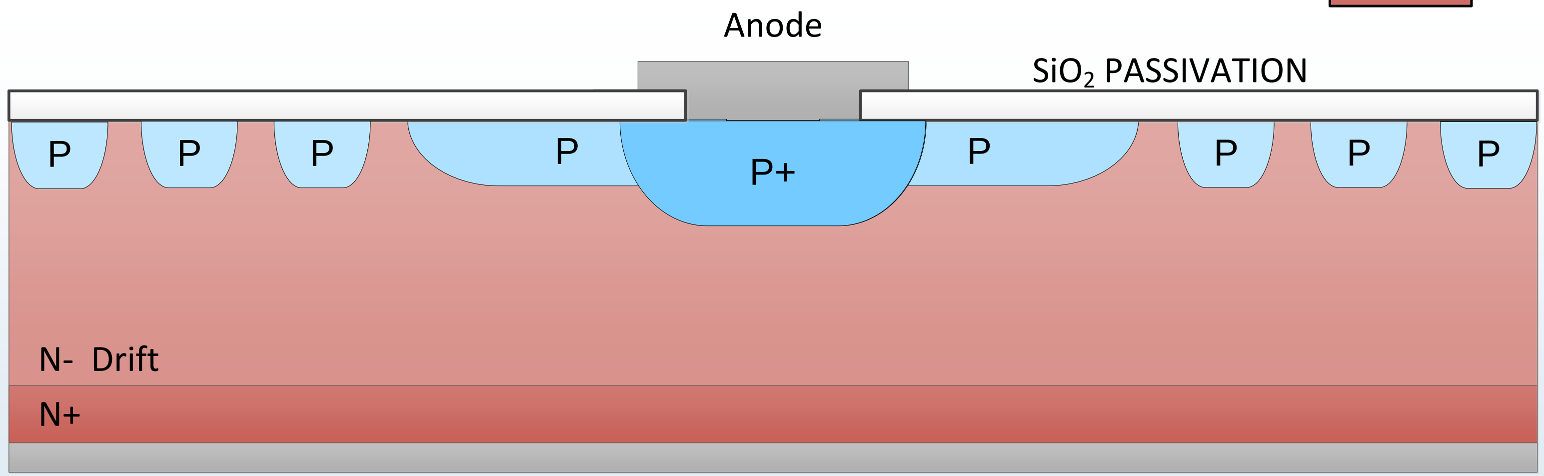
Semiconductor Devices: Optimising Breakdown Voltage

In reality, diodes, like most power devices are vertical in order to maximise their area and hence current rating.

Therefore, one-dimensional approximations of V_{BD} do not hold as there has to be an edge to the device.

Real devices are designed as 2D cut throughs, using FEM to optimise the **edge termination**, which dissipates the high electric field at the device extremities.





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Semiconductor Devices: Diode Resistance

- The on-resistance of a device impacts on the conduction losses…

$$P_{ON} = I^2_{ON} R_{ON}$$

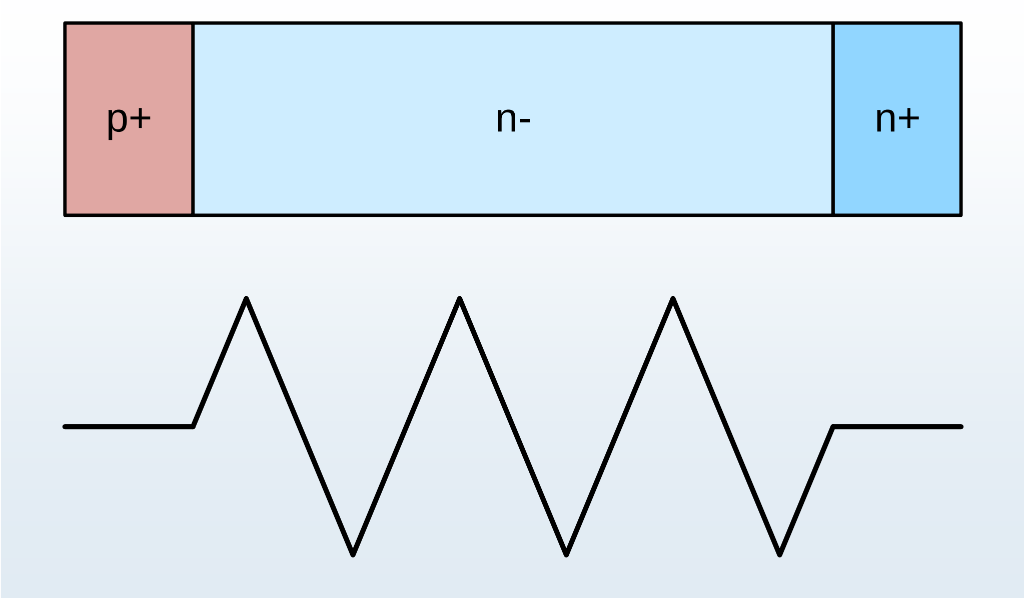
- To minimise R_{ON}, W_D, should be minimised or conductivity (σ) maximised:

$$R_{ON} = \frac{W_D}{A\sigma}$$

$$\sigma = \left(qn\mu_n + qp\mu_p\right)$$

μ = Carrier Mobility; q=charge of electron;

p = number of holes; n = number of electrons (N_D)



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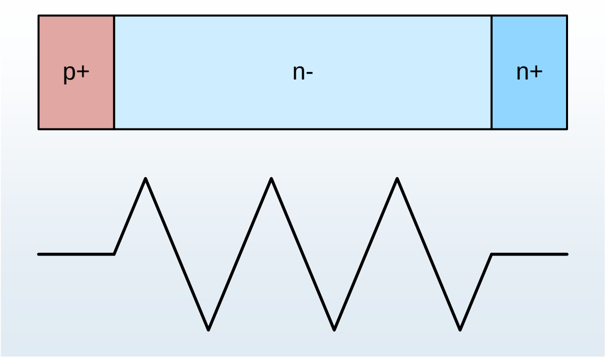
Semiconductor Devices: Optimising Power Devices

To optimise On-Resistance:

$$R_{ON} = \frac{W_D}{A(qn\mu_n + qp\mu_p)}$$

Minimise Drift Region Width (W_D)

Maximise carriers (p,n; N_D)

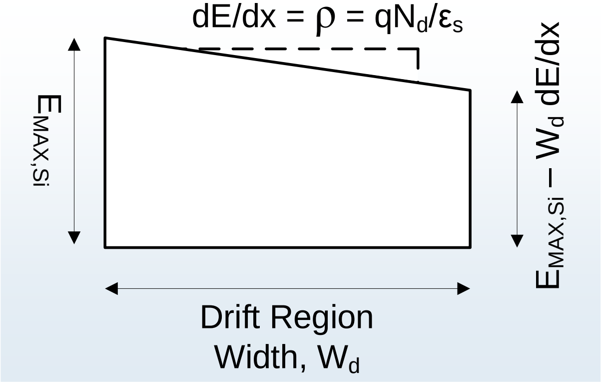


To optimise Breakdown voltage:

$$V_{BD} = W_D\left(E_{max,Si} - W_D\frac{qN_D}{2\varepsilon_s}\right)$$

Maximise Drift Region Width (W_D)

Minimise Drift Region Doping (N_D)



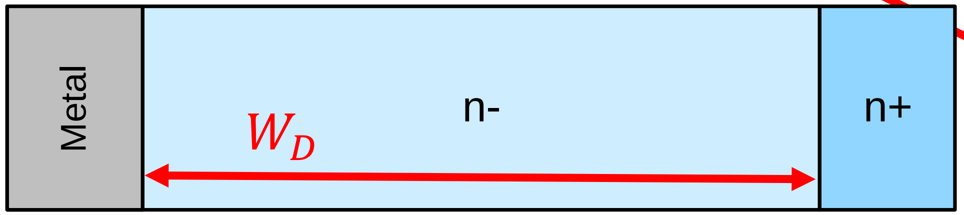
Semiconductor Devices: Unipolar limit

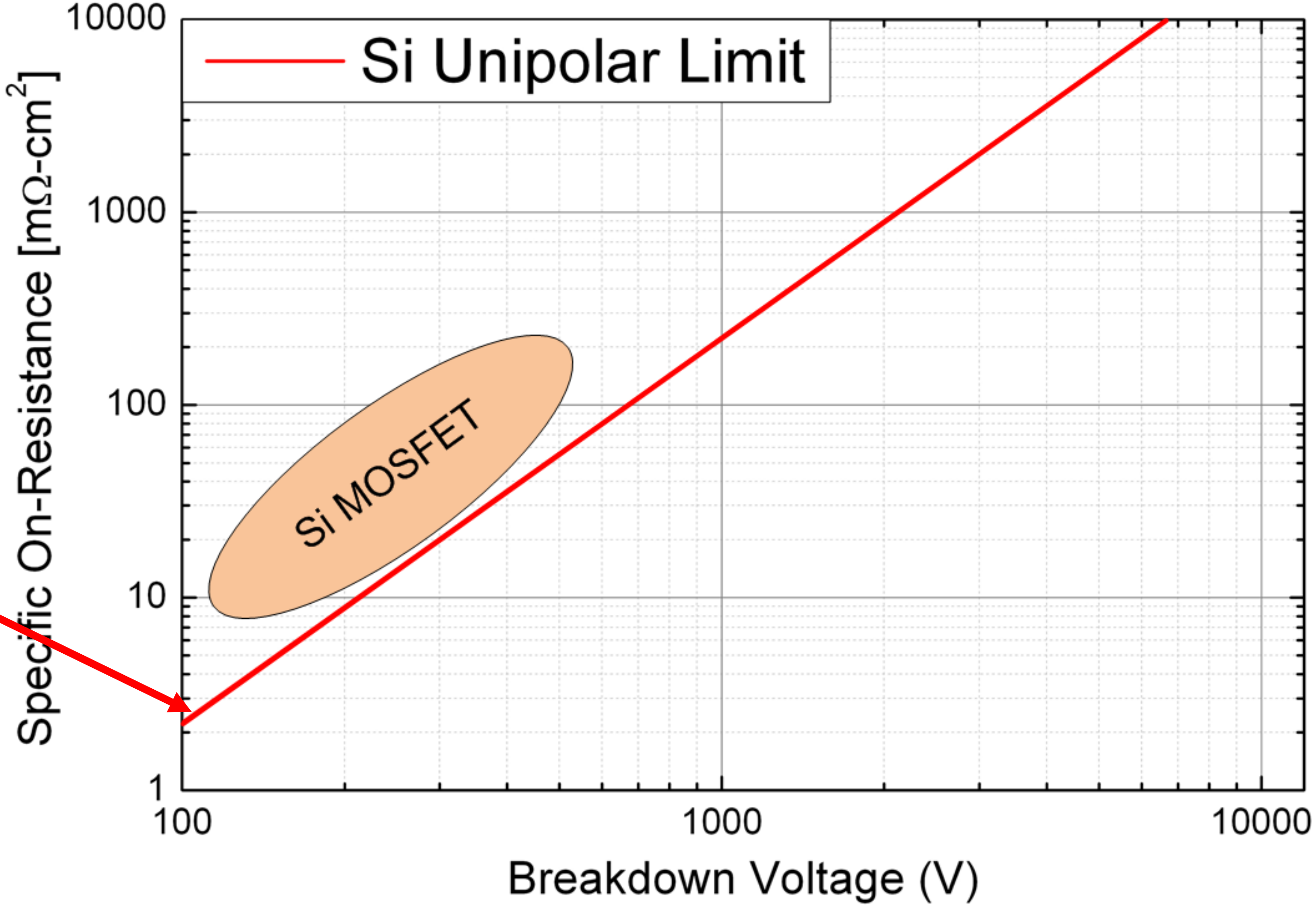
For a Unipolar device (Schottky, MOSFET):

$n = N_D$, and W_D is a trade off.

$$R_{ON} = \frac{W_D}{A q N_D \mu_n}$$

$$V_{BD} = W_D\left(E_{max,Si} - W_D \frac{q N_D}{2\varepsilon_s}\right)$$



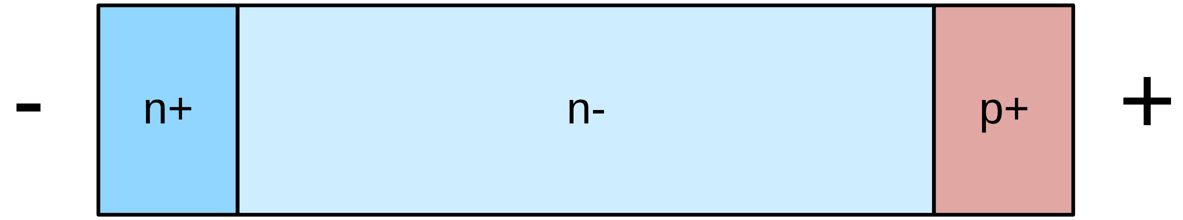


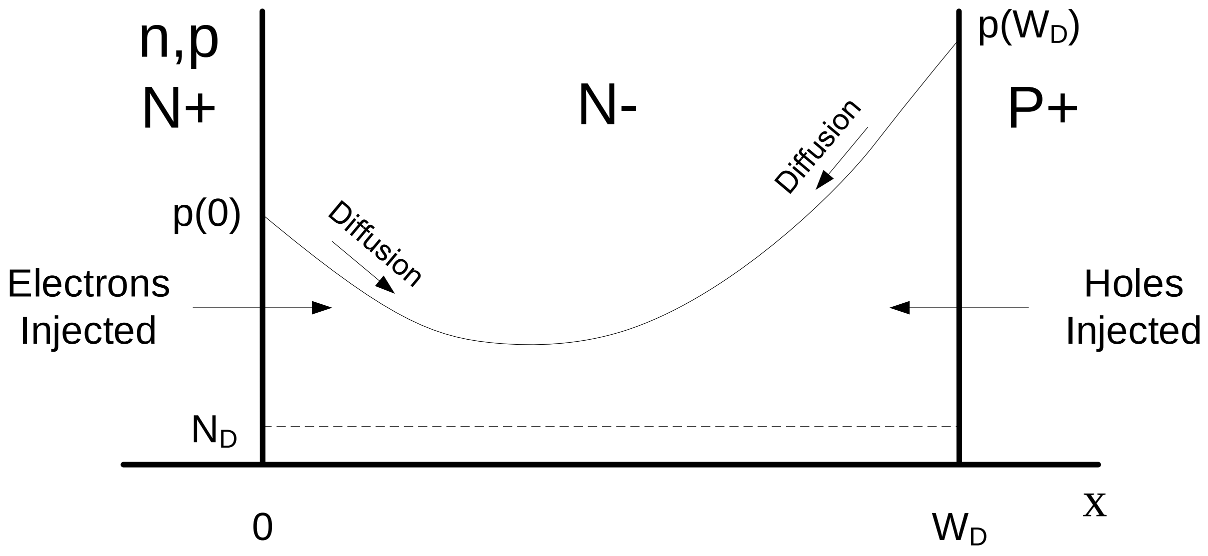
Semiconductor Devices: Bipolar Devices

- Bipolar devices (IGBTs, PiN diodes) use both electrons and holes in the on-state.

- Carriers are injected from both ends of the drift region. This lowers the on-resistance *only* while the device is on. This is **Conductivity Modulation**.

$$R_{ON} = \frac{W_D}{A(qn\mu_n + qp\mu_p)}$$



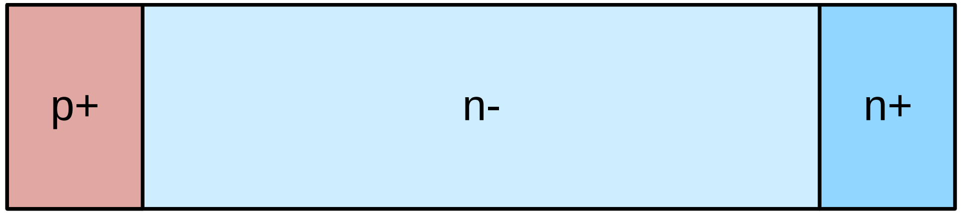


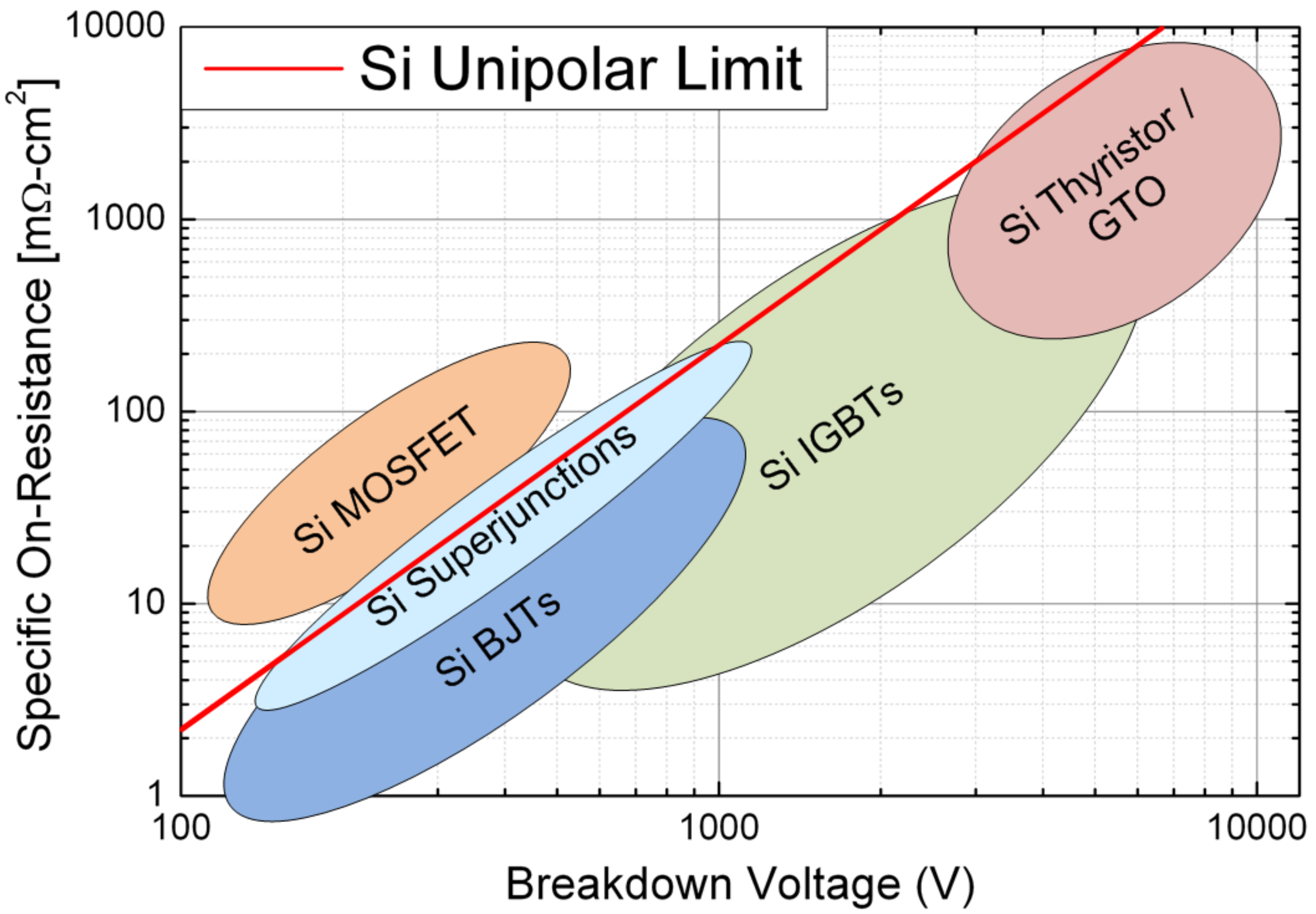
Semiconductor Devices: Bipolar Devices

Bipolar devices cheat the unipolar limit, using high-level injection.

$$R_{ON} = \frac{W_D}{A(qn\mu_n + qp\mu_p)}$$

$$V_{BD} = W_D\left(E_{max,Si} - W_D\frac{qN_D}{2\varepsilon_s}\right)$$

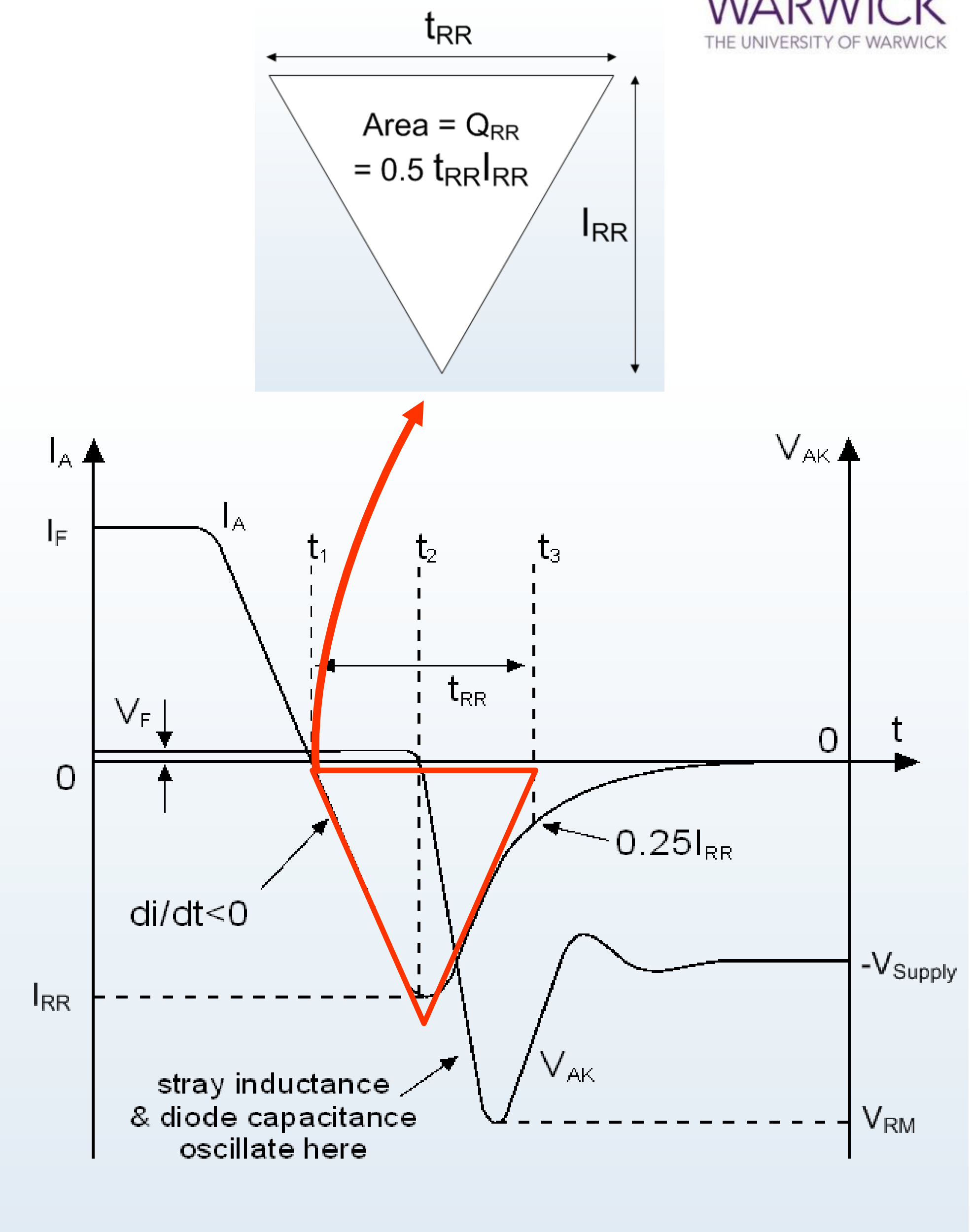




Semiconductor Devices: Bipolar Devices

- The holes and electrons that conductivity modulate the on-state of the devices have to be injected into the drift region on turn-on and extracted during turn-off.

- This causes energy losses when switching, particularly in turn-off. Large negative 'Reverse Recovery' current (I_{RR}) peaks occur as the charge (Q_{RR}) is extracted.



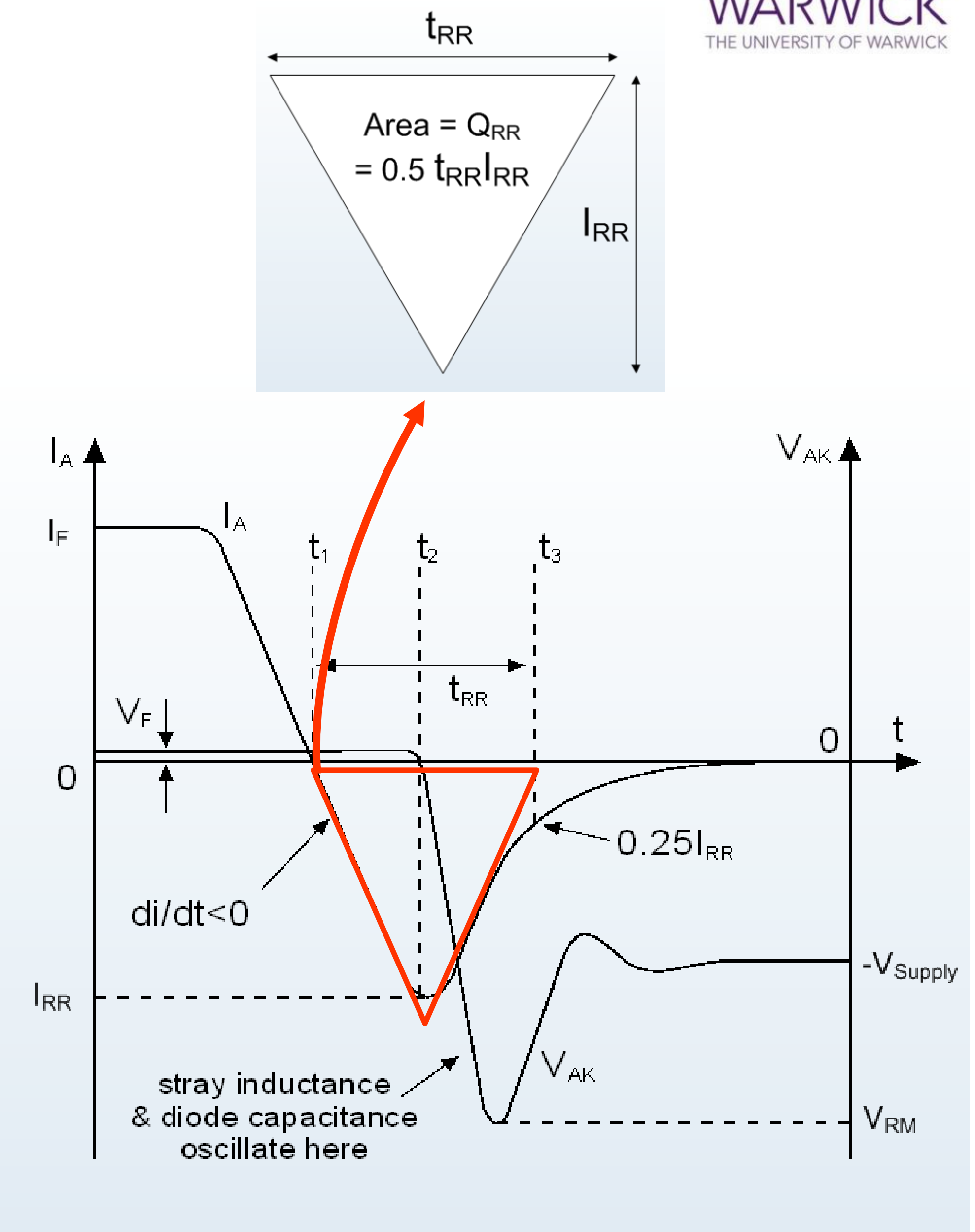
Semiconductor Devices: Bipolar Devices

- Q_{RR} can be optimised by controlling the carrier lifetime (τ) of the material.

- Carrier lifetime is the time it takes for the injected carriers to recombine.

- If τ is high, on-resistance and on state losses will be low, but switching losses will be high.

- If τ is low, on-resistance and on state losses will be high, but switching losses will be low.



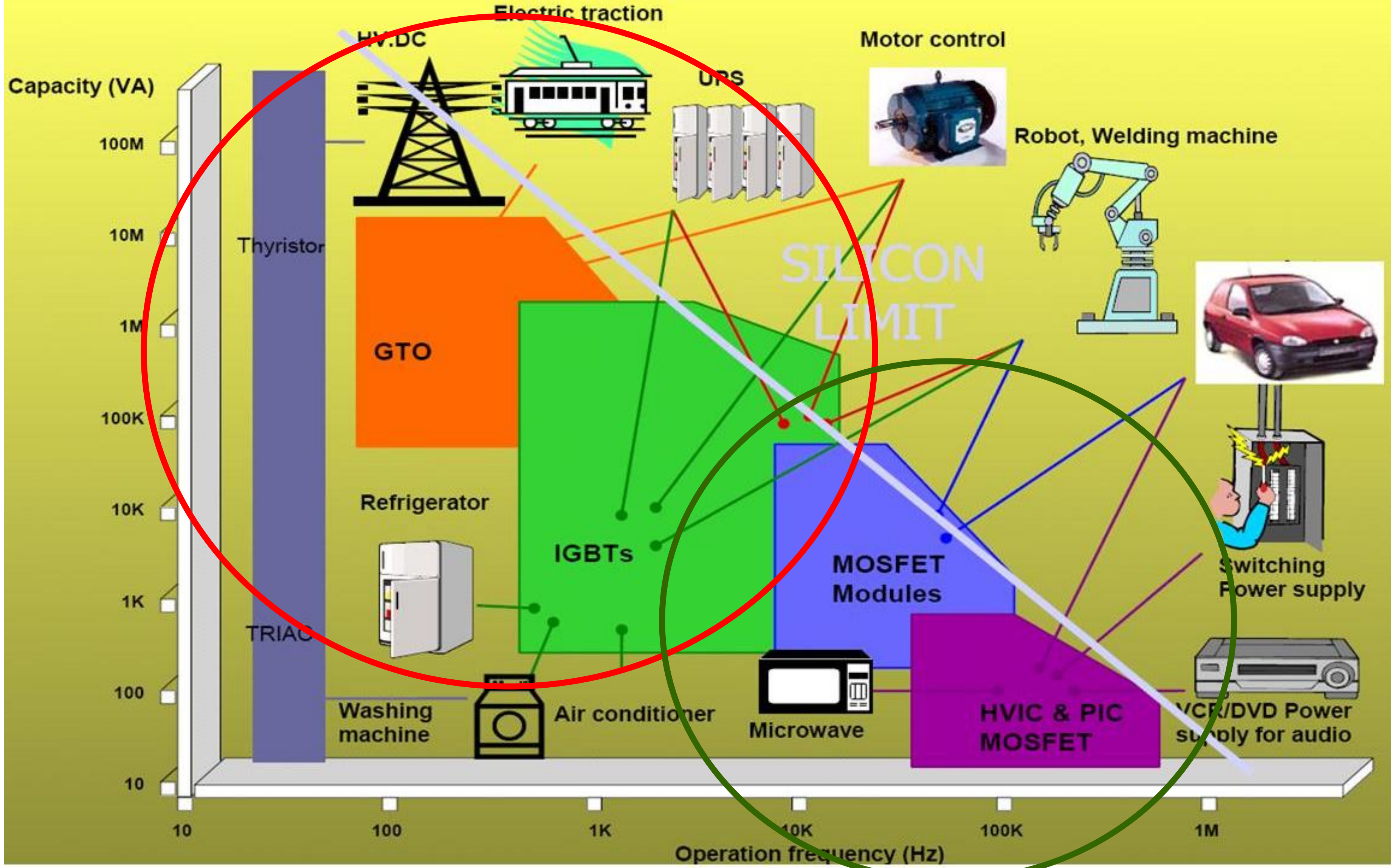
Semiconductor Devices: Unipolar vs Bipolar Device Trade-off

Bipolar Devices:

Low R_{ON} but high switching loss limits f_{SW}.

Unipolar Devices:

Higher R_{ON} limits power of applications but low switching loss means fast f_{SW}.



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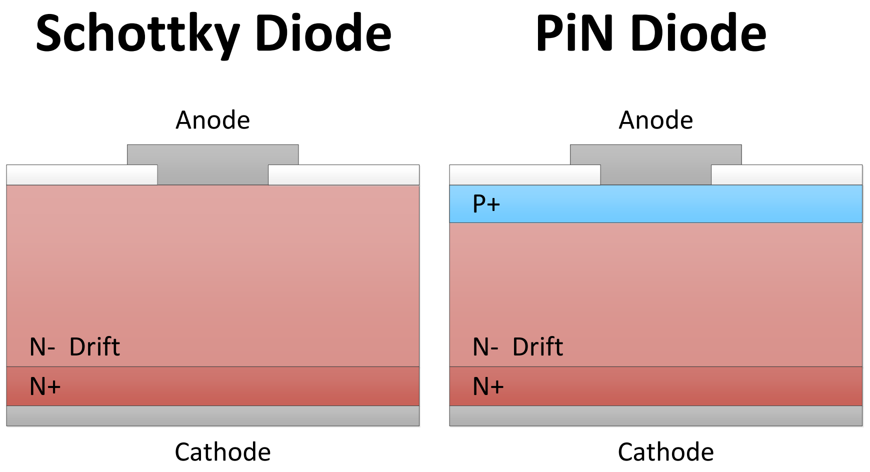
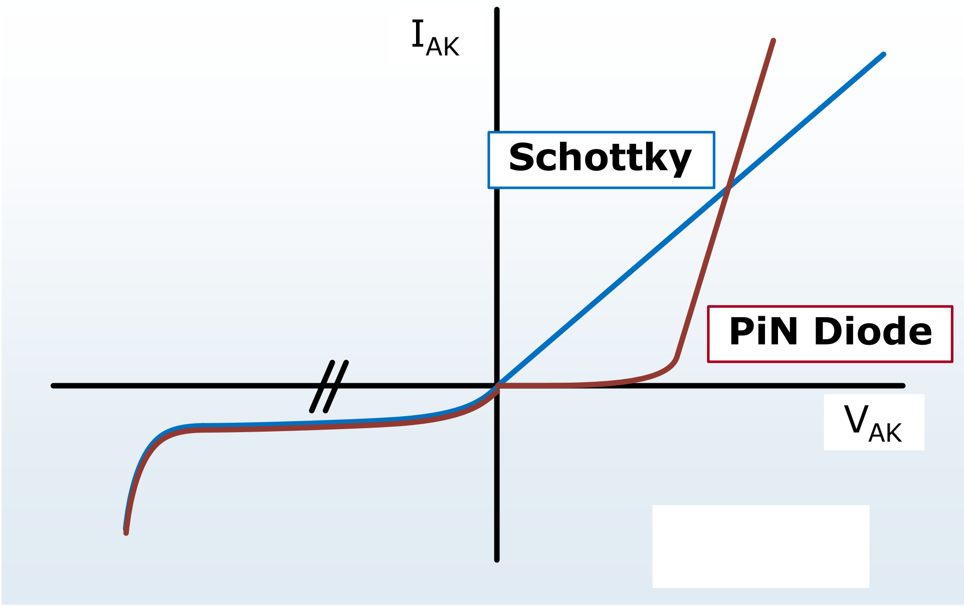
Semiconductor Devices: Power Diodes Summary

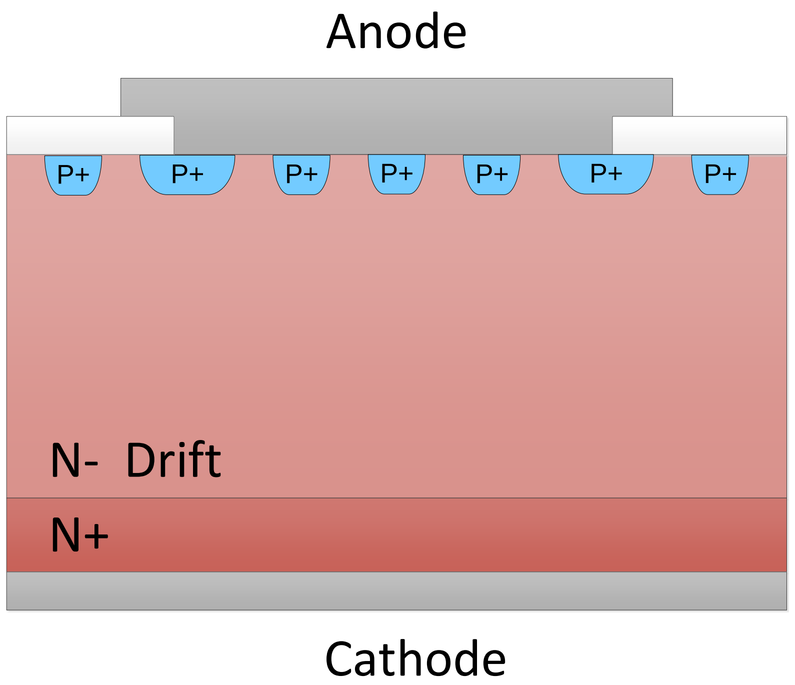
- Power diodes are vertical so that large area, high current devices are possible.
- PiN diodes have a built-in potential arising from the p-n junction but have very low resistance.
- Schottky Diodes are unipolar, exploiting the potential barrier at the metal-semiconductor interface. It is fast switching, having no conductivity modulation.

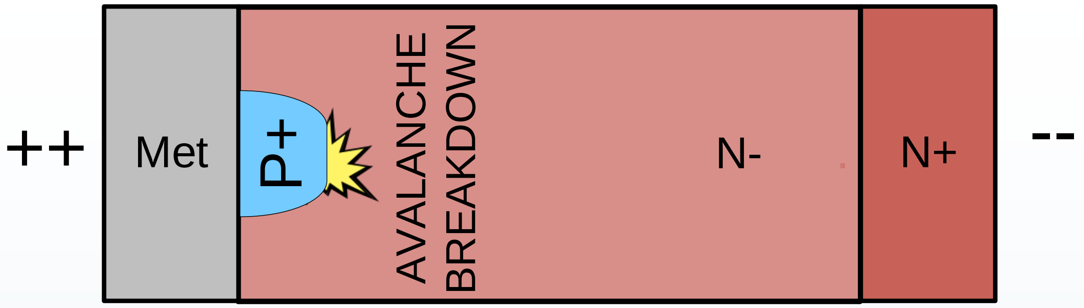


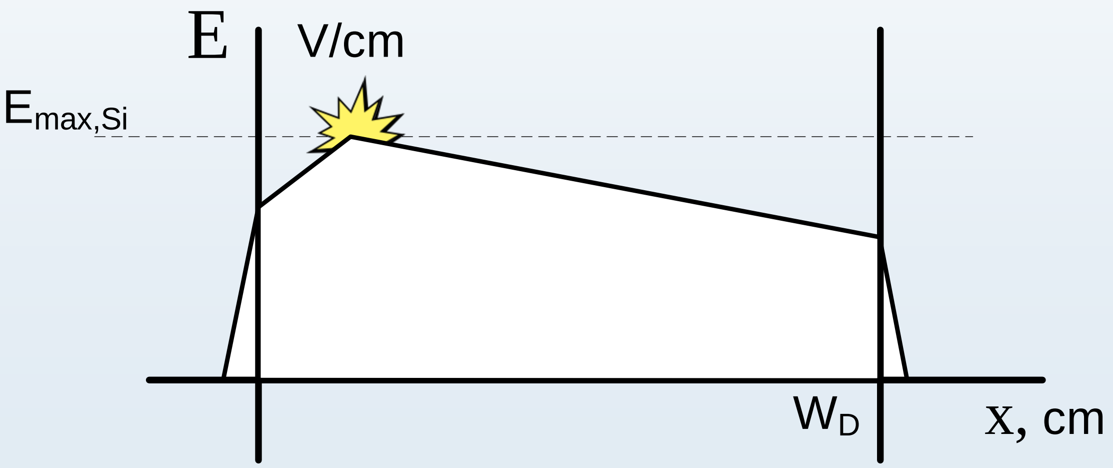


Semiconductor Devices: State of the Art Power Diodes

Device designers use a Merged PiN / Schottky (MPS) diode, or a Junction Barrier Schottky (JBS) to bring the peak of the e-field away from the surface. This improves the device's 'ruggedness'.

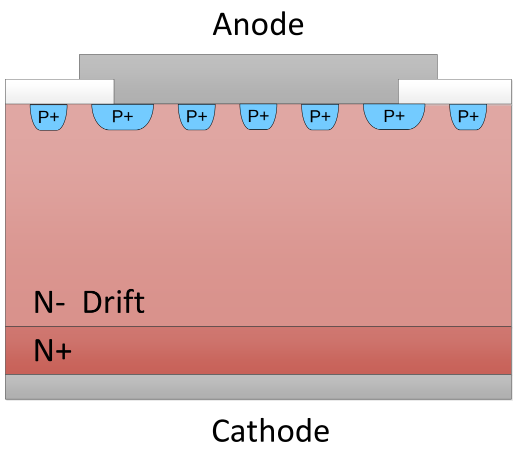




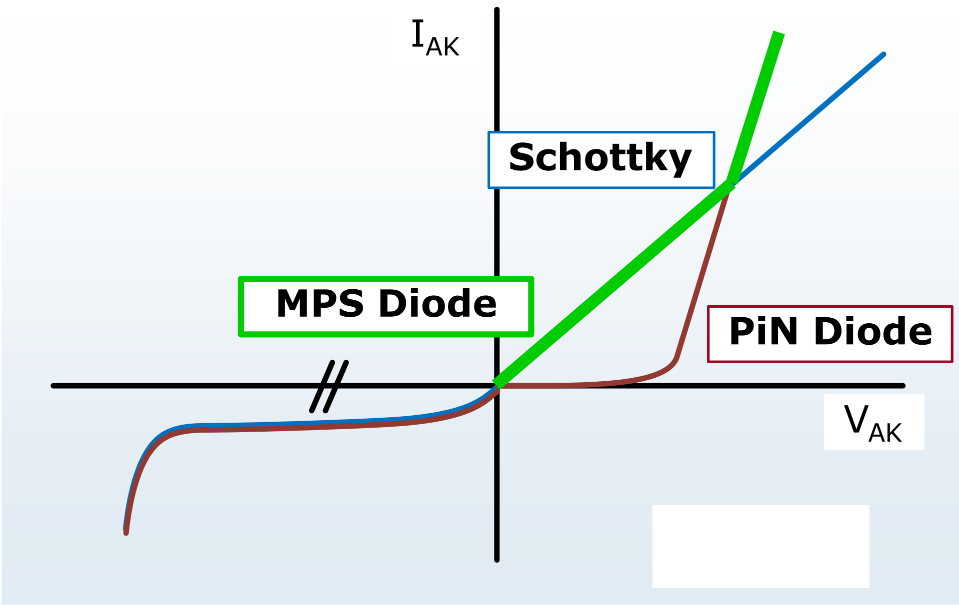


Semiconductor Devices: State of the Art Power Diodes

In a Merged PiN / Schottky (MPS) diode, the P-regions are active and the device is a true hybrid. Ideally, they would switch on as Schottky diodes with high level injection at high current density.



In a Junction Barrier Schottky (JBS) the P regions are lower doping and they do not result in any hole injection. Hence they only shape the E-field.



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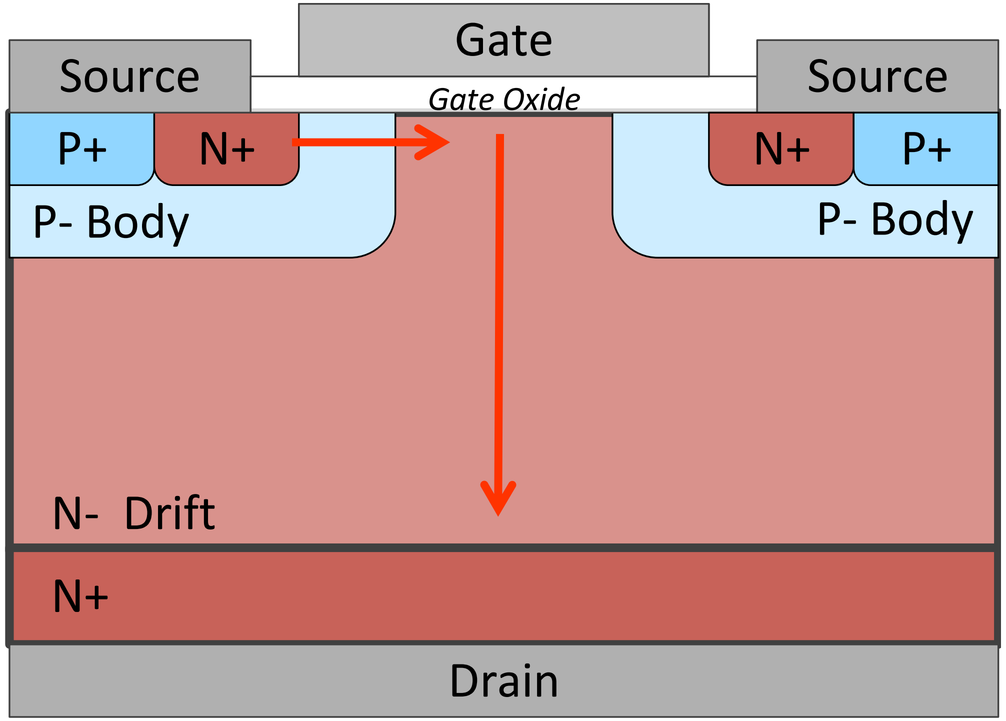
Semiconductor Devices: Power MOSFETs

- The Power MOSFET is a unipolar device, known as a *Double Diffused MOSFET (DMOS)*.

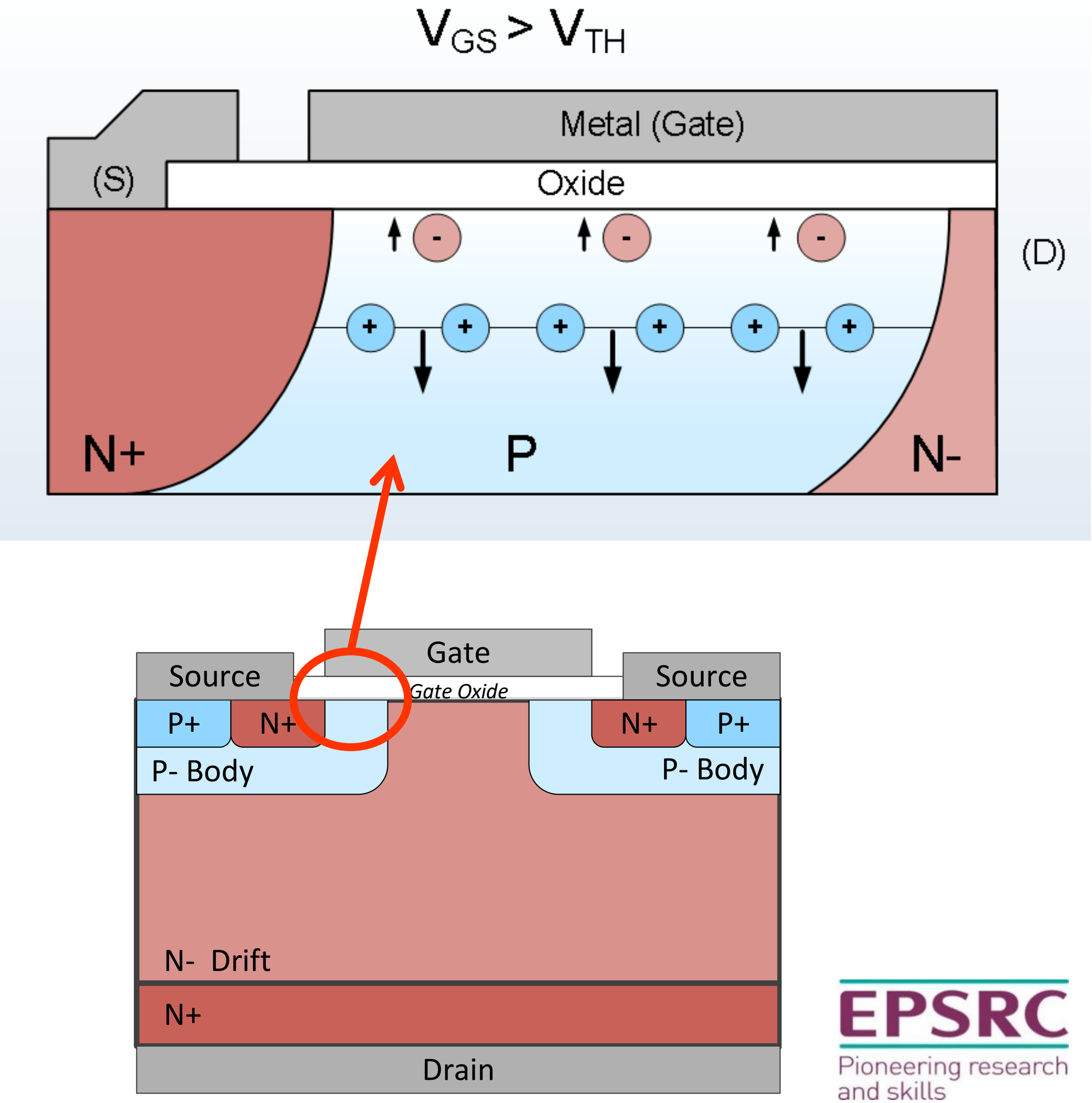
- The application of a +ve gate voltage forms *two* inversion regions in the p-channels, that allows electron to flow from source to drain.

- As a vertical device it makes use of a thick drift region for supporting high voltage and a large area for high current.



Semiconductor Devices: Power MOSFETs

- Zooming in on one of the gates of the DMOS device, this region resembles a CMOS transistor
- A positive voltage is applied to the gate V_{GS} greater than the threshold voltage V_{TH}.
- This repels the majority holes of the p-type and attracts the minority electrons.
- An *inversion layer* forms - an N-channel is formed in the p-type layer, connecting the N-type Source and Drift regions

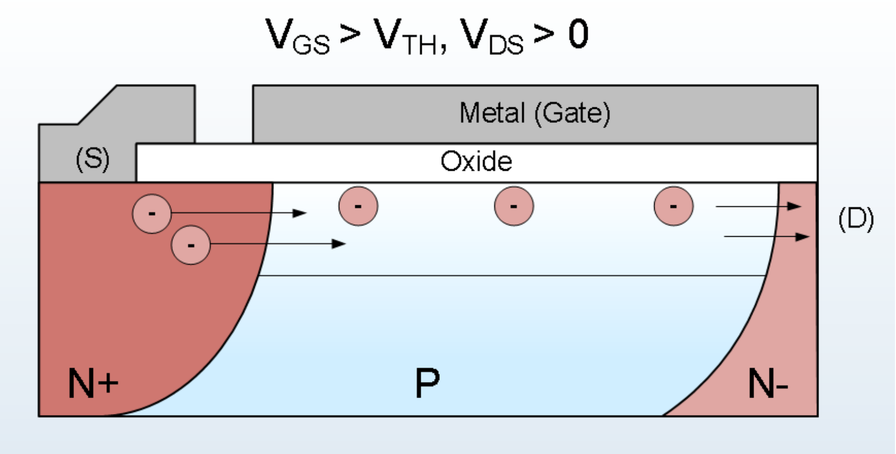


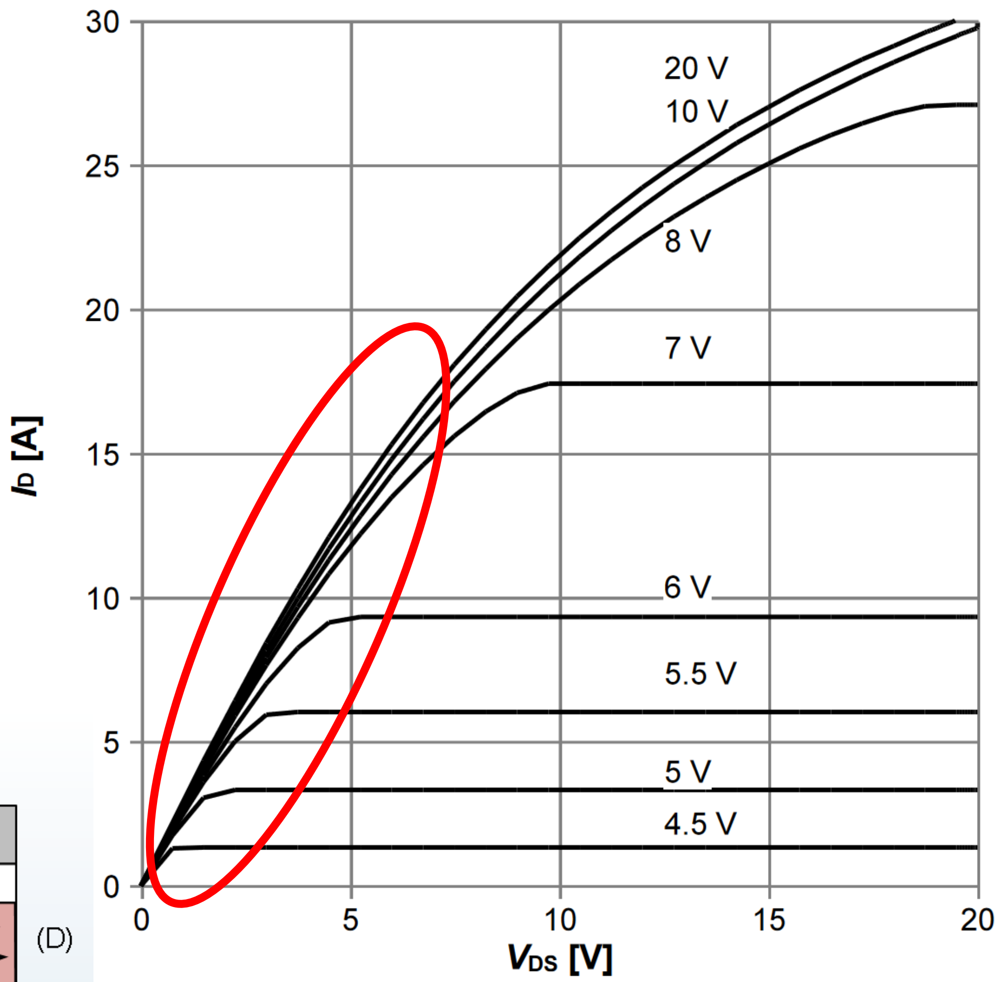
Semiconductor Devices: Power MOSFETs

The MOSFET response has two distinct regions:

- A Linear Region, occurs with the application of a small drain voltage V_{DS}.
- This region is governed by the on-resistance of the device $R_{DS,ON}$ (ohms-cm^2).

$$R_{DS(on)} = \lim_{V_{DS}\to 0}\left(\frac{V_{DS}}{I_D}\right)$$





Infinieon 600V CoolMOS™ E6 Power MOSFET

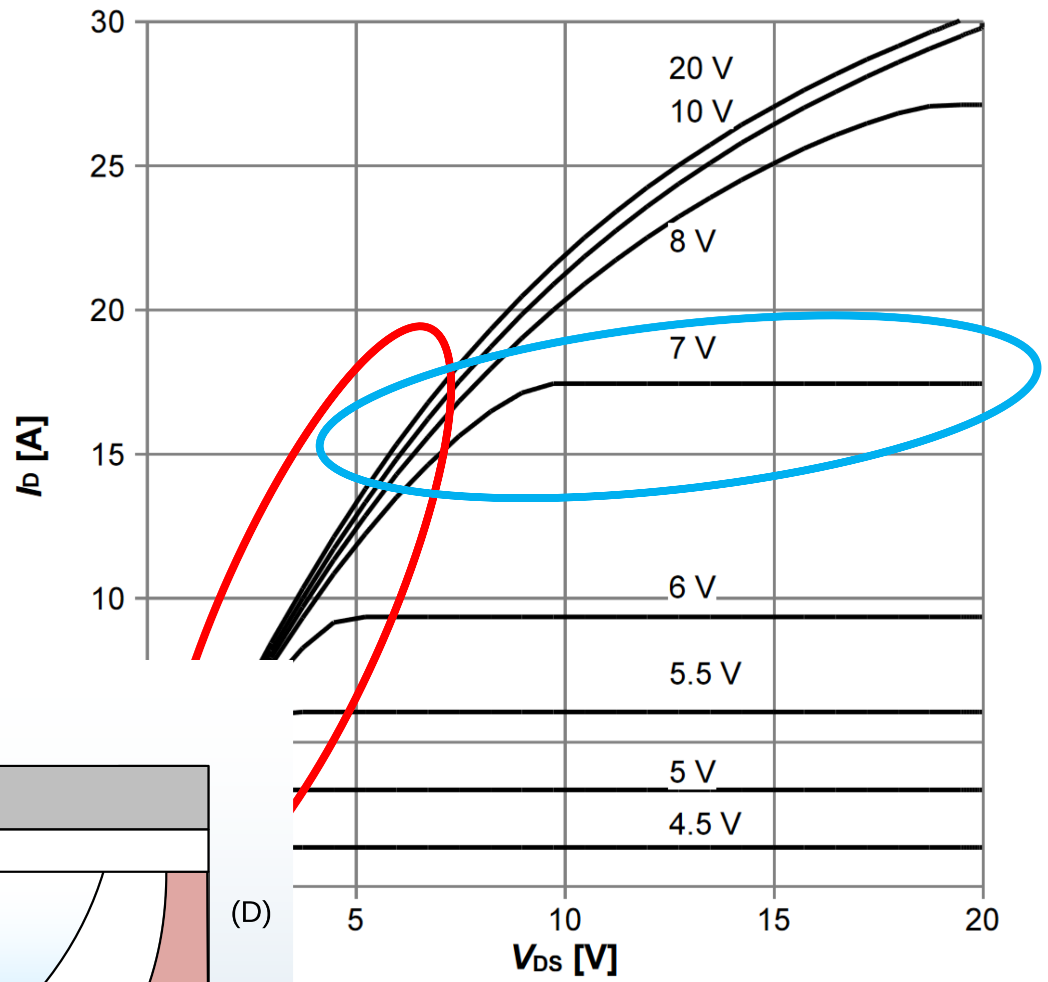
Semiconductor Devices: Power MOSFETs

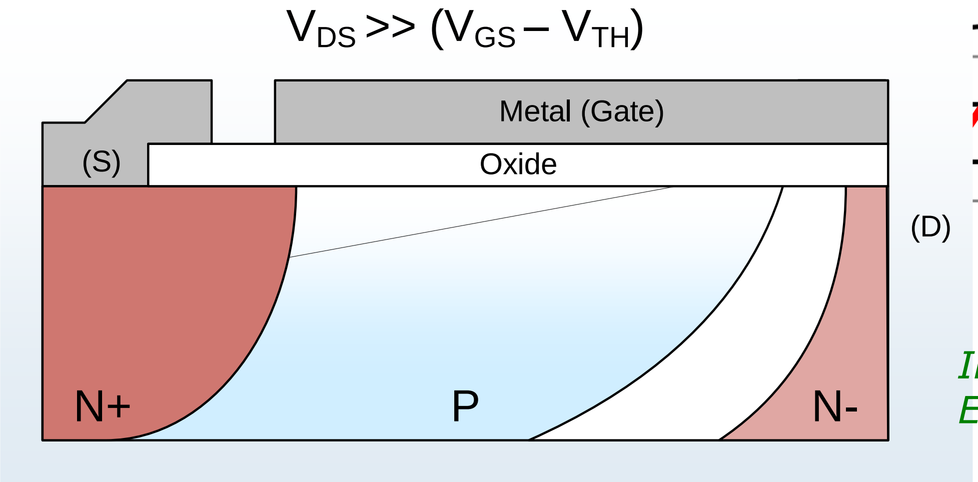
The MOSFET response has two distinct regions:

- A Saturation Region, occurs as $V_{DS} > V_{GS}$ as the channel becomes fully pinched off.

- Here, the MOSFET is entirely dependent on the gate voltage and acts like a nonlinear voltage controlled current.

- $I_D = K_P (V_{GS} - V_{TH})^2 / 2$





Infinieon 600V CoolMOS™ E6 Power MOSFET

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Semiconductor Devices: Power MOSFETs

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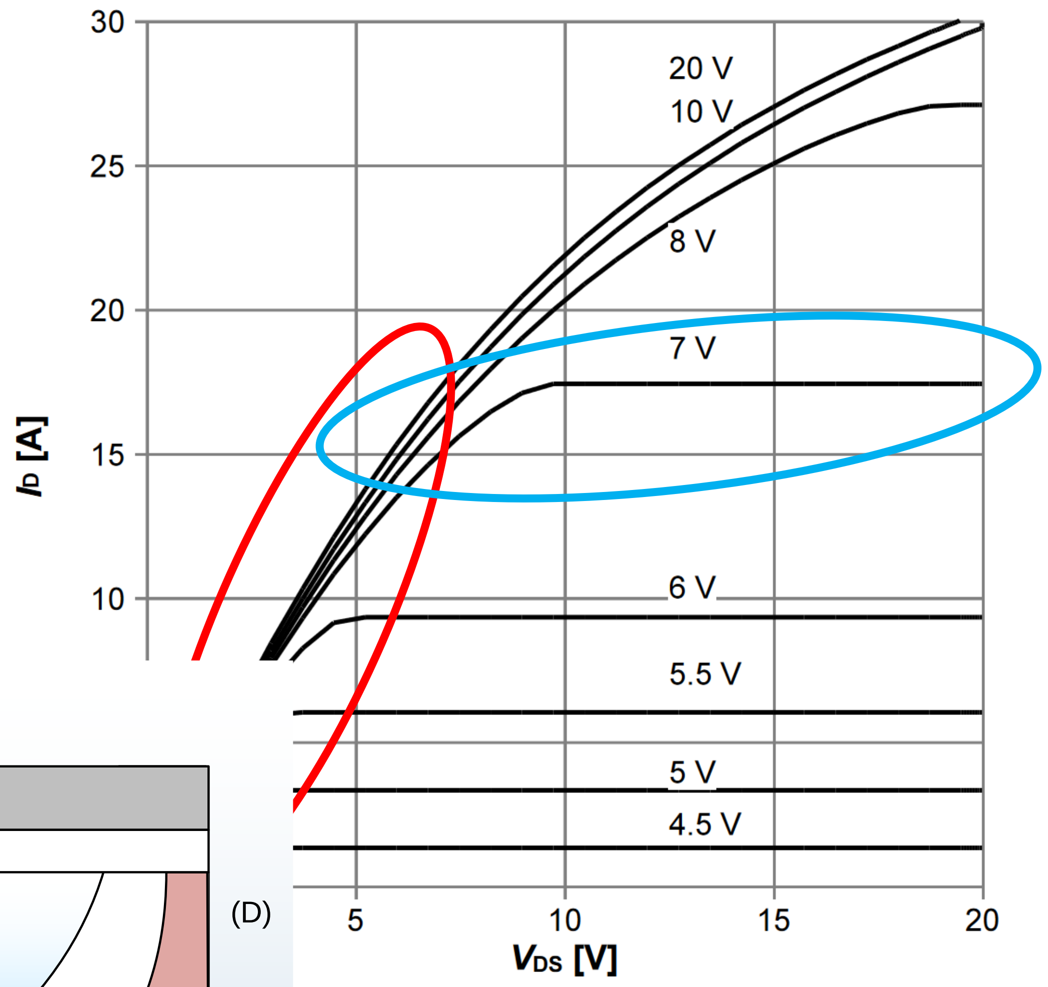
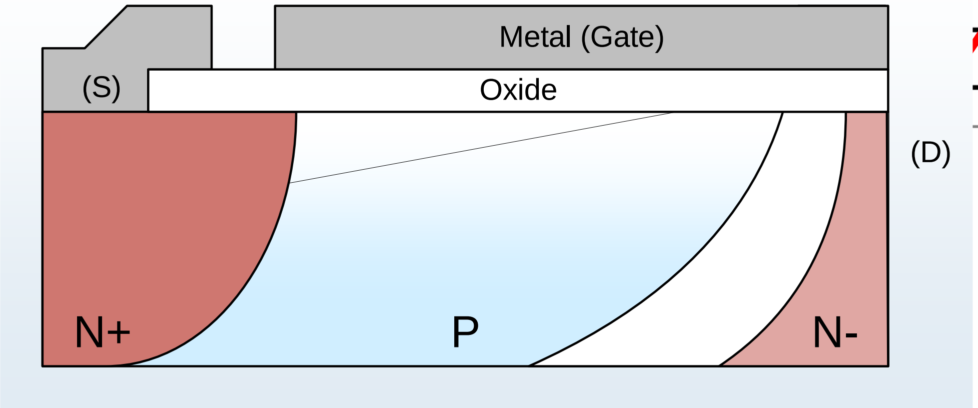


600V CoolMOS™
E6 Power MOSFET

$V_{DS} >> (V_{GS} – V_{TH})$



Semiconductor Devices: Power MOSFETs

The planar MOSFET has four major resistances.

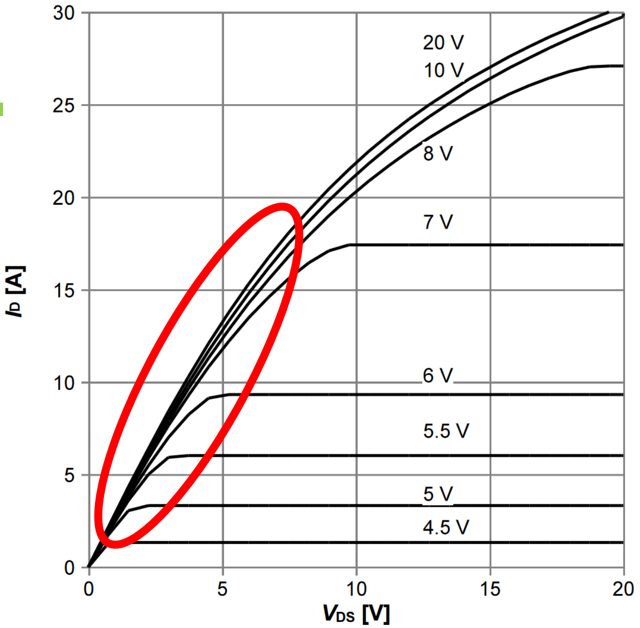
- The **drift resistance** is the major contributor to most devices and scales with V_{BD}.

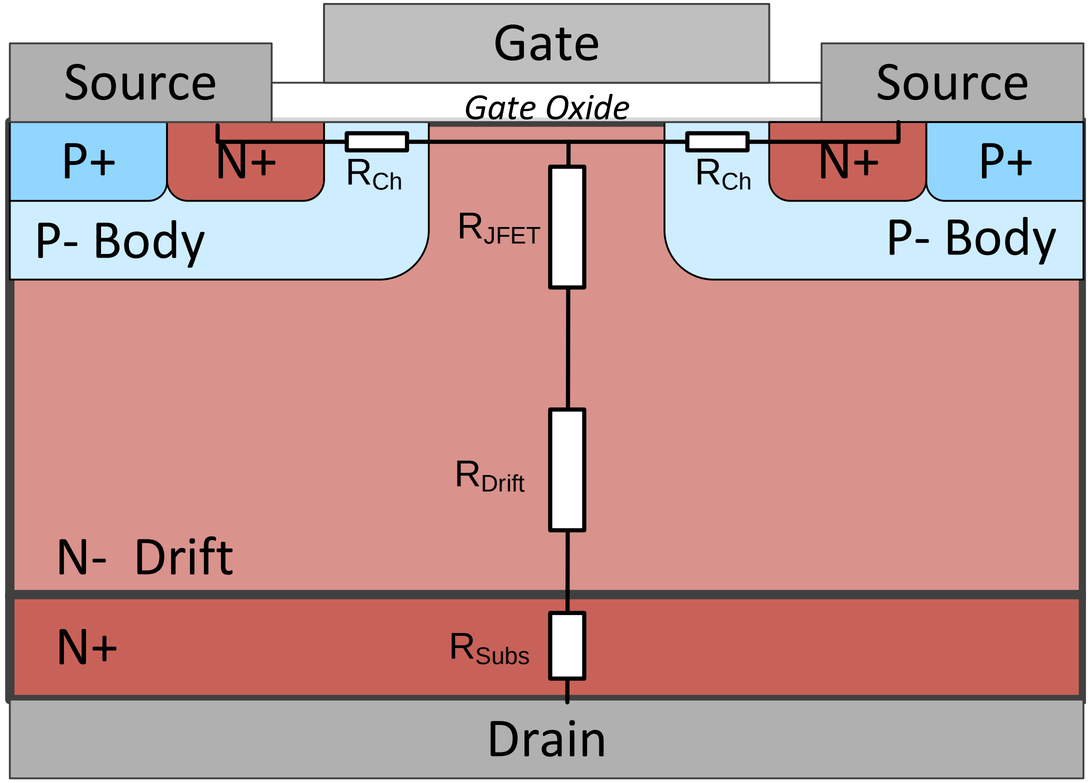
- The **channel resistance** is affected by the semiconductor surface and will not scale.

- **JFET resistance** is the pinching of the current in the centre of the device. R_{JFET} is in direct conflict with device area (and so cost).

- **Substrate resistance** arises from the thick starting wafer. It is usually aggressively thinned after fabrication.

Infineon 600V CoolMOS™ E6 Power MOSFET

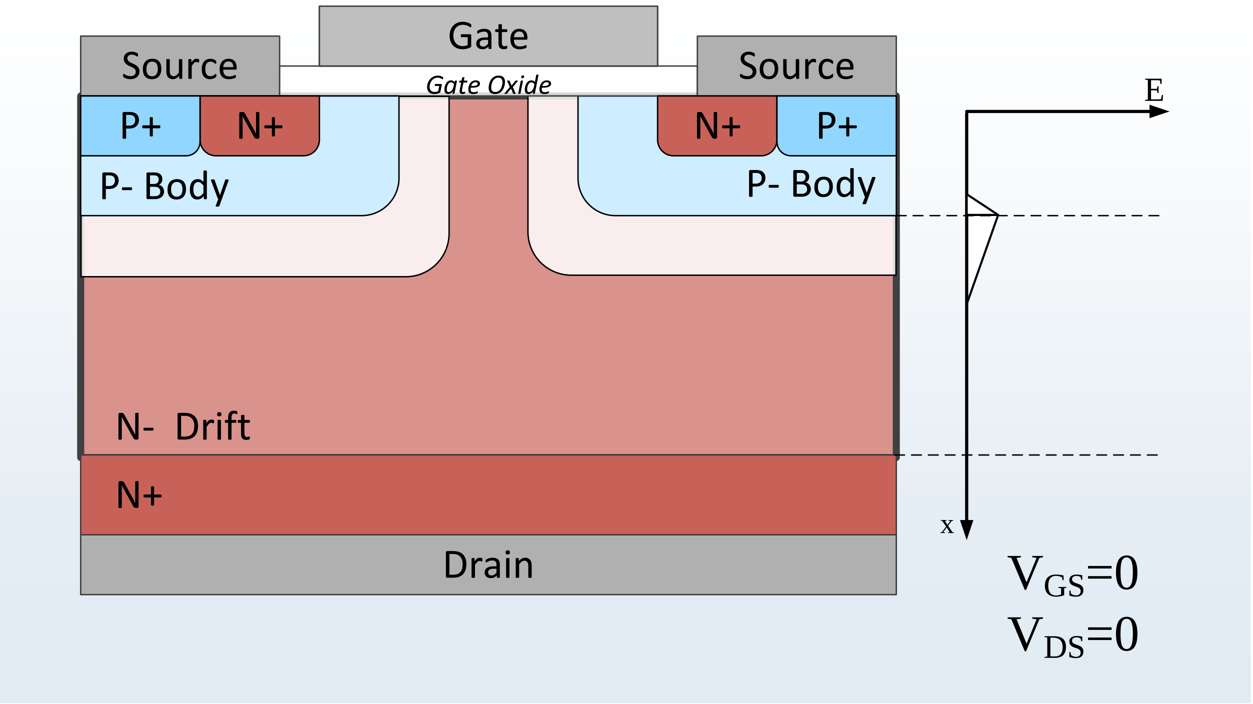




Semiconductor Devices: Power MOSFETs – Off state

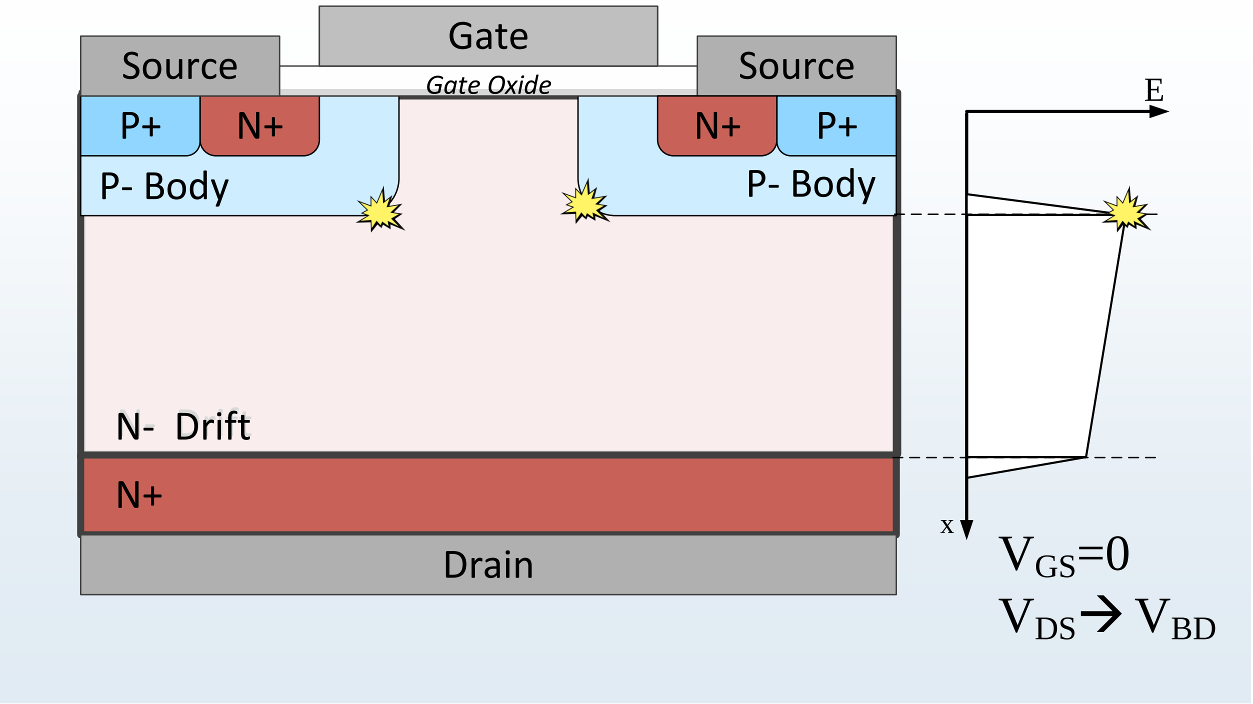
- The MOSFET is in its Forward blocking state when $V_{DS} > 0$ and $V_{GS} < V_{TH}$.

- Without applying $V_{DS,}$ a depletion region exists around the P-body – N-Drift junctions



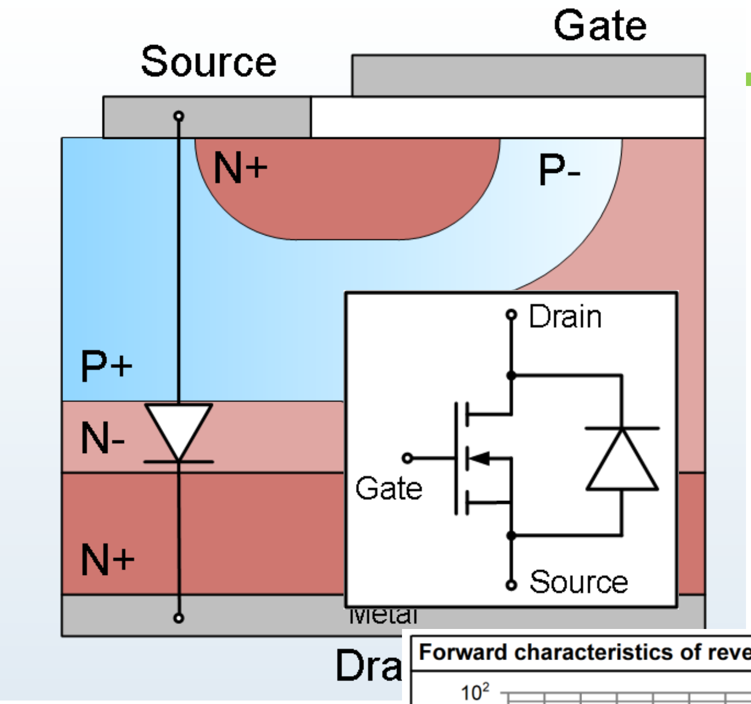
Semiconductor Devices: Power MOSFETs – Off state

- The MOSFET is in its Forward blocking state when $V_{DS} > 0$ and $V_{GS} < V_{TH}$.
- Without applying $V_{DS,}$ a depletion region exists around the P-body – N-Drift junctions
- Applying V_{DS} further reverses this p-n junction, causing the depletion region to widen and the field to increase…
- …until the device breaks down at the junction corner



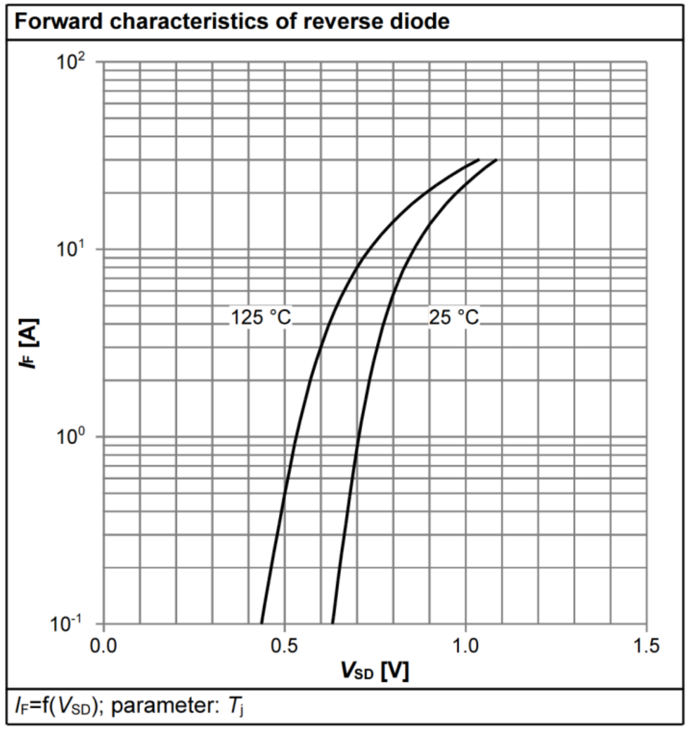
Semiconductor Devices: Power MOSFETs
The Body Diode / Third-quadrant behaviour

- The MOSFET has a built in PiN diode, across the P+ source contact, N-Drift and N+ substrate, removing any reverse blocking capability in the device.



- This body diode can be utilised as a freewheeling diode in a half bridge circuit, providing a single unified solution, reducing parts cost, and space.

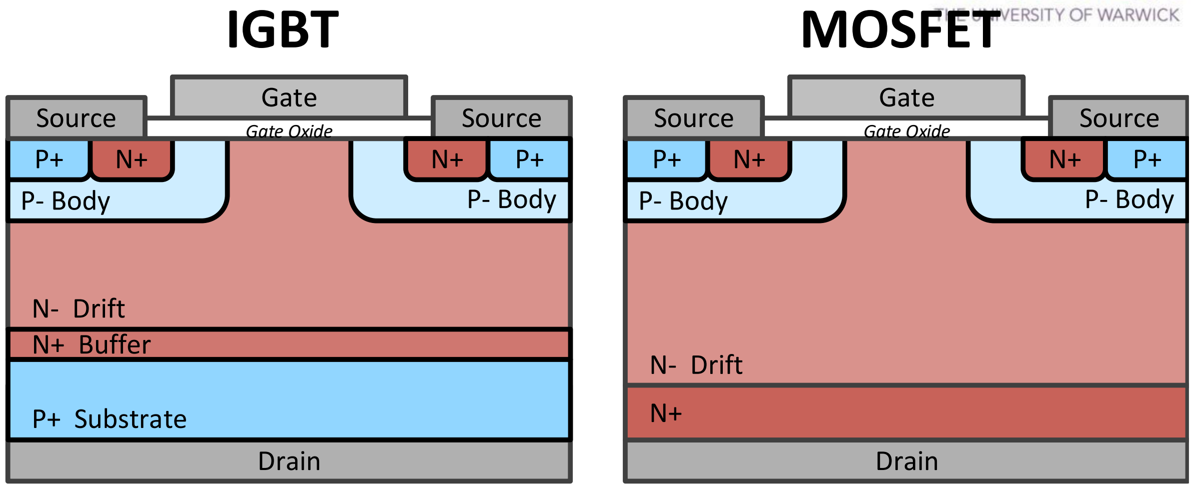
- However, this is a PiN diode and bipolar – not unipolar like the MOSFET.

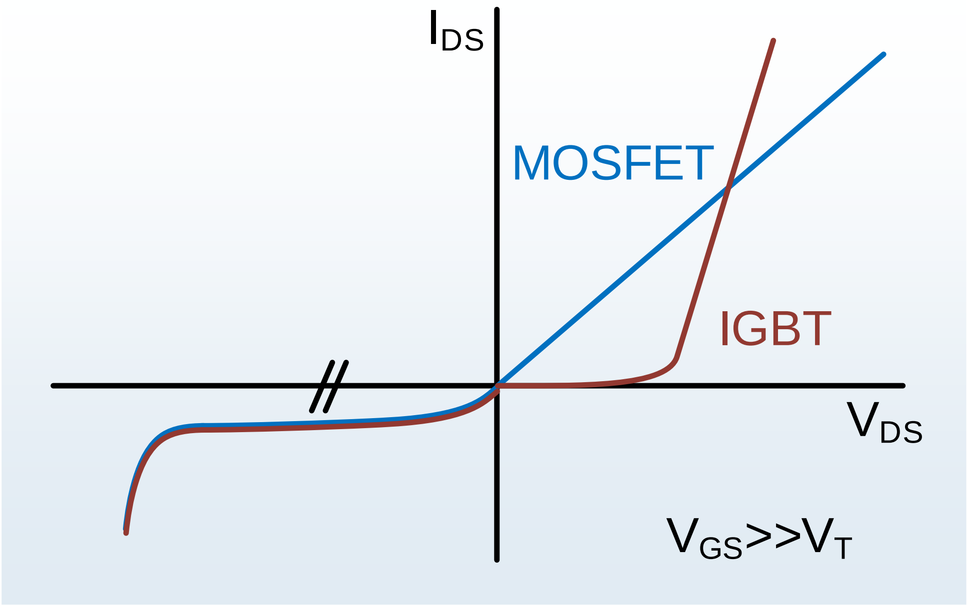


Infinieon 600V CoolMOS™ E6 Power MOSFET

Semiconductor Devices: IGBTs

- The Insulated Gate Bipolar Transistor (IGBT) is the bipolar equivalent of the unipolar MOSFET.
- A P+ region drain injects holes into the drift region, which meet the electrons from the source.
- Just like the PiN diode, this reduces conduction losses at the expense of switching losses.
- **More on IGBTs later!!**





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Underpinning Research

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The need for Wide Bandgap Power Electronics

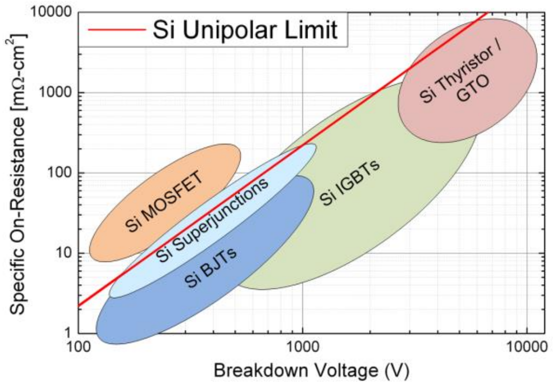
- Until the mid 2000s this was the status-quo, with silicon the only material in the power electronics market.

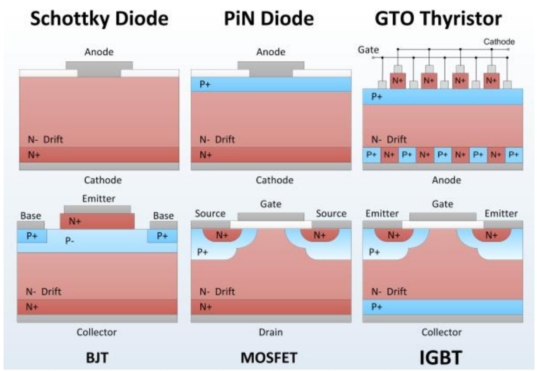
- Hence the choice was between Si unipolar or Si bipolar, high voltage or switching speed.

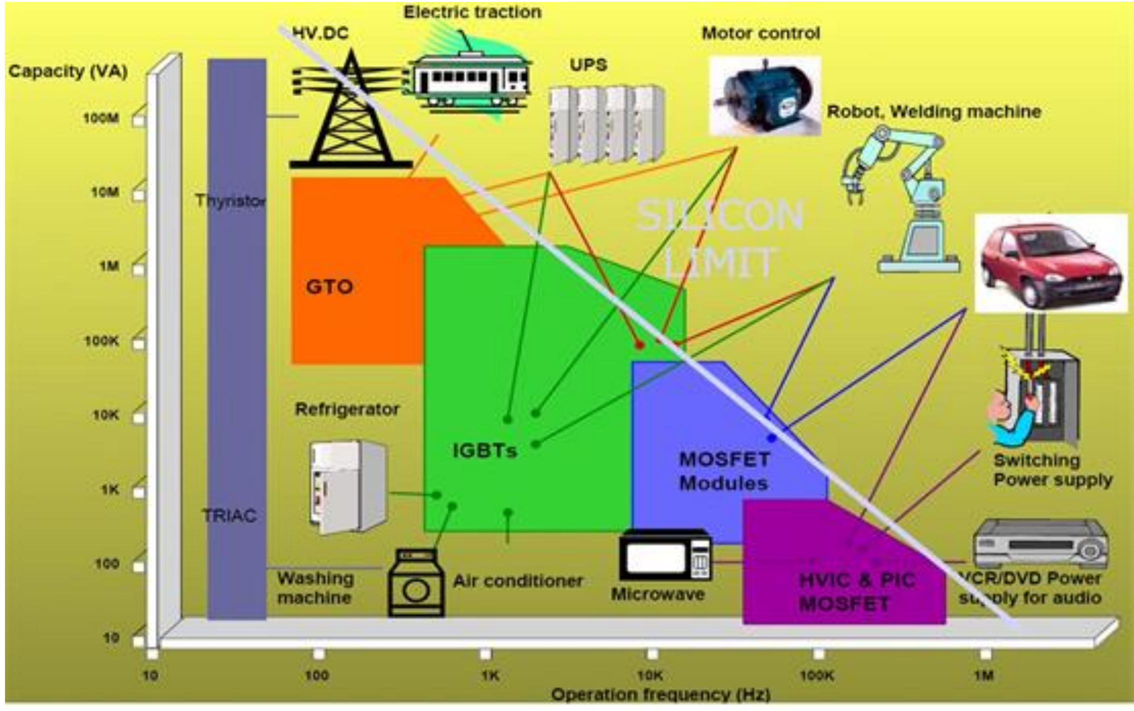
- In 2002 **SiC Schottky diodes** commercially available, followed by **SiC MOSFETs** in 2010.

  These are now available from 600-1700 V.

Here is why...!







The need for Wide Bandgap Power Electronics

To optimise On-Resistance:

$$R_{ON} = \frac{W_D}{AqN_D}$$

Minimise Drift Region Width (W_D)

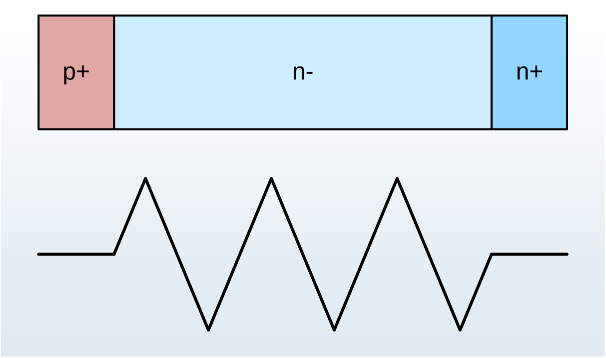
Maximise carriers (N_D)

To optimise Breakdown voltage:

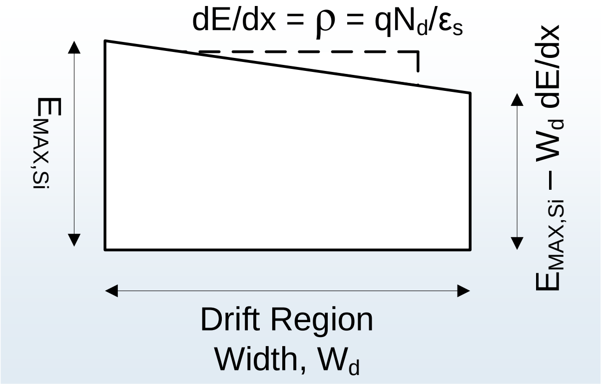
$$V_{BD} = W_D\left(E_{max,Si} - W_D\frac{qN_D}{2\varepsilon_s}\right)$$

Maximise Drift Region Width (W_D)

Minimise Drift Region Doping (N_D)



$$E_{max,SiC} = 10 \times E_{max,Si}$$



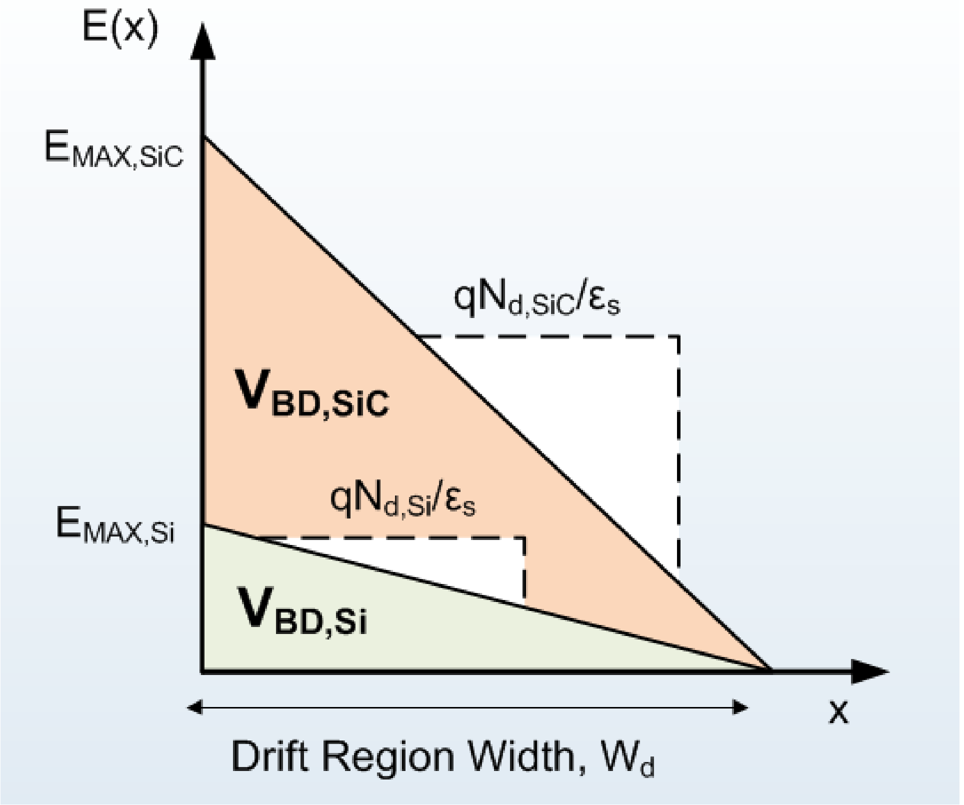
The need for Wide Bandgap Power Electronics

	Silicon	SiC	GaN	Diamond
Bandgap, E_G (eV)	1.1	3.26	3.45	5.5
Critical Electric Field, E_{max} (MV/cm)	0.25	2.2	3	5

A 10x increase in E_{max} can be exploited in two ways:

1. Keep W_D the same:

- V_{BD} greatly increased: $V_{BD,SiC} \approx 10V_{BD,Si}$
- Max possible doping can be increased, $N_{D,SiC} \approx 10N_{D,Si}$
- SiC device has higher V_{BD} AND lower R_{ON}.



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The need for Wide Bandgap Power Electronics

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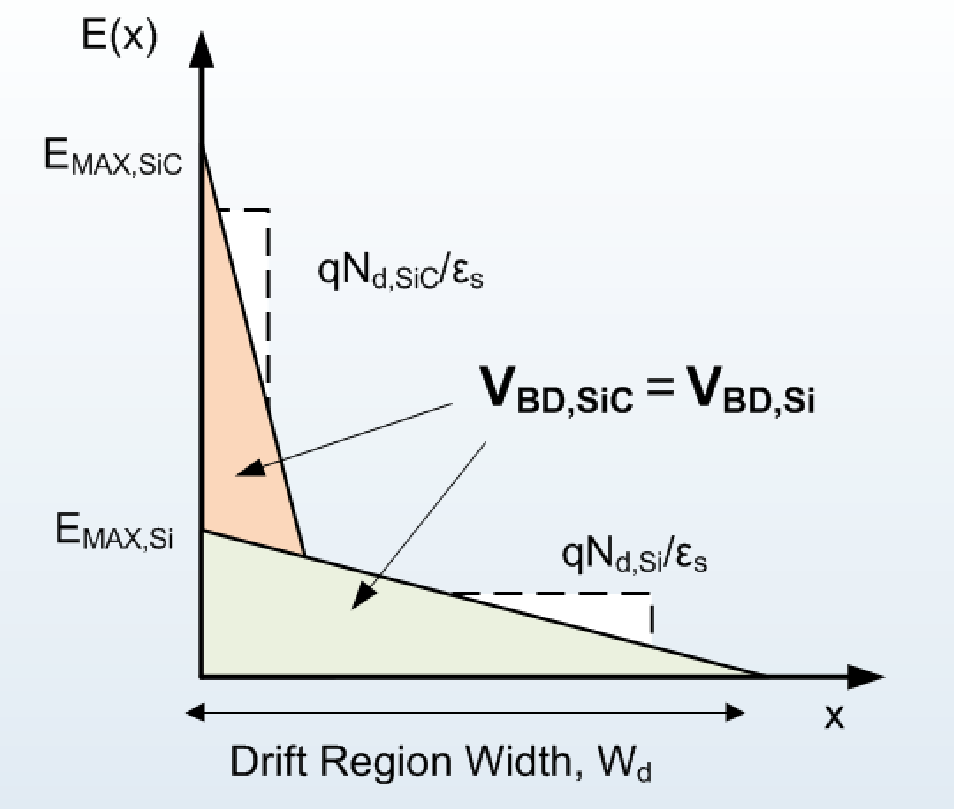
Critical Electric Field, E_{max} (MV/cm)	0.25	2.2	3	5

A 10x increase in E_{max} can be exploited in two ways:

2. Keep V_{BD} the same:

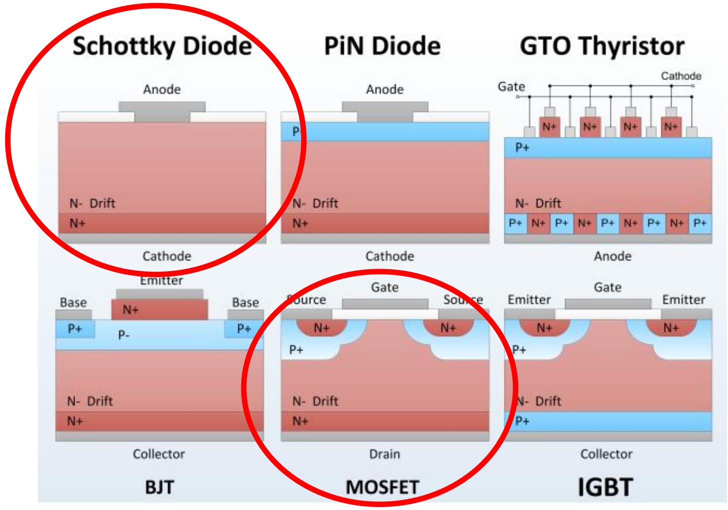
- W_D greatly decreased: $10\ W_{D,SiC} \approx W_{D,Si}$
- Max possible doping can be vastly increased, $N_{D,SiC} \approx 100\ N_{D,Si}$
- Both benefit R_{ON}! $500\ R_{ON,SiC} \approx R_{ON,Si}$.

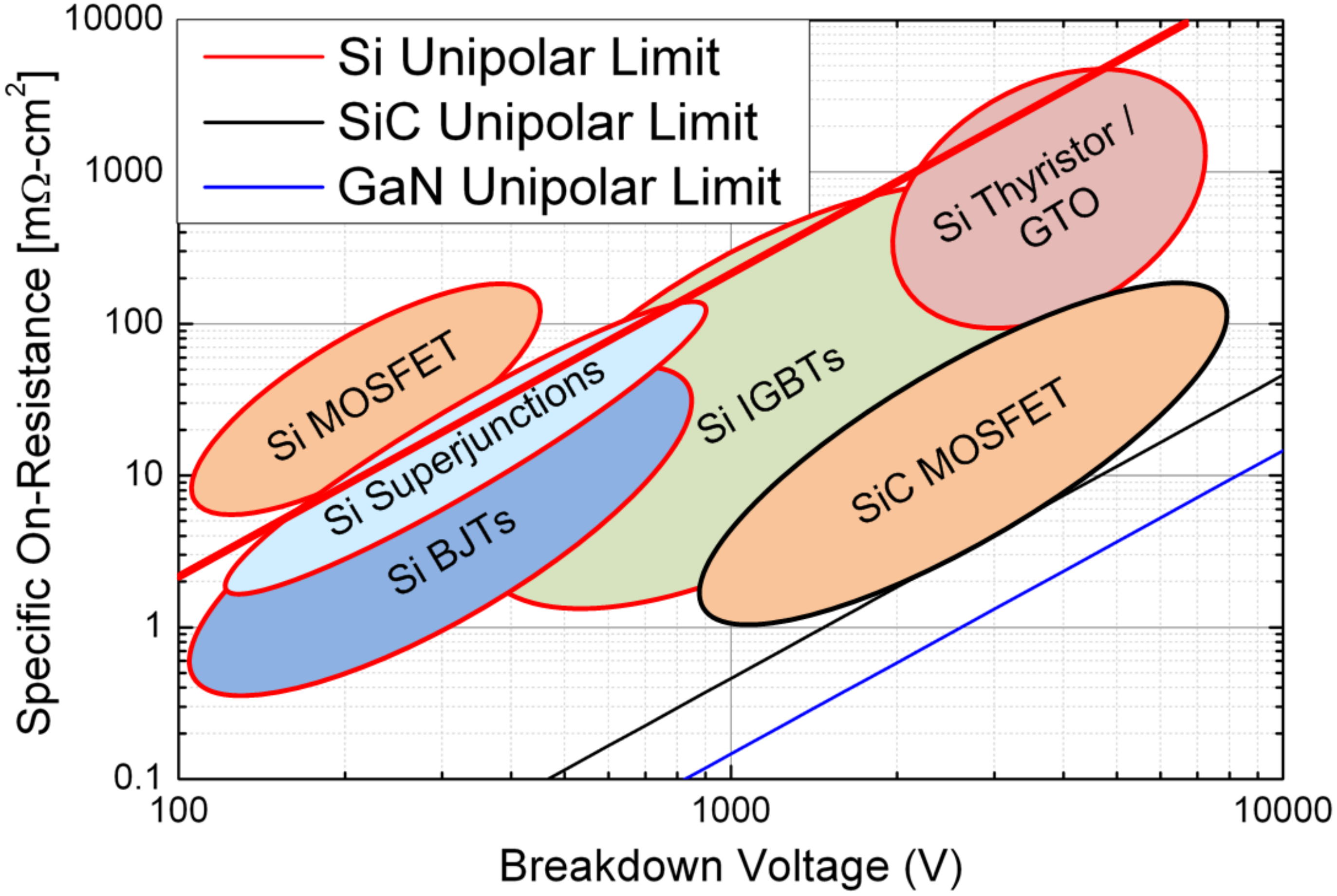


The need for Wide Bandgap Power Electronics

The increase in E_{max} is responsible for a much reduced unipolar limit in the WBG semiconductors compared to Si.

Now there are WBG unipolar devices capable of competing against the IGBT and GTO, offering a much faster switching solution.





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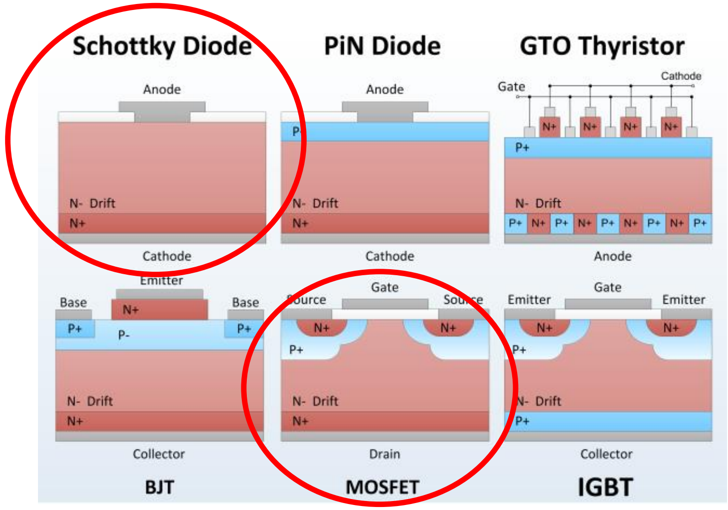

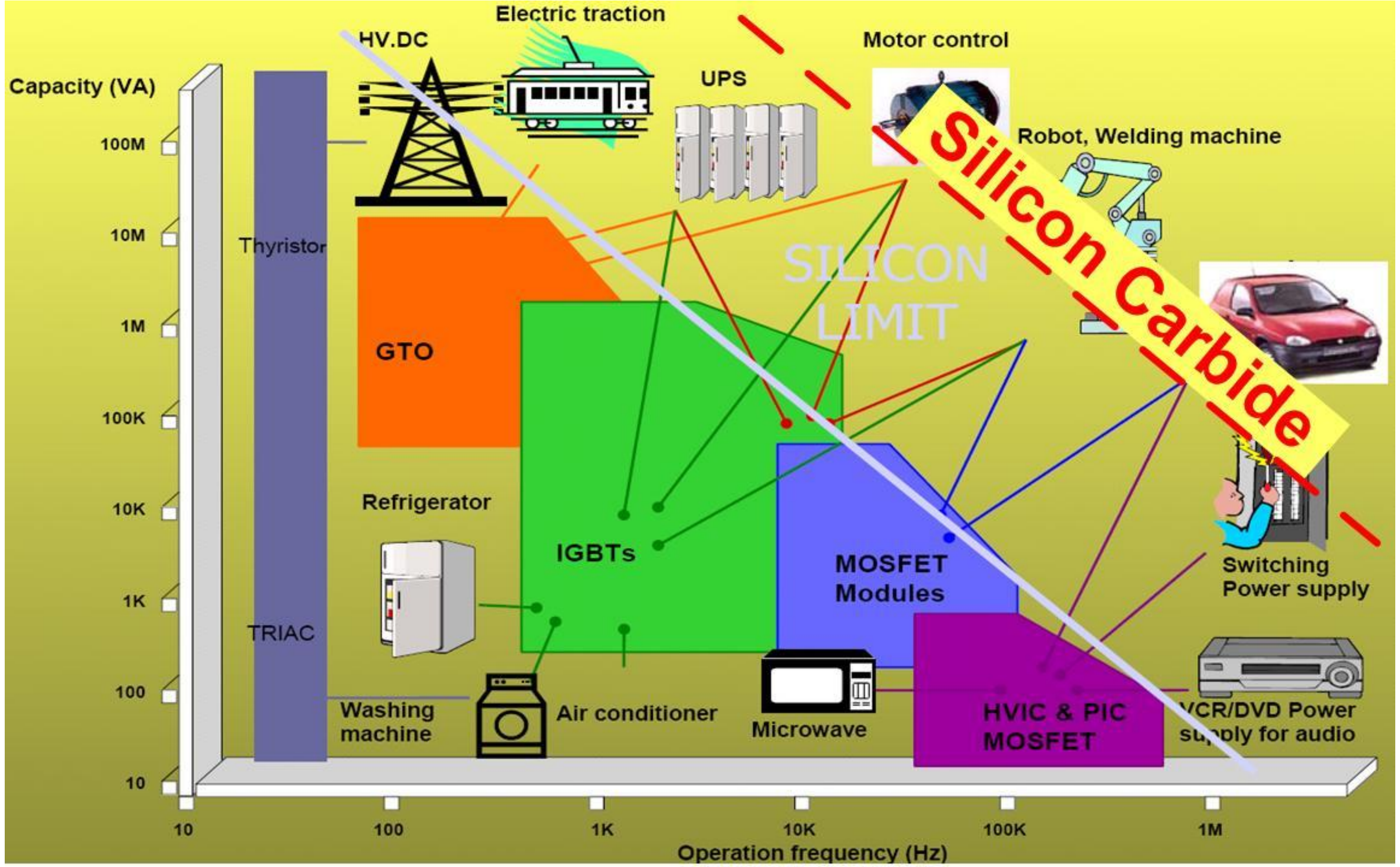

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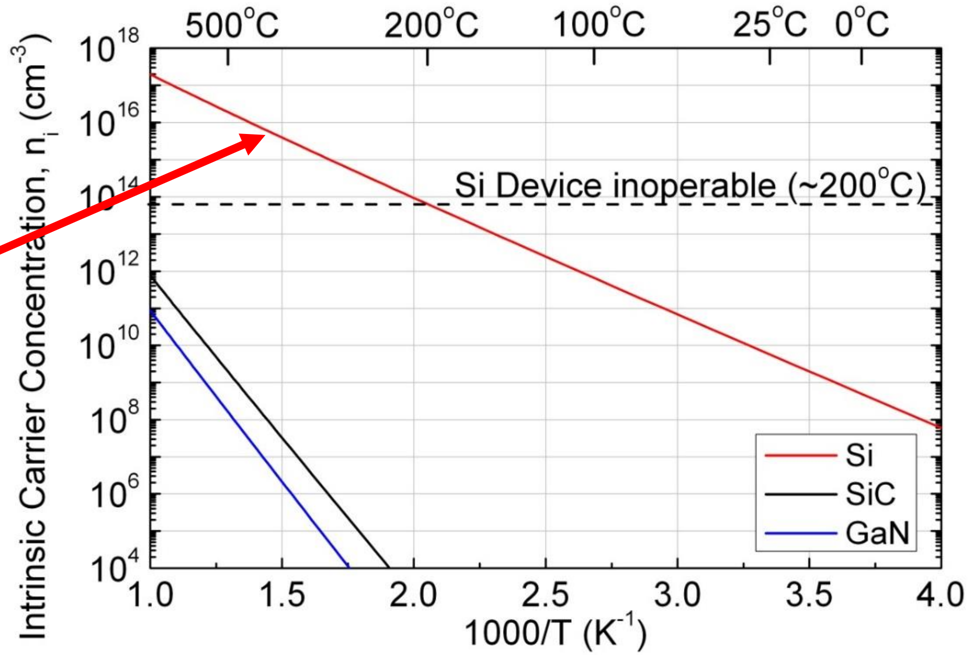
The need for Wide Bandgap Power Electronics

	Silicon	SiC	GaN	Diamond
Bandgap, E_G (eV)	1.1	3.26	3.45	5.5
Thermal Conductivity (W/cmK)	1.5	3.8	1.3	20

Thermal performance is also greatly improved.

- 2.5x T.C. improvement over Si allows heat to easily be removed
- The wide the bandgap means few carriers at high temperature:

$$n_i = \sqrt{N_C N_V} \exp\left(-\frac{qE_G}{2kT}\right)$$



The need for Wide Bandgap Power Electronics

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Critical Electric Field, E_{max} (MV/cm)	0.25	**2.2**	**3**	**5**
Thermal Conductivity (W/cmK)	1.5	**3.8**	1.3	**20**
Natural Oxide	**SiO_2**	**SiO_2**	No	No
Electron Mobility, μ_n (cm^2/Vs)	1400	900*	1000**	1800
Wafer Size	**12"+**	6"	<2"	<2"
Defect Density (cm^{-2})	**< 1**	~1000	10^6 - 10^8	
Cost	**Very Low**	High	Med-High	Very High

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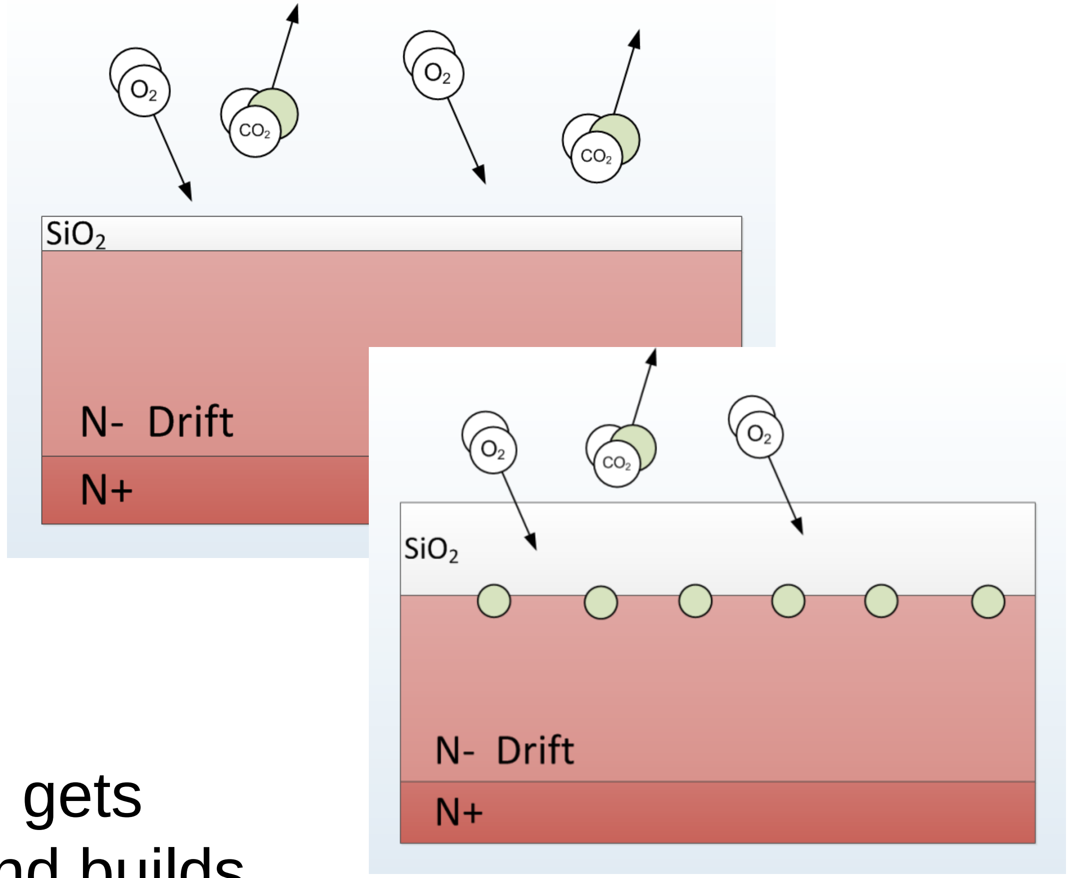
The need for Wide Bandgap Power Electronics

A big advantage that SiC has over GaN and diamond is that it can be thermally oxidised to form SiO_2. However, the presence of the carbon causes significant problems.

During oxidation at >1200C, SiO_2 is initially formed and the carbon is dispersed as CO_2.

$SiC + 2O_2 + \text{energy} = SiO_2 + CO_2$



As the layer gets thicker, the carbon gets trapped by the existing SiO_2 layer and builds up at the SiC/SiO_2 interface.

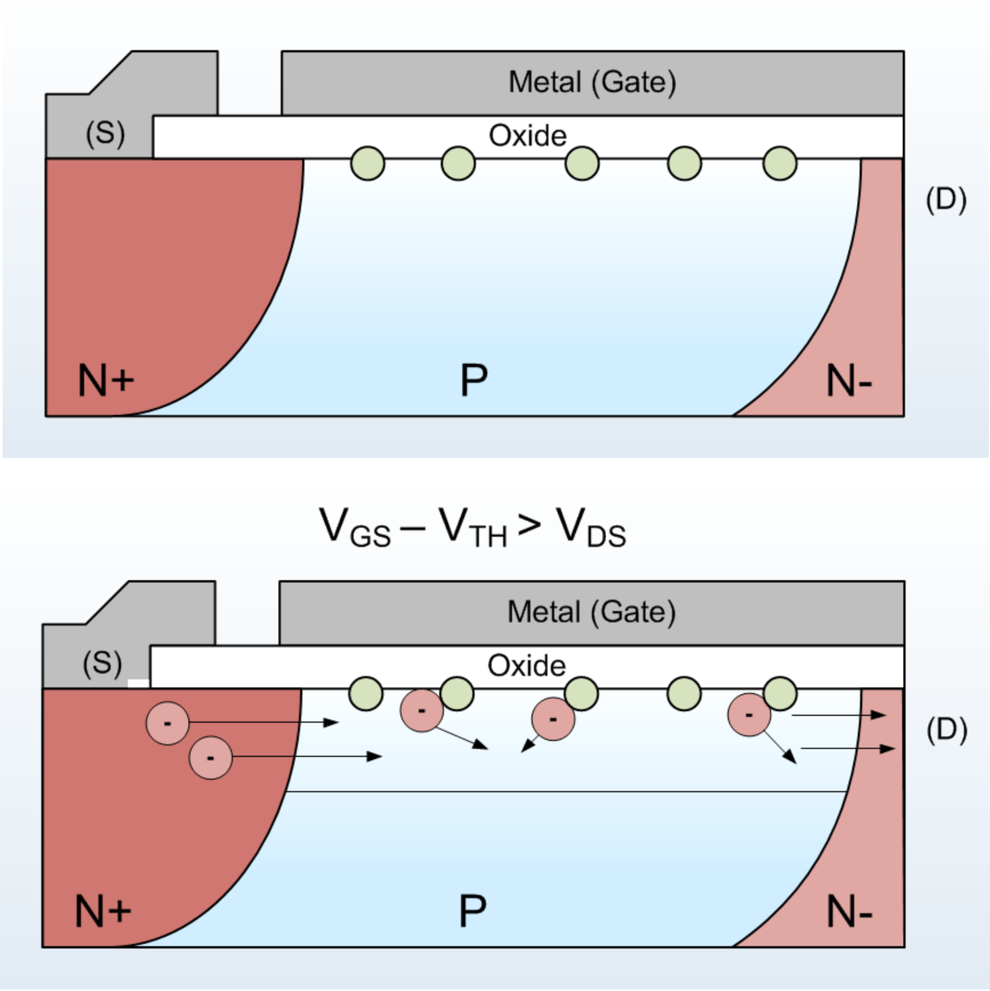
The need for Wide Bandgap Power Electronics

The result of the trapped charge at the SiC/SiO2 interface is the presence of foreign particles within the channel region of the SiC MOSFET.

The trapped carbon scatters electrons as they pass through the channel, so decreasing the channel mobility (μ_{Ch}) of a SiC MOSFET.

A channel mobility of less than 50 cm^2/Vs is typical for SiC. In Si μ_{Ch} is > 500 cm2/Vs.

$$I_D = \mu_{ch} C_{Ox} W (V_{GS} - V_T)^2 / 2L$$



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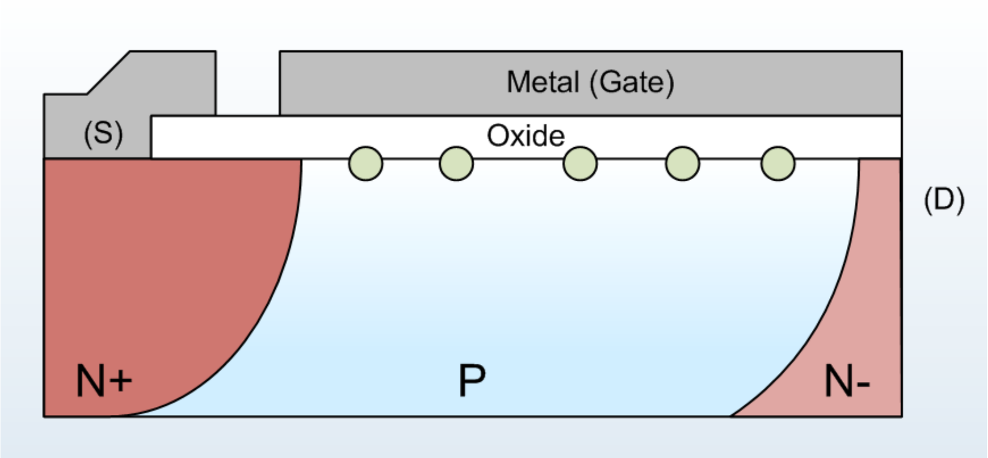
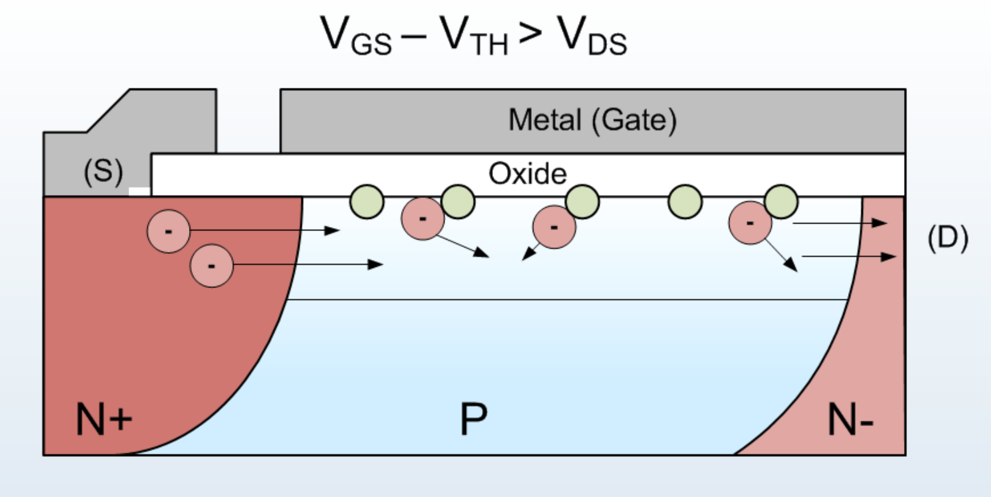
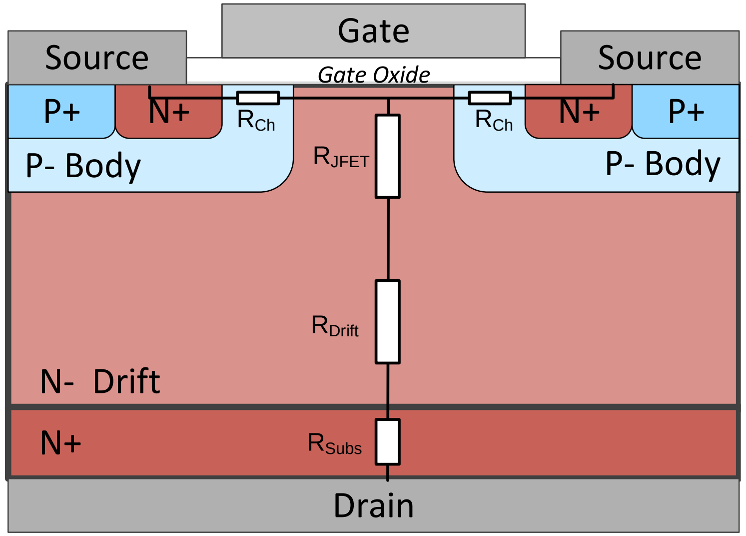


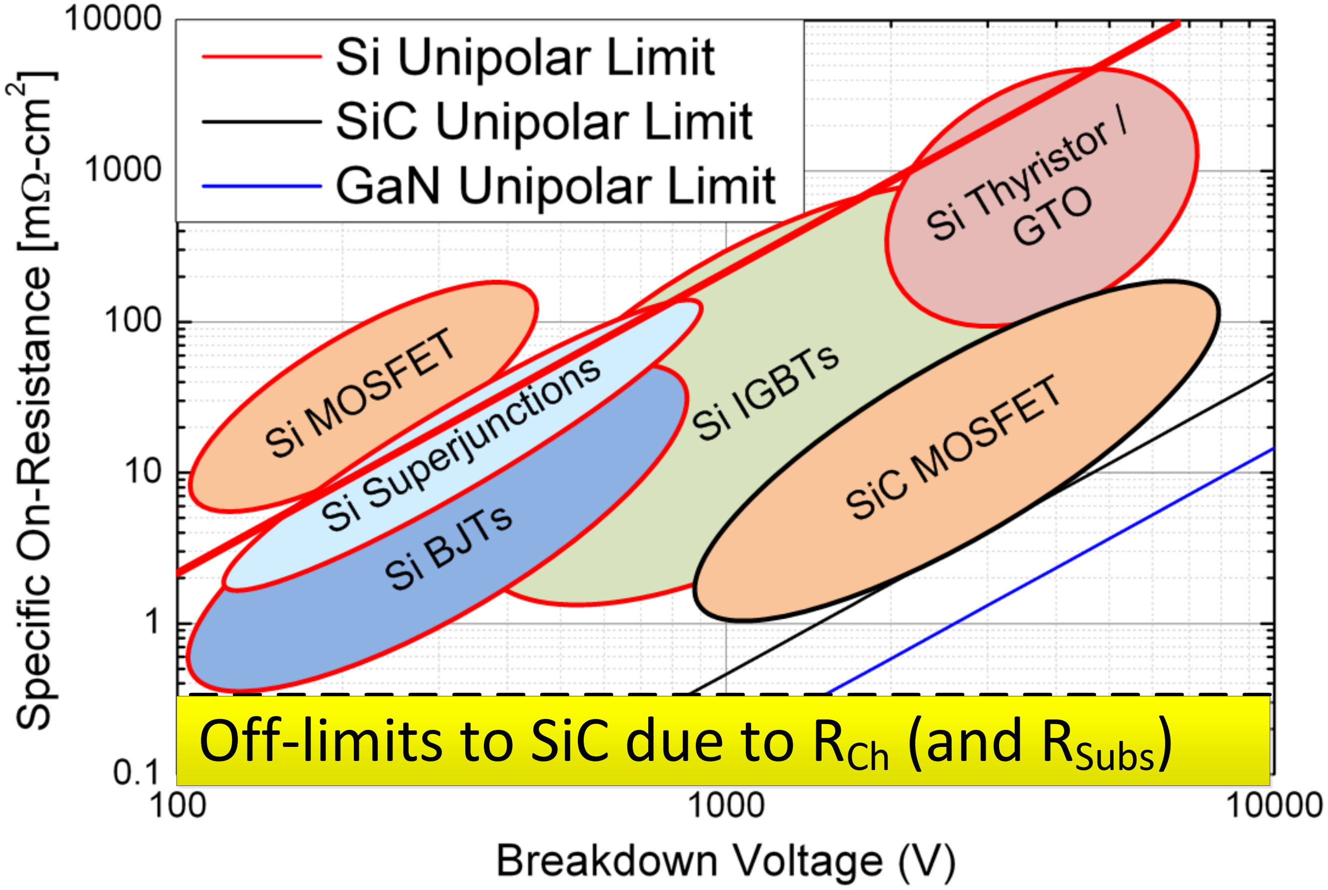


The need for Wide Bandgap Power Electronics

Below 600 V, R_{drift} will continue to reduce but R_{Ch} will not due to the poor channel mobility. This limits how far SiC can be downscaled in voltage

Work is also still required to minimise R_{SUBS} by thinning the thick, high resistance substrates of SiC.

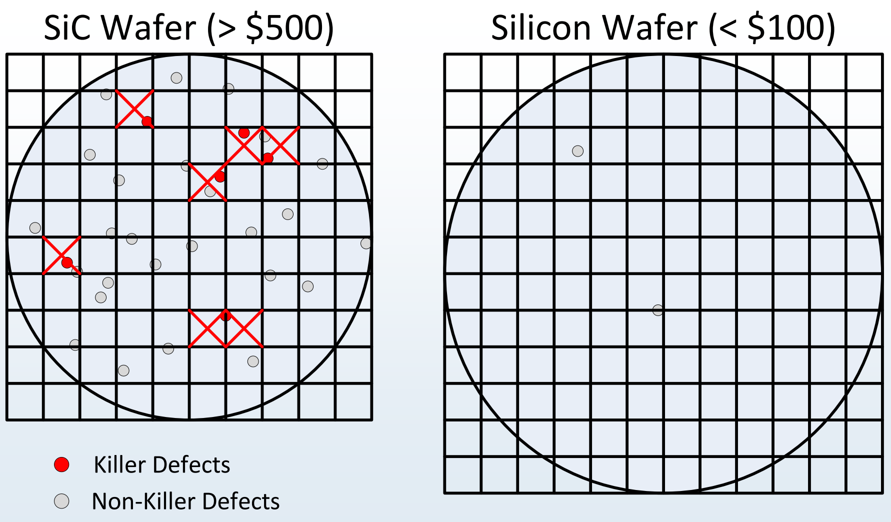




The need for Wide Bandgap Power Electronics

Other outstanding issues with SiC include:

- High cost: market forces helping.
- Material quality and size: SiC wafers now 6” (compared to 12”+ in Si) and defect densities are coming down. “Killer” defects now eliminated but “non-killer” defects still limit bipolar devices.
- Reliability. Long term stability of the devices – Short Circuit withstand time, oxide stability etc. – all need improvement. (More Later)



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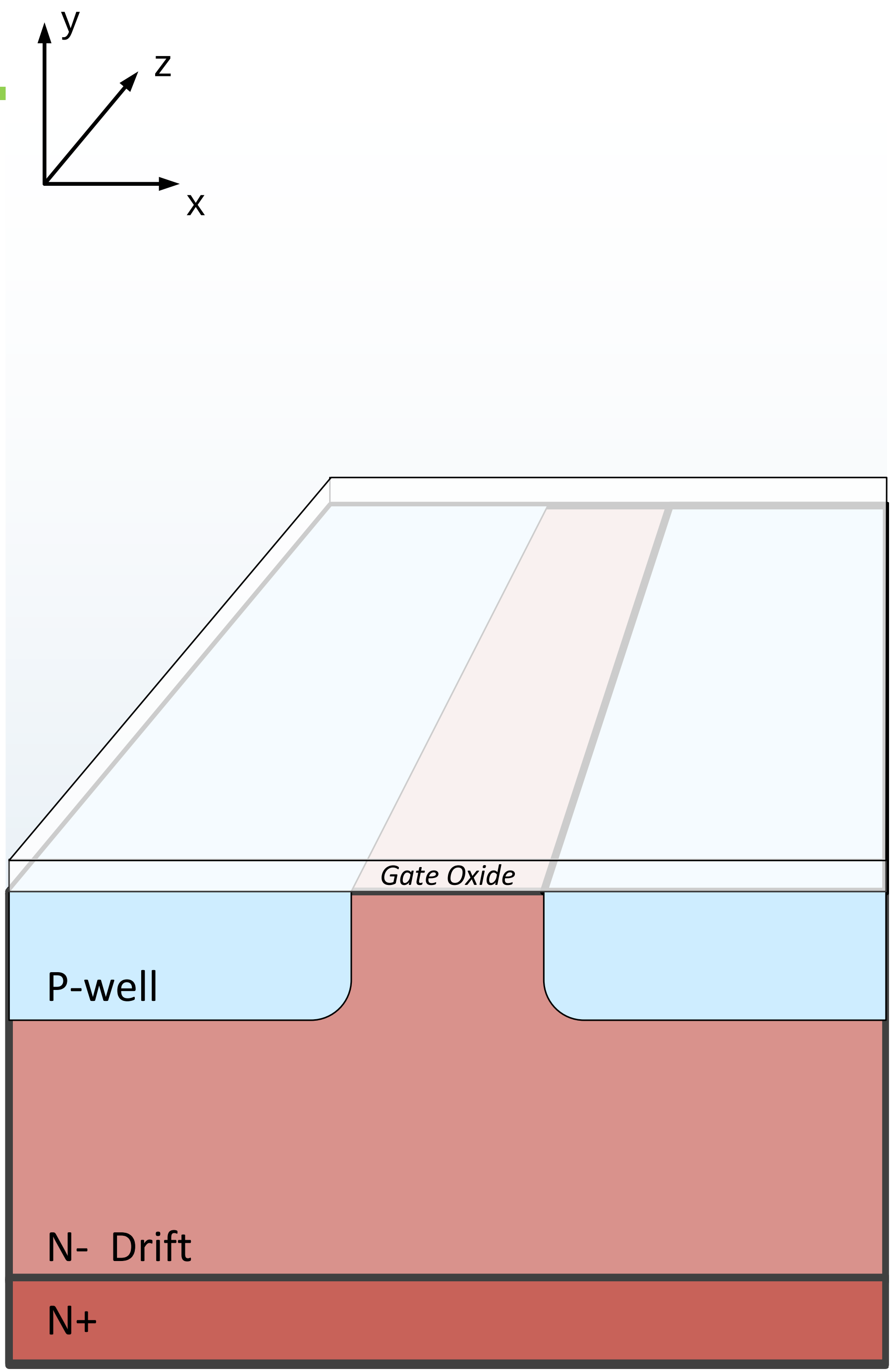
Fabricating a SiC Power MOSFET

MOSFET Fabrication is a long complex process, involving numerous stages:

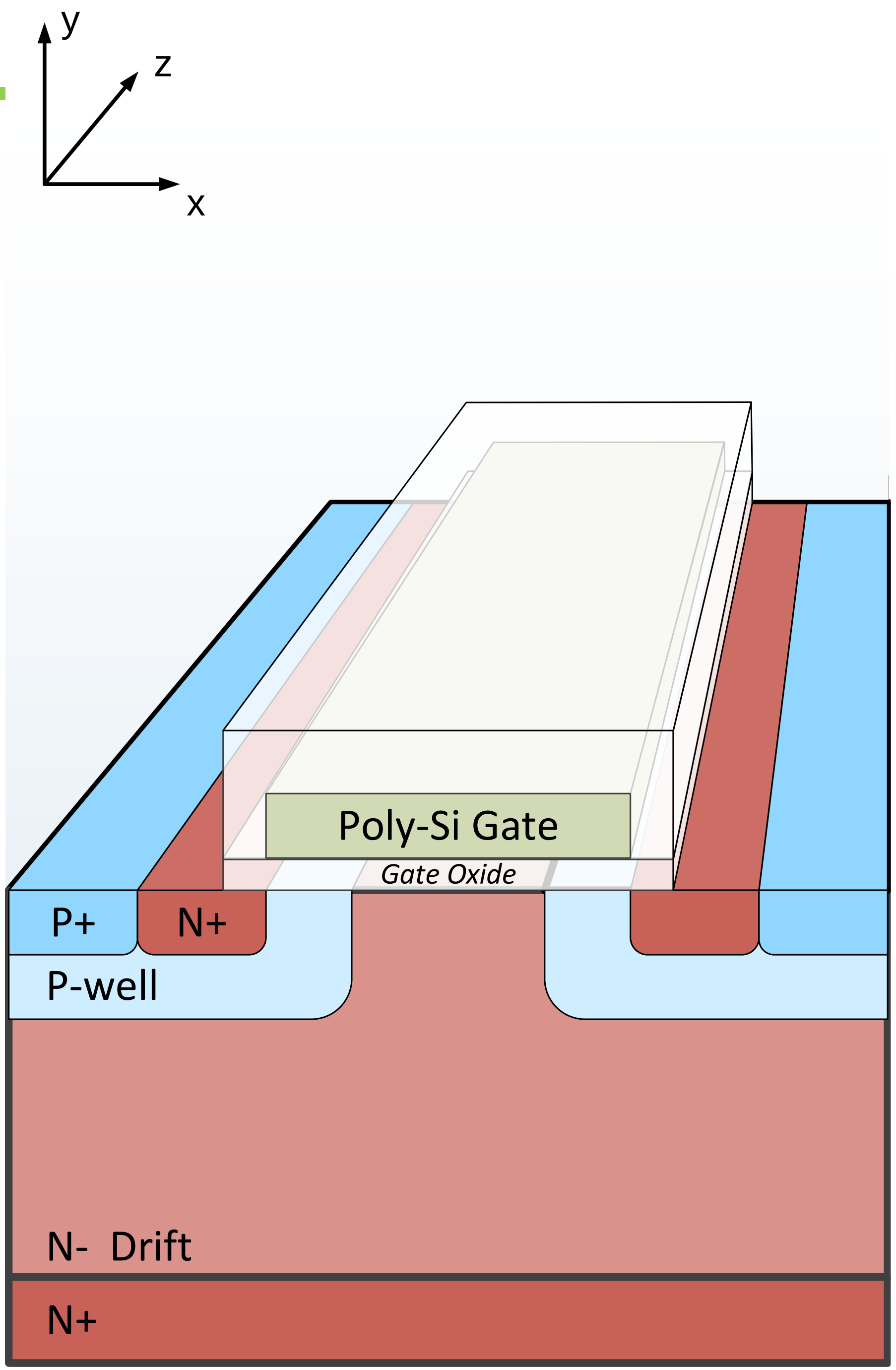
- N+ SiC substrate bought from Cree etc.
- Growth of the drift region in a CVD epitaxial process.
- Ion-Implantation of the P-well regions.
- Thermal oxidation to form the gate oxide. N2O post-oxide anneal to improve μ_{Ch}



Fabricating a SiC Power MOSFET

MOSFET Fabrication is a long complex process, involving numerous stages:

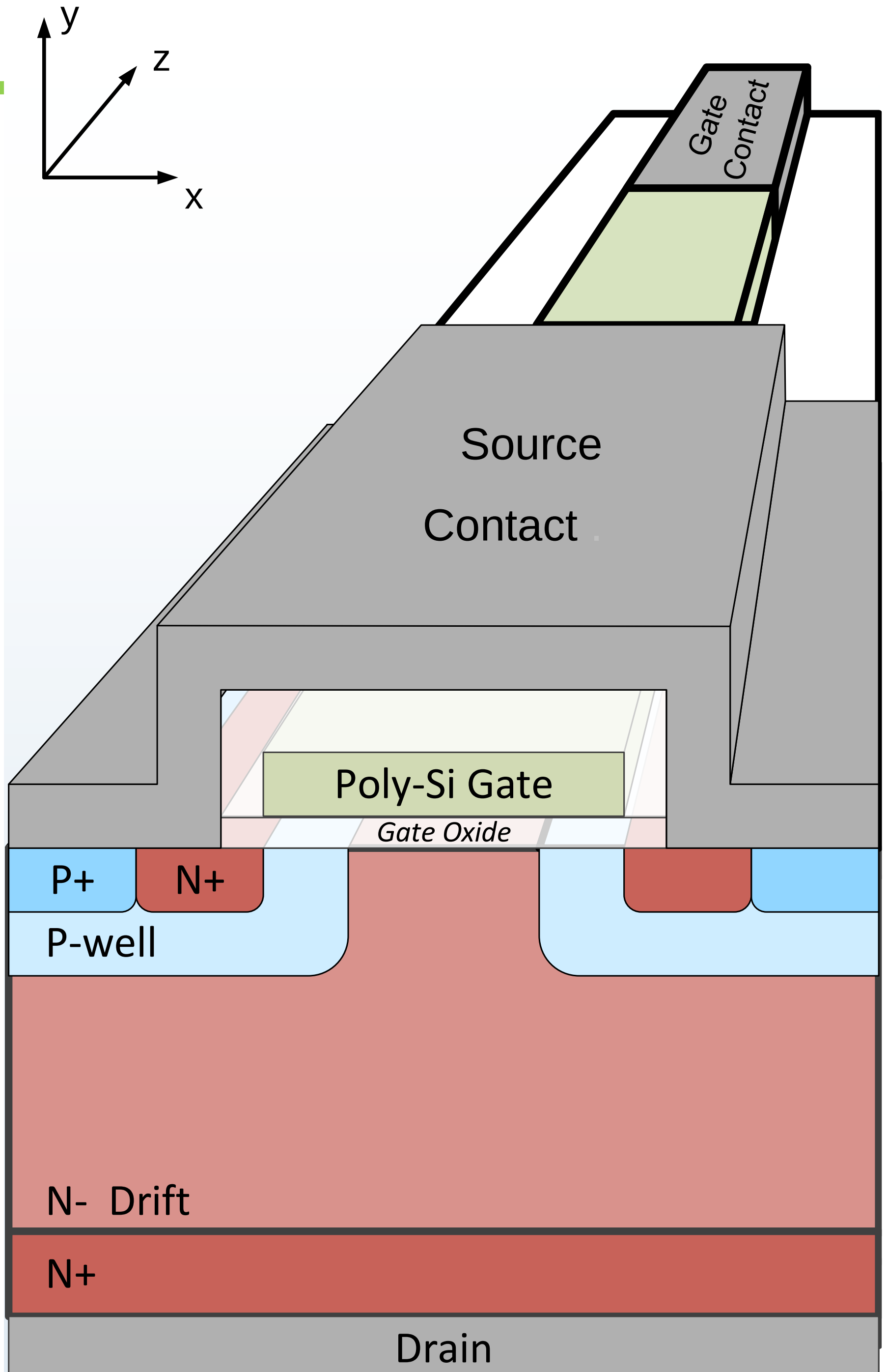
- Deposition of a Polycrystalline Si Gate by PECVD. Etch back to oxide.
- Dip in hydrofluoric acid to remove oxide
- Ion-Implantation of the P+ and N+ source regions.
- Oxidation of the poly-Si gate to form spacers.



Fabricating a SiC Power MOSFET

MOSFET Fabrication is a long complex process, involving numerous stages:

- Formation of source contacts by metal evaporation and/or sputtering
- Formation of metal drain contact on backside.
- Formation of metal gate contact in the third dimension, at the end of the 'fingers'



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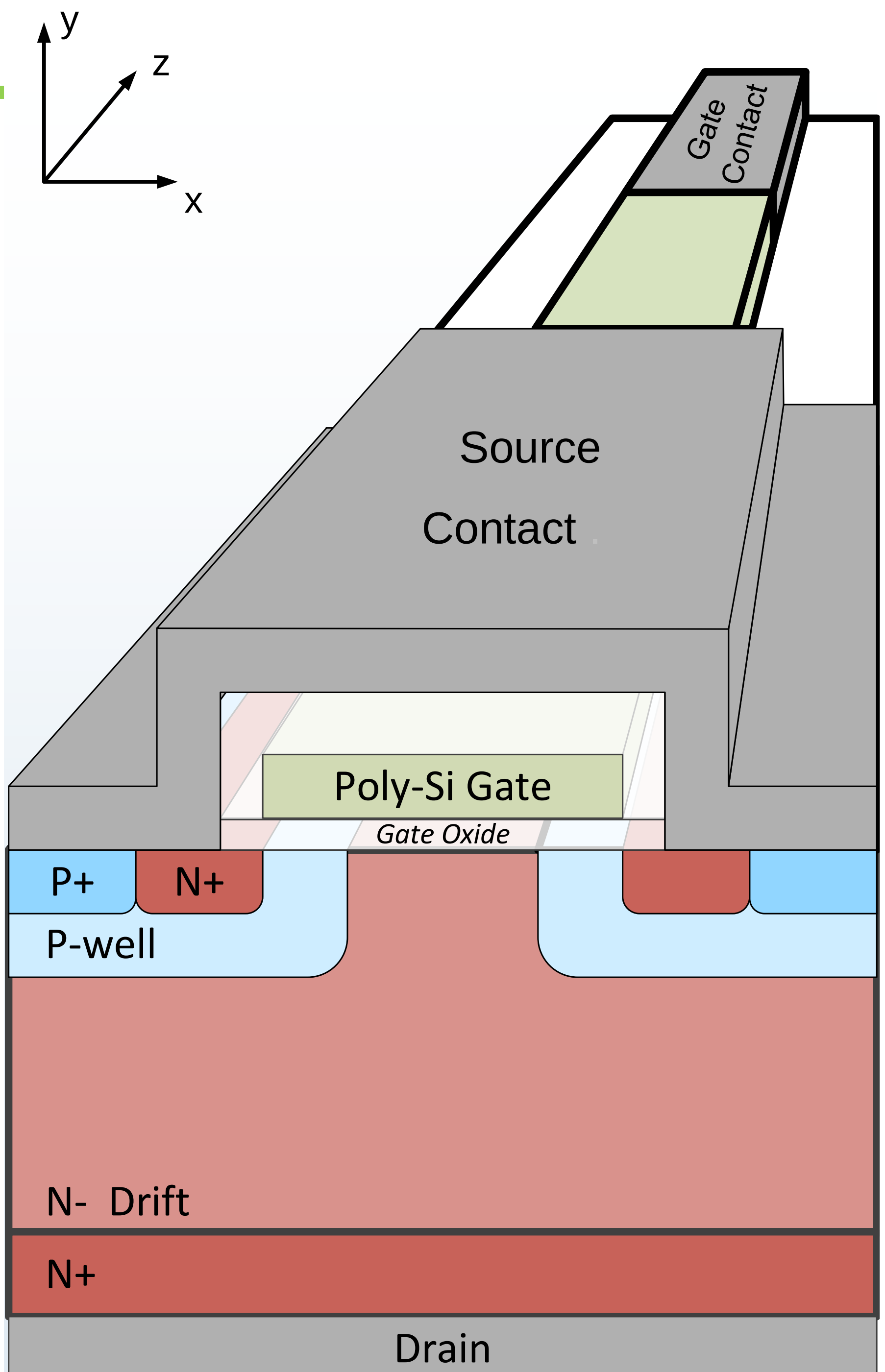
- PN junctions
- Diodes: off-state characteristics of power devices
- Diodes: on-state and the unipolar limit
- Power MOSFETs and IGBTs
- The need for wide-bandgap power devices
- Device Fabrication
- **State of the art SiC power MOSFETs**

Optimising the SiC Power MOSFET

- To optimise a MOSFET, the goal is first to minimise the resistance ($R_{DS,ON}$; $\Omega.cm^2$) of the device.
- Low $R_{DS,ON}$ reduces the semiconductor area required to achieve a desired current rating.
- This in turn maximises yield and reduces cost.
- Reducing switching losses and ensuring reliability are maintained are also important factors.

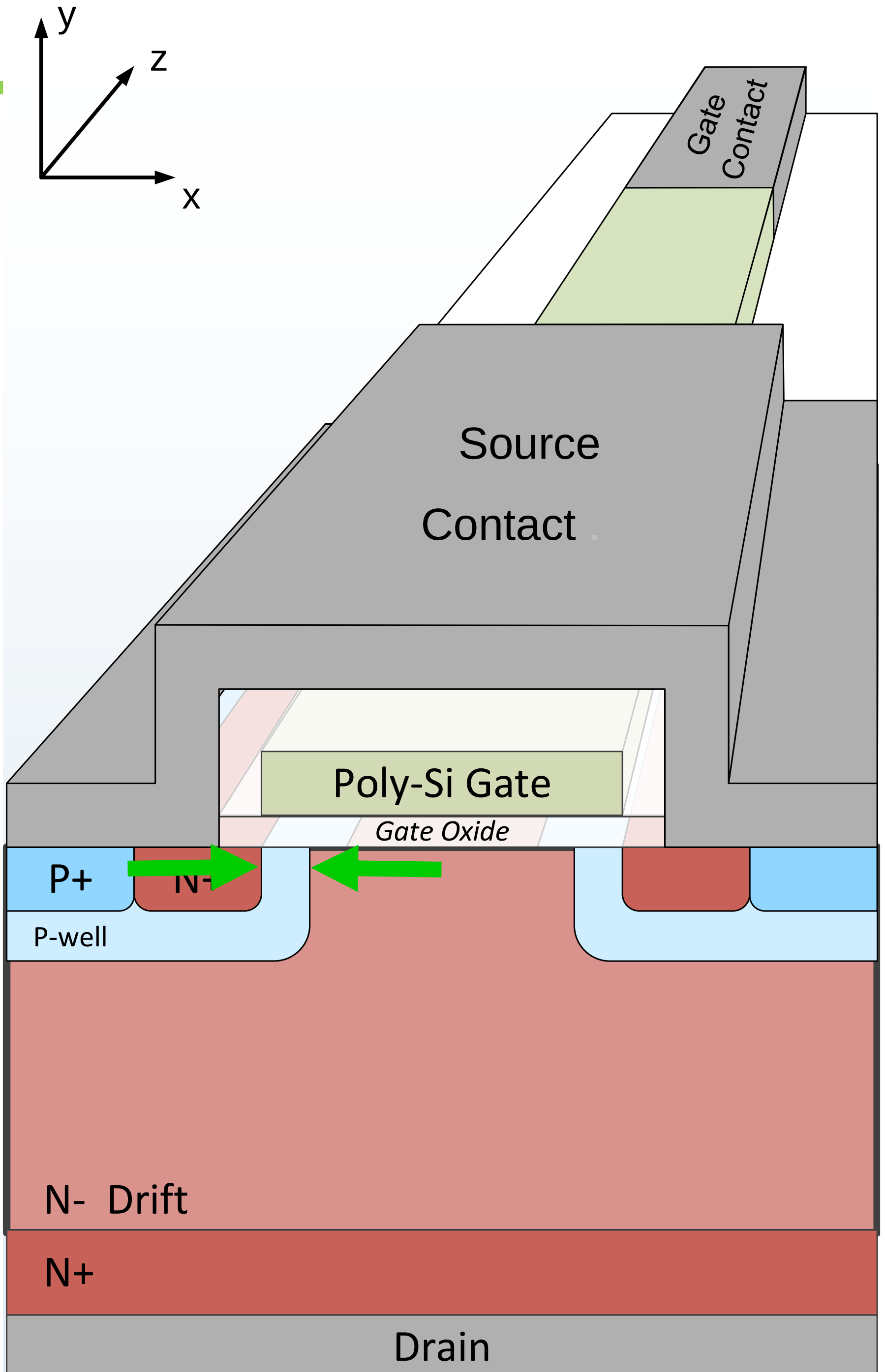


Optimising the SiC Power MOSFET

Methods to optimise the Power MOSFET

1. Shrink the channel length to minimise channel resistance. However risk of punchthrough in the off-state!

$$R_{ON} = R_{Drift} + R_{JFET} + R_{Ch} + R_{Subs} + R_{Other}$$



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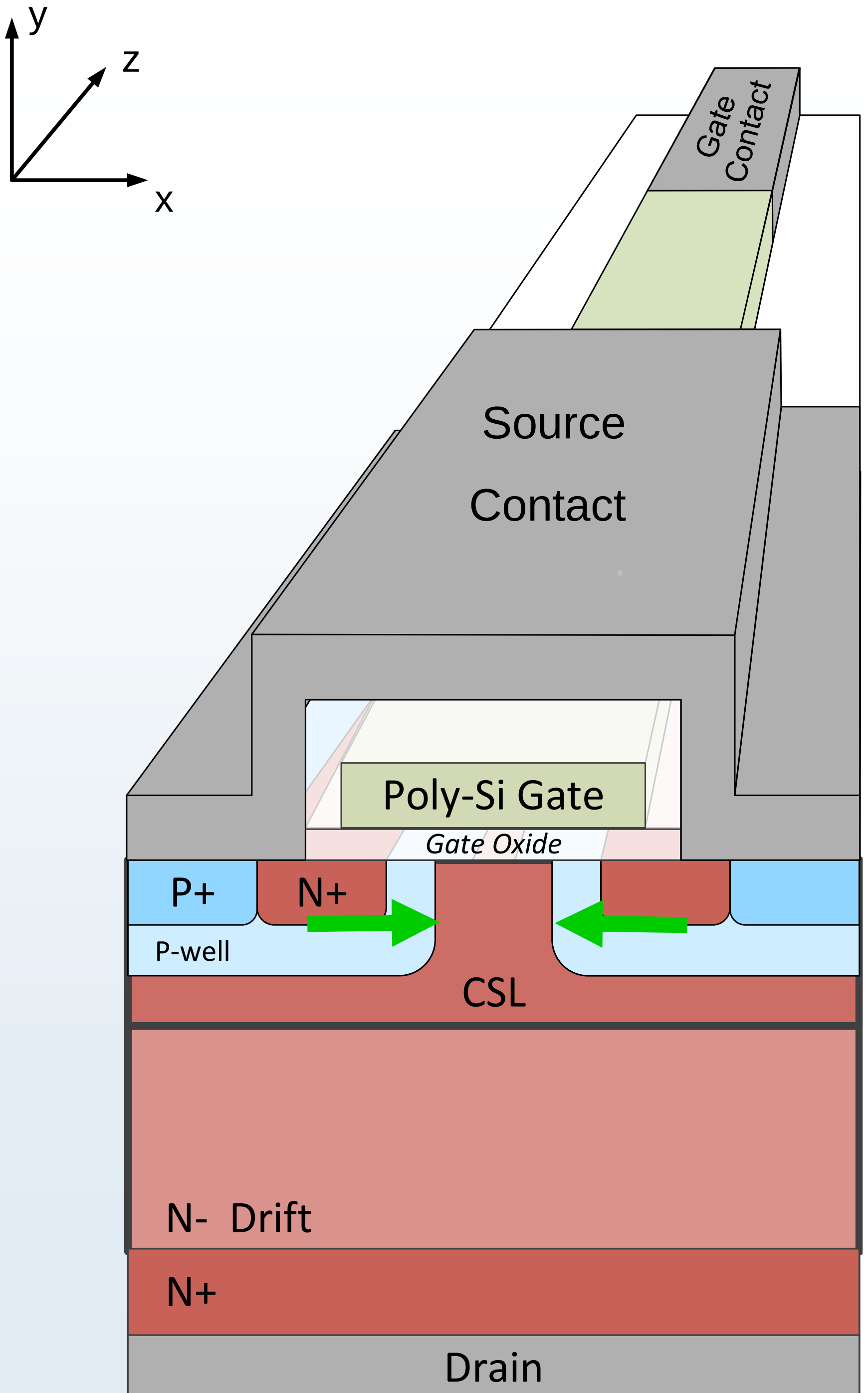
1. Shrink the channel length to minimise channel resistance. However risk of punchthrough in the off-state!

2. Minimise JFET Resistance by adding a Charge Storage Layer. This highly doped region allows the JFET width to be reduced

$$R_{ON} = R_{Drift} + R_{JFET} + R_{Ch} + R_{Subs} + R_{Other}$$



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1. Shrink the channel length to minimise channel resistance. However risk of punchthrough in the off-state!

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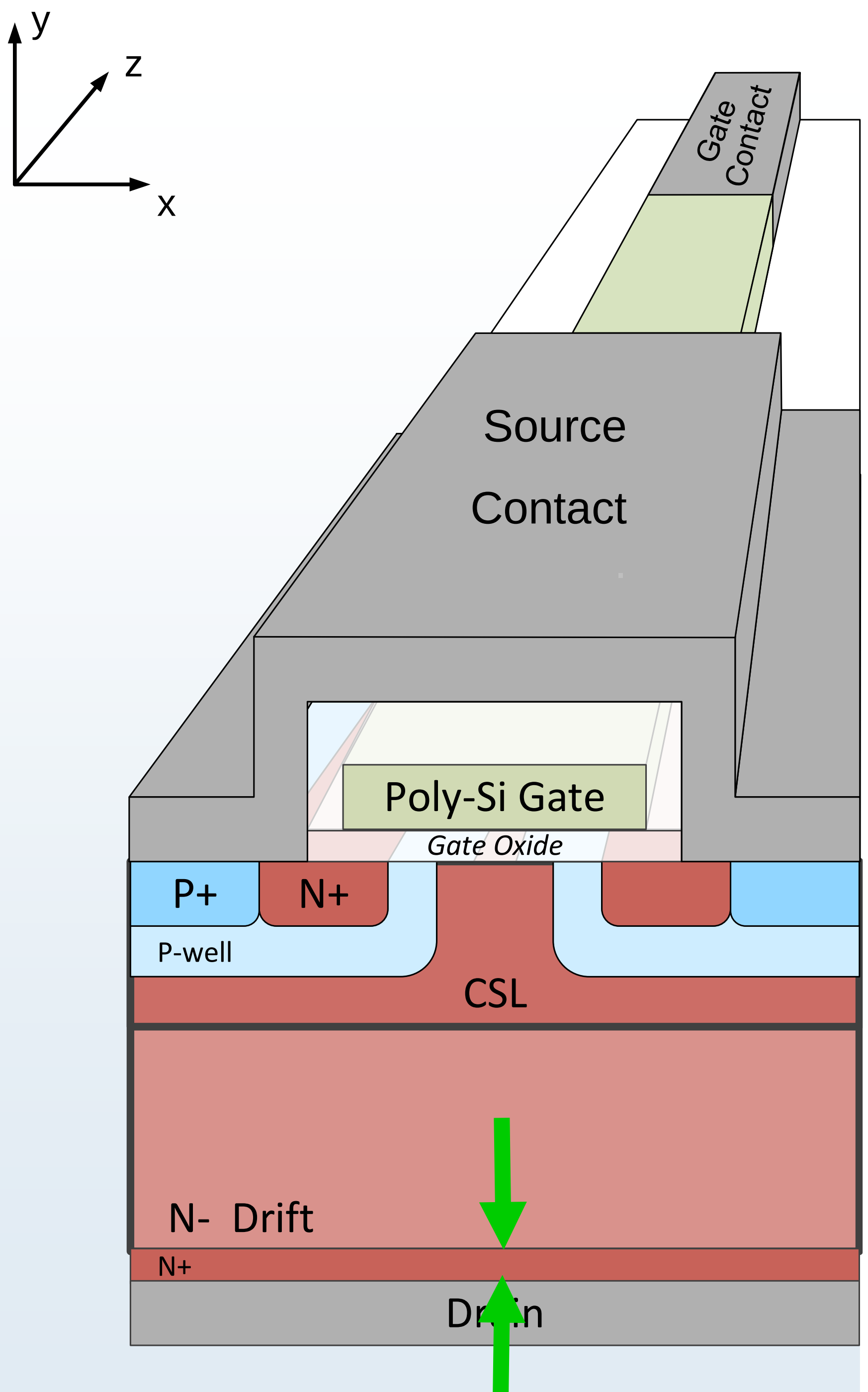
3. Thin the high resistance SiC Substrate

$$R_{ON} = R_{Drift} + R_{JFET} + R_{Ch} + R_{Subs} + R_{Other}$$



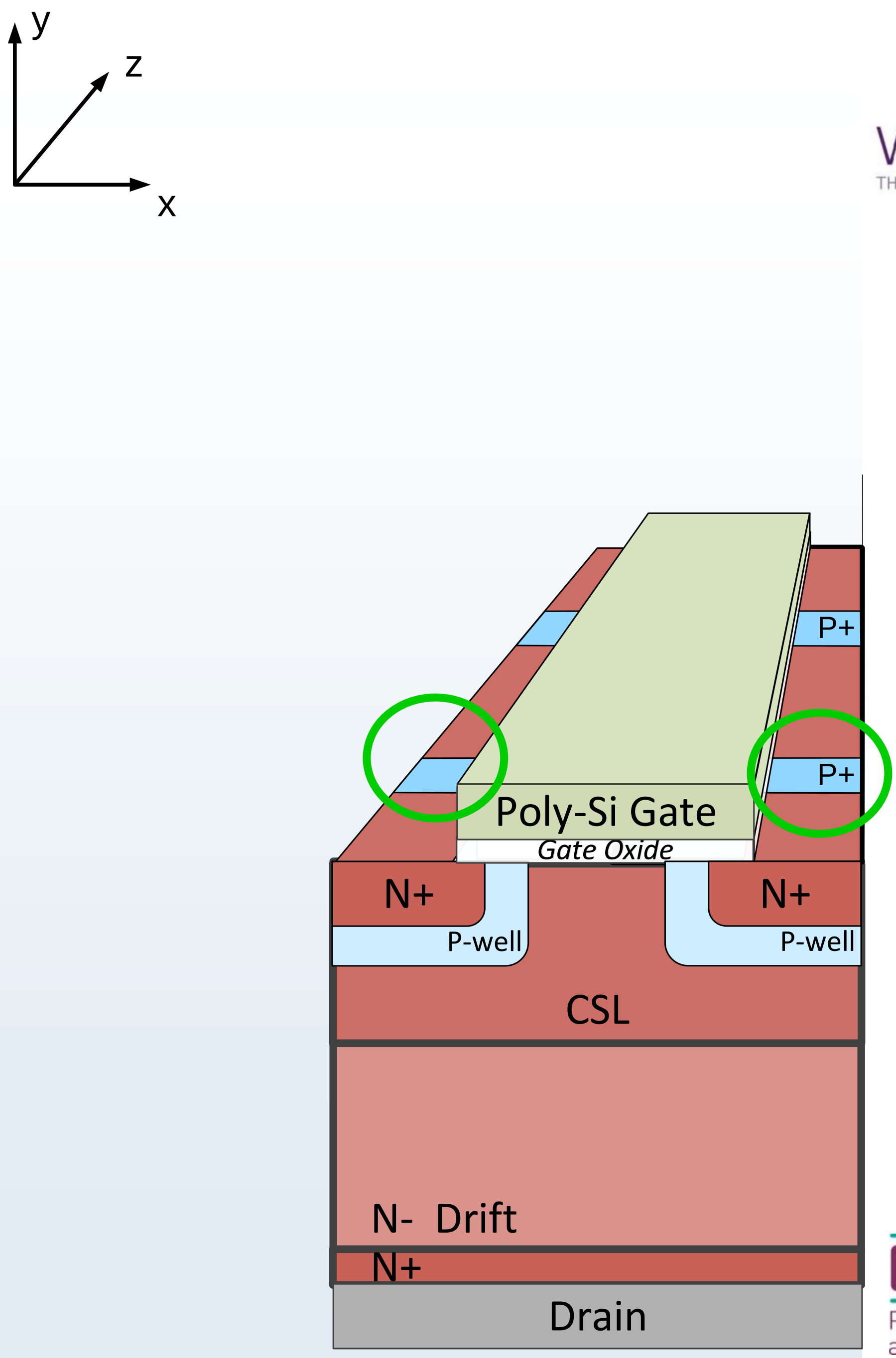
Optimising the SiC Power MOSFET

Methods to optimise the Power MOSFET

4. Move the P+ contacts into the third dimension. This minimises the device area, reducing cost.

This is also used to improve device ruggedness.

£££/Amp



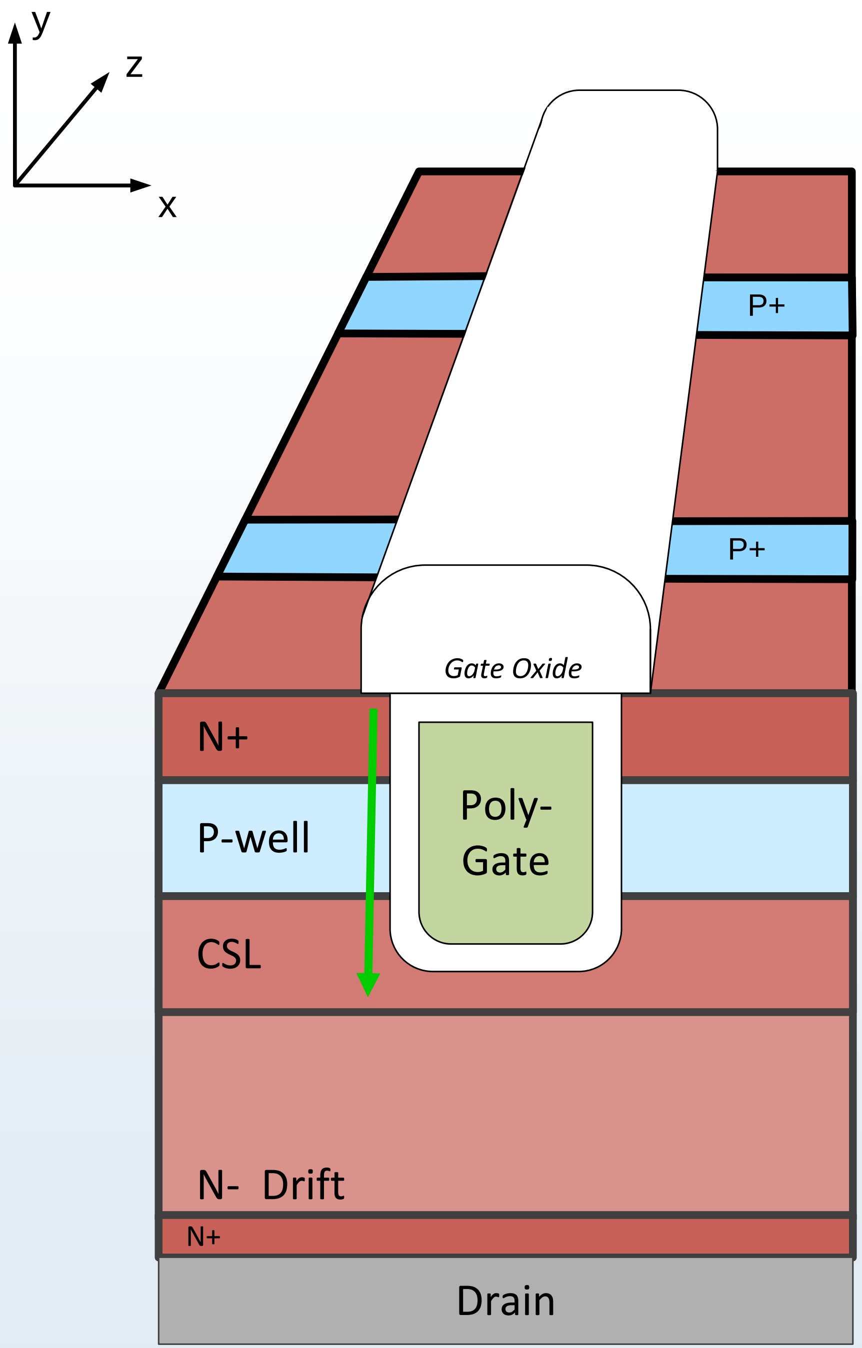
Optimising the SiC Power MOSFET

Methods to optimise the Power MOSFET

5. Move to a Trench Gate structure. This means the gate is now vertical. This has multiple advantages:

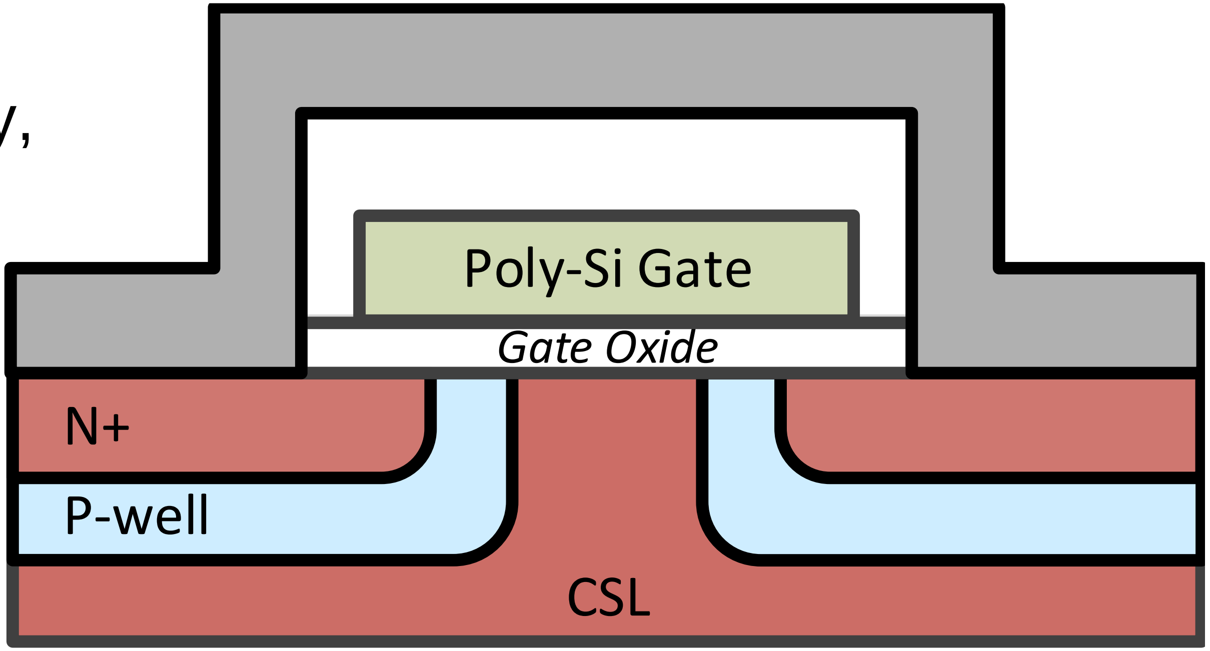
- Elimination of R_{JFET}.
- Reduction of R_{Ch}, due to higher channel mobility
- Big reduction in area, hence £/amp

$$R_{ON} = R_{Drift} + \cancel{R_{JFET}} + R_{Ch} + R_{Subs} + R_{Other}$$

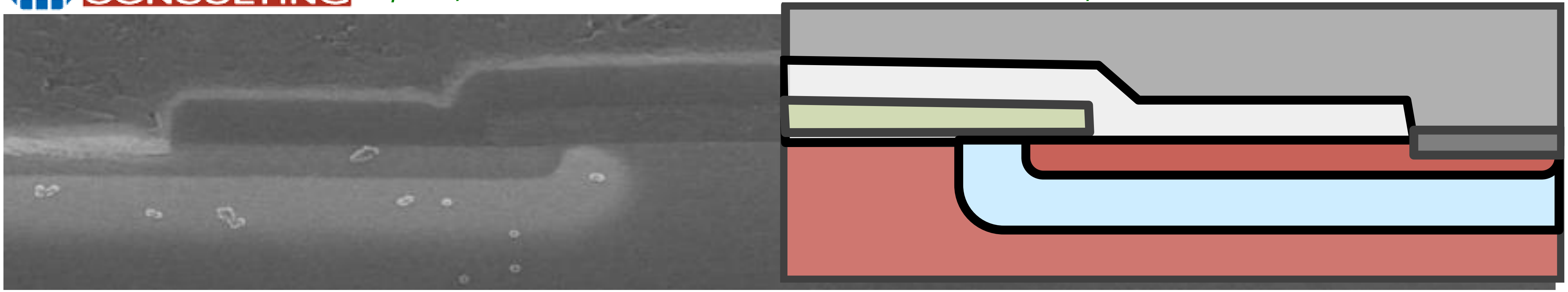


Commercial SiC Power MOSFET Designs

- Many planar devices are available today, including from STMicroelectronics, who supply Tesla among others.
- Below is a SEM cross section of the STC30N120, showing the regions previously discussed.



SYSTEMPlus CONSULTING *https://www.systemplus.fr/reverse-costing-reports/stmicroelectronics-1200v-sic-mosfet-stc30n120/*



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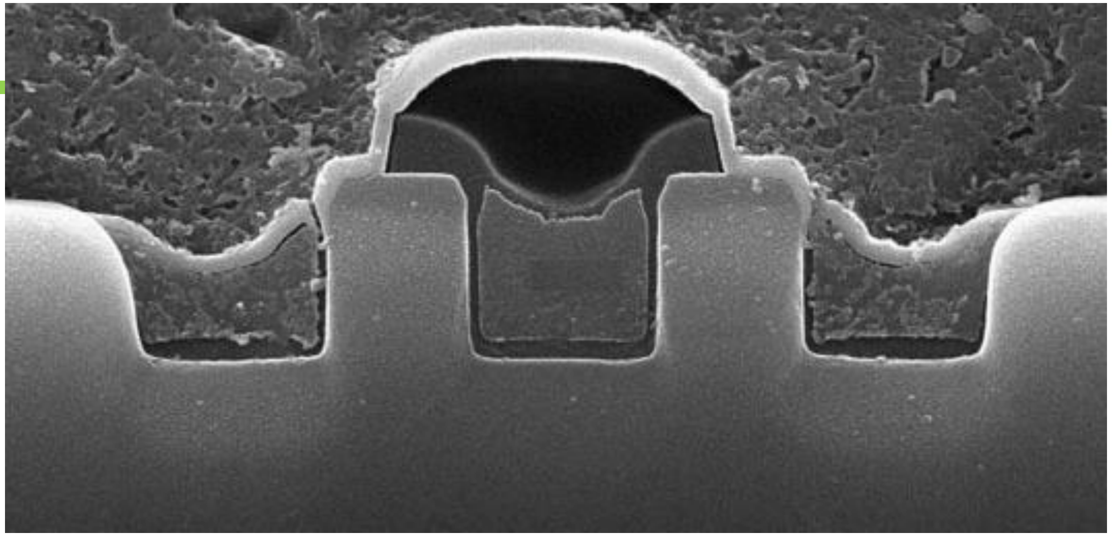
EPSRC Pioneering research and skills

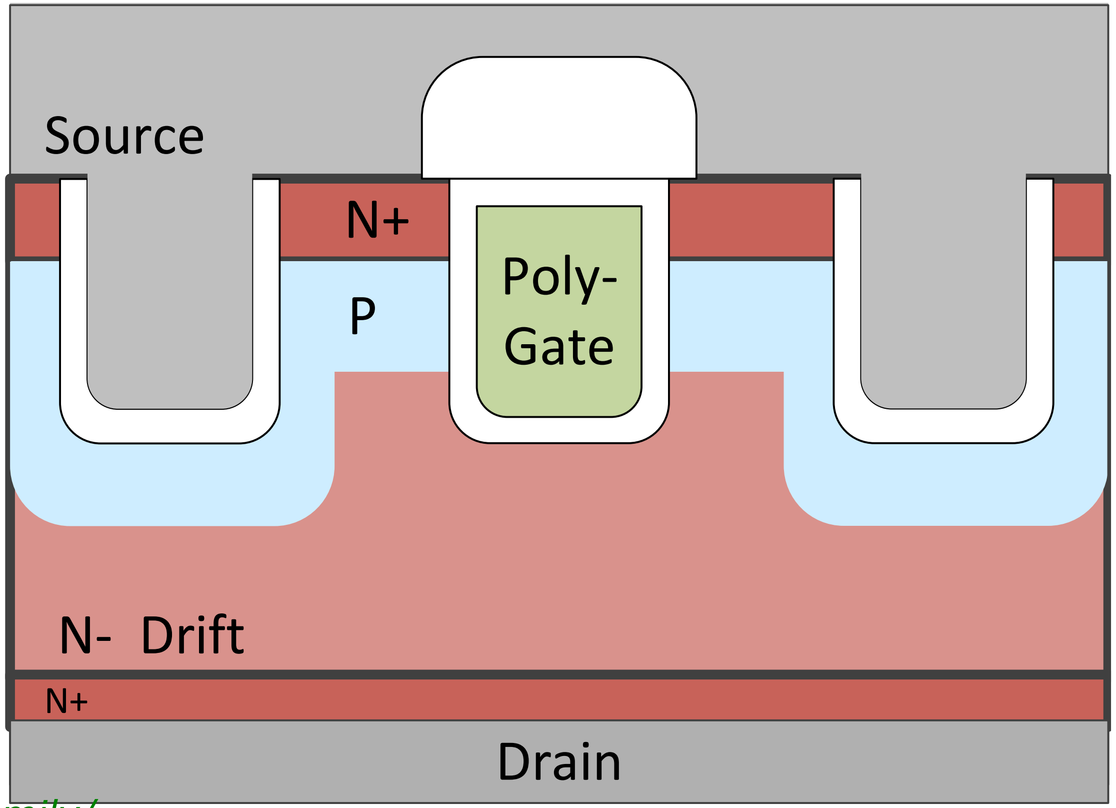
Commercial SiC Power MOSFET Designs

Rohm 3rd Gen. Double Trench MOSFET Design.

- Trench gate structure to maximise density, and remove JFET region. Conduction vertically down both sides of every other trench
- Conduction 50% less than Gen 2 planar design, C_{ISS} down by 35%.
- Dummy trench every other, to enhance short circuit ruggedness and to protect gate oxide.

https://www.systemplus.fr/reverse-costing-reports/rohm-sic-mosfet-gen3-trench-design-family/





Commercial SiC Power MOSFET Designs

Infineon CoolSiC Trench MOSFET Design.

- Trench gate structure to maximise density, and remove JFET region.
- Conduction vertically down one side of every trench.
- Deep P-regions on every trench to limit the field across the gate oxide and enhance short-circuit ruggedness.

https://www.systemplus.fr/reverse-costing-reports/1200v-coolsictm-mosfet-module-df11mr12w1m1_b11-from-infineon/