E3-238 : Analog VLSI Circuits

Dr. Navakanta Bhat

Associate Professor, ECE Department
Indian Institute of Science, Bangalore-560012

Email: navakant@ece.iisc.ernet.in
URL: http://ece.iisc.ernet.in/~navakant/Navakant_Bhat.html

August 2005

L-14	28-9-05	Output stage, Folded cascode, OTA, OPAMP circuits, Sample & hold

Output stage requirement

Capable of providing high output current to drive large loads

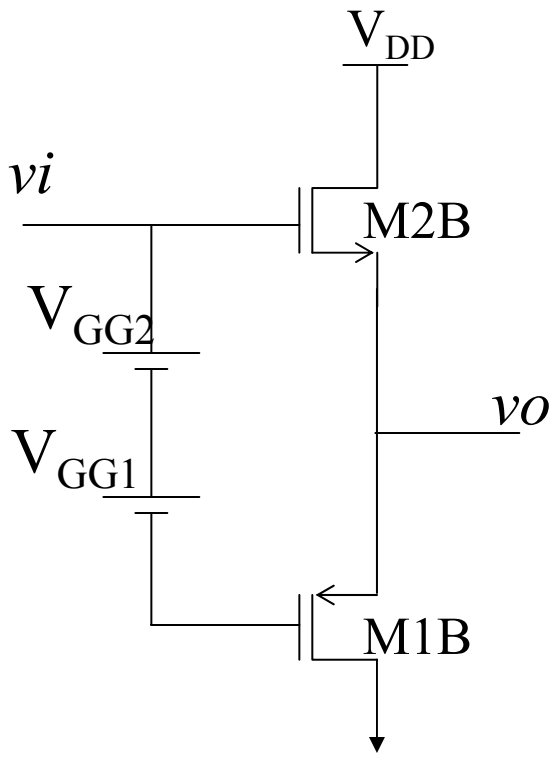
However, the DC bias current should be low to avoid Static power dissipation

The output impedance should be very low

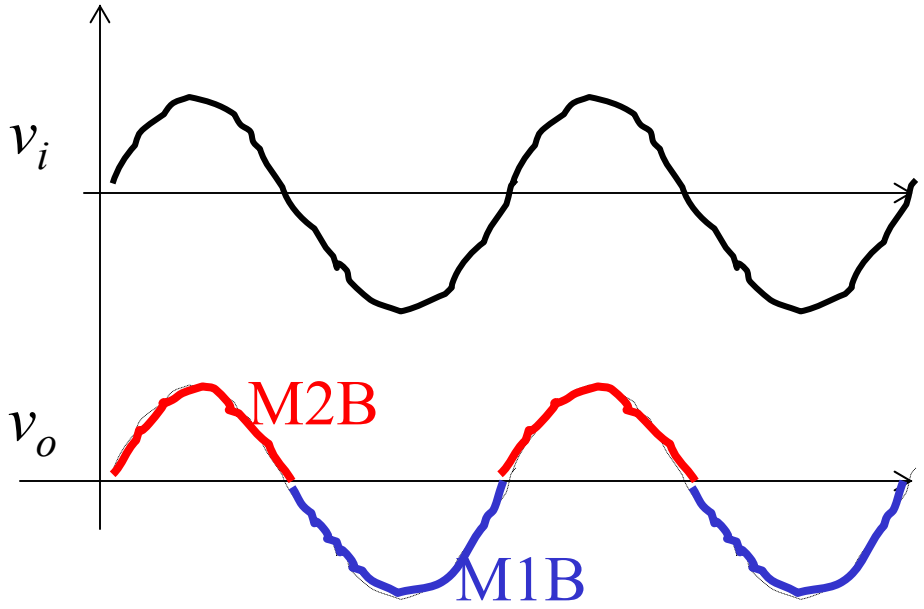
Source follower can serve the purpose

Class AB NMOS and PMOS source follower (push-pull) stage is a preferred configuration

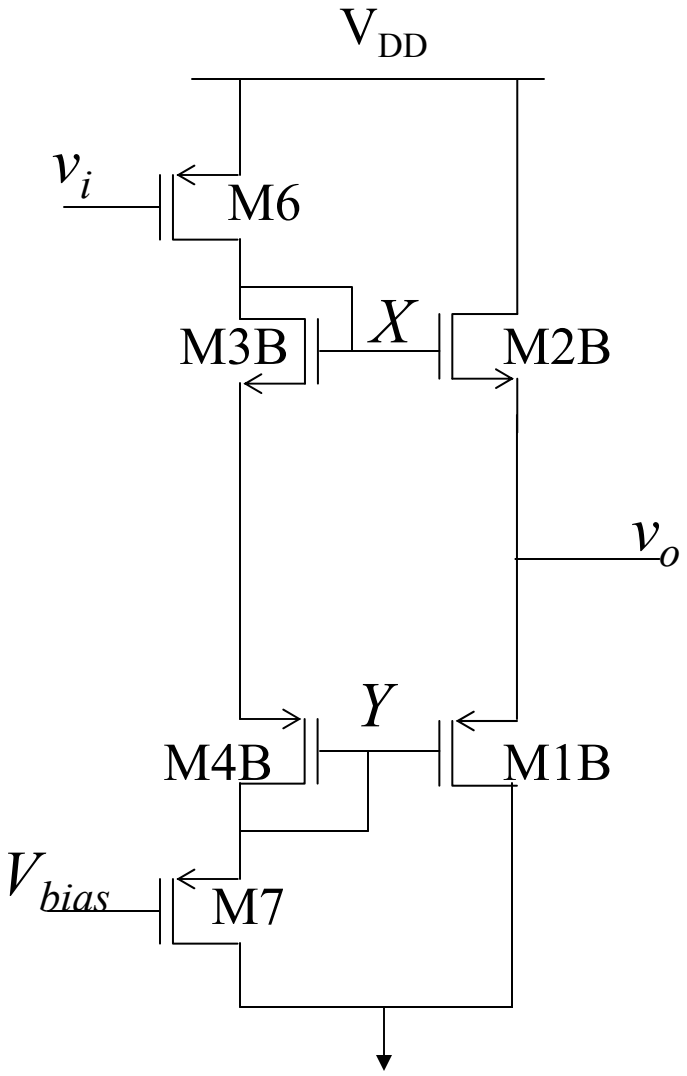
Output stage class AB



V_{GG1} and V_{GG2} are set such that M1B and M2B are biased just above *Vt* to avoid cross over distortion



Biasing the output stage



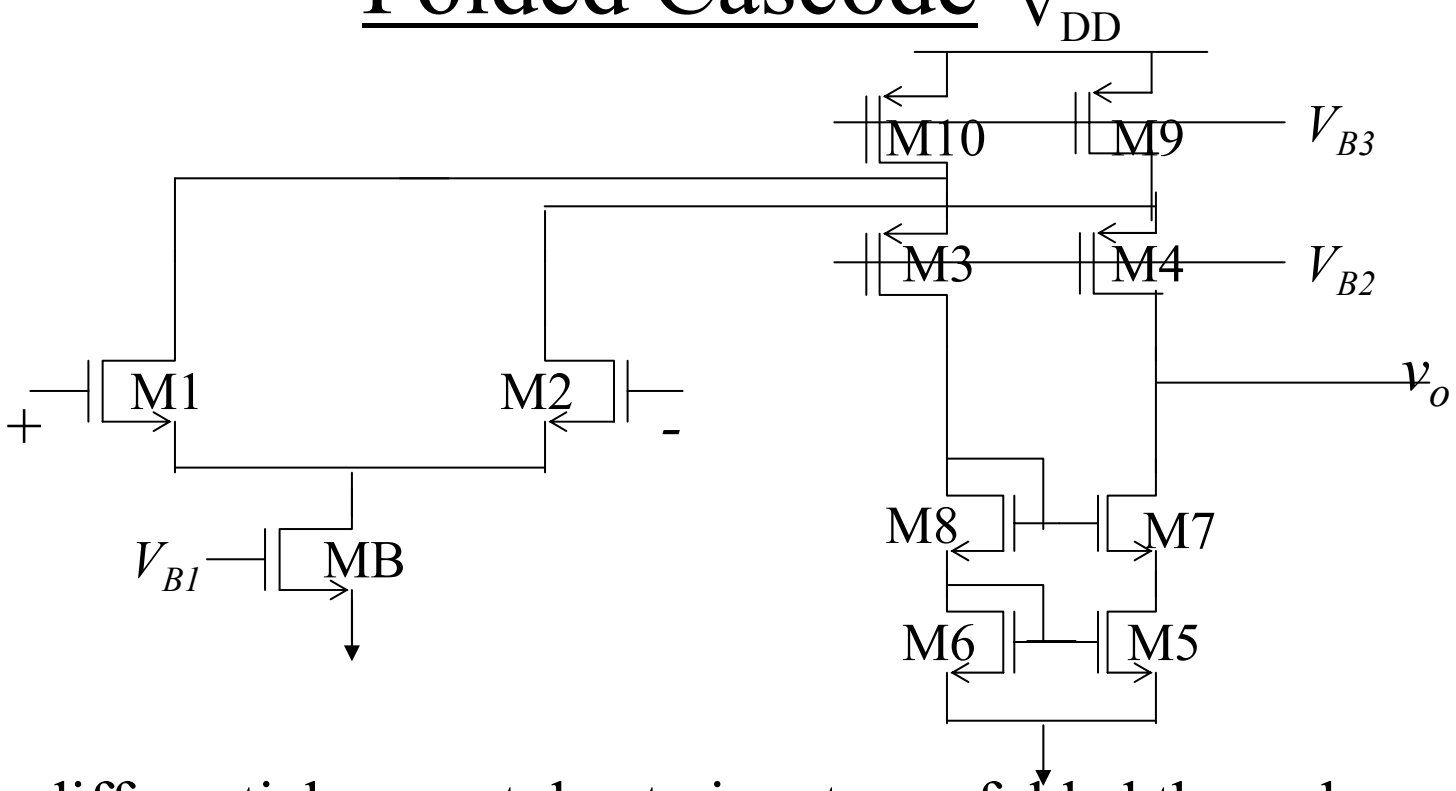
M3B and M4B are diode connected NMOS and PMOS respectivel

$$V_{xy} = V_{gs3b} + V_{gs4b}$$

$$V_{xy} = V_{tn3b} + V_{tp4b} + 2\Delta V$$

Choose the sizes of M3B and M4B such that *Vxy* is just above the the two $V_t s$ of M1B and M2B to avoid cross over distortion

Folded Cascode



The differential current due to inputs are folded through M1-M3 and M2-M4 pairs

The gain will be comparable to 2 stage OPAMP due to cascoding of the load transistor

The load capacitance itself acts as compensation capacitance

Folded cascode gain

$$A_v(0) = \frac{g_m}{\frac{g_{o2} + g_{o9}}{g_{m4} r_{o4}} + \frac{g_{o5}}{g_{m7} r_{o7}}}$$

$$A_v(0) = \frac{\left(g_m r_o\right)^2}{3}$$ Assuming all g_m and r_o are identical

The dominant pole is associated with the output

C_L provides frequency compensation

Increasing C_L improves phase margin

OTA and OPAMP Circuits

Operational Transconductance Amplifier

OTA is essentially an OPAMP without an output buffer

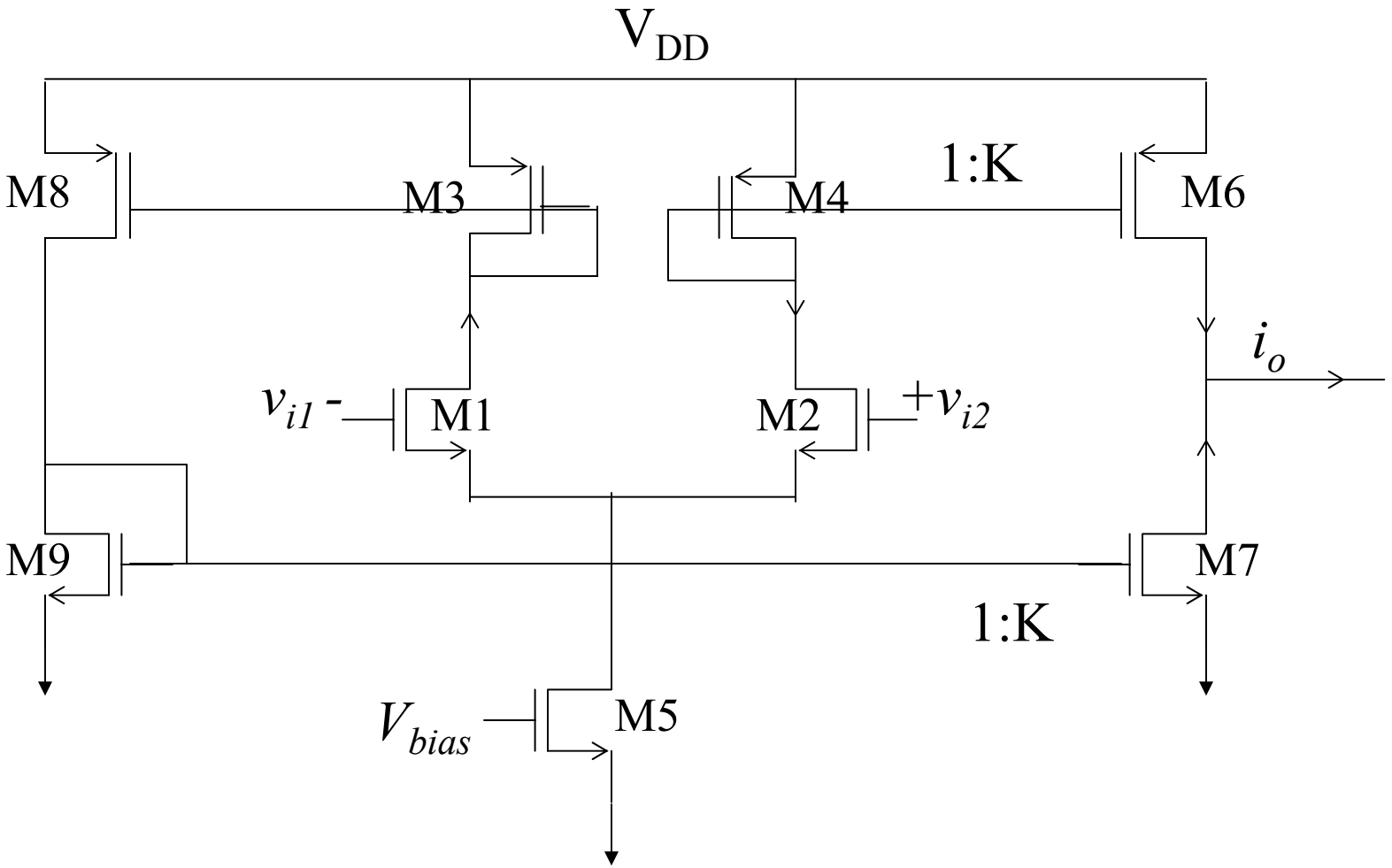
An OTA without output buffer can drive only capacitive loads

OTA is an amplifier where all nodes except I/O are low impedance nodes. Hence the two stage OPAMP configuration minus buffer is NOT an OTA since the drain of M4 is high impedance node

As the name suggests, the quantity of interest in OTA is not the voltage gain, but it is

$$Gm = \frac{i_{out}}{v_{i2} - v_{i1}} = \frac{i_{out}}{v_i}$$

The basic OTA circuit configuration



Gm expression

Assumptions

$g_{m1}=g_{m2}$ and $(W/L)_3=(W/L)_4=(W/L)_8$

$(W/L)_6=K(W/L)_4$ and $(W/L)_7=K(W/L)_9$

Then

$$i_o = i_{d6} - i_{d7} = K(i_{d4} - i_{d9}) = K(i_{d2} - i_{d1})$$

$$i_o = K\left(g_m \frac{v_i}{2} + g_m \frac{v_i}{2} \right) = K g_m v_i$$

$$G_m = \frac{i_o}{v_i} = K g_m$$

Transconductance Gm

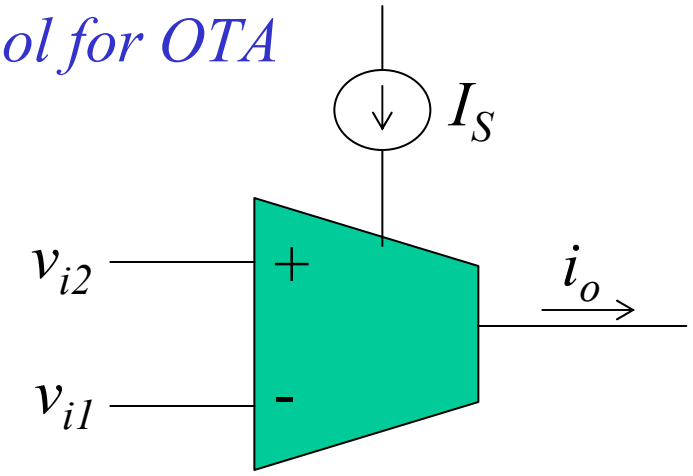
Gm can be set by appropriate K

For a given K (i.e. after design) Gm can still be varied by setting an appropriate bias current, I_S

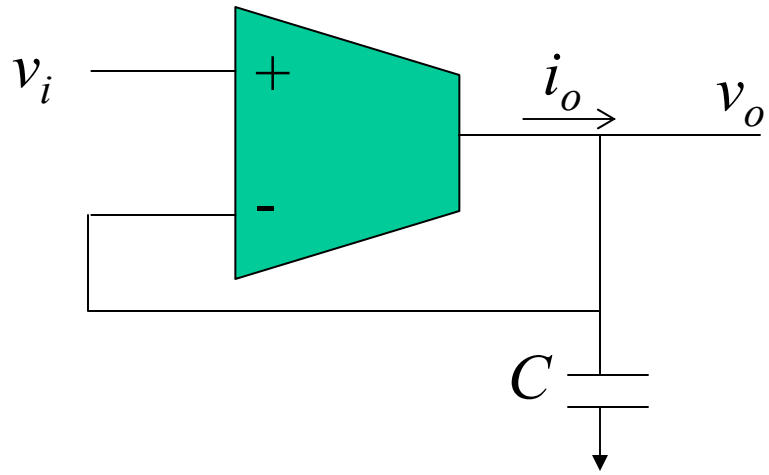
i.e. Filters made using OTA can be tuned by changing I_S

Output pole is the only dominant pole!
i.e. capacitive loads improve the phase margin

The symbol for OTA



Simple Low pass filter



$$v_o = i_o \frac{1}{j\omega C}$$

$$v_o = G_m(v_i - v_o)\frac{1}{j\omega C}$$

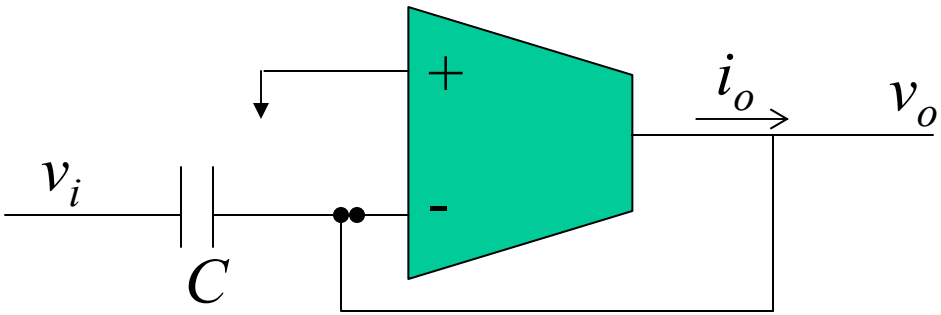
$$\frac{v_o}{v_i} = \frac{G_m / j\omega C}{1 + G_m / j\omega C}$$

$$\frac{v_o}{v_i} = \frac{1}{1 + j\omega\left(\frac{C}{G_m}\right)}$$

Single pole low pass filter with a cut off frequency of

$$\omega_p = G_m/C$$

Simple High pass filter



$$v_o - v_i = \frac{i_o}{j\omega C} = \frac{-G_m v_o}{j\omega C}$$

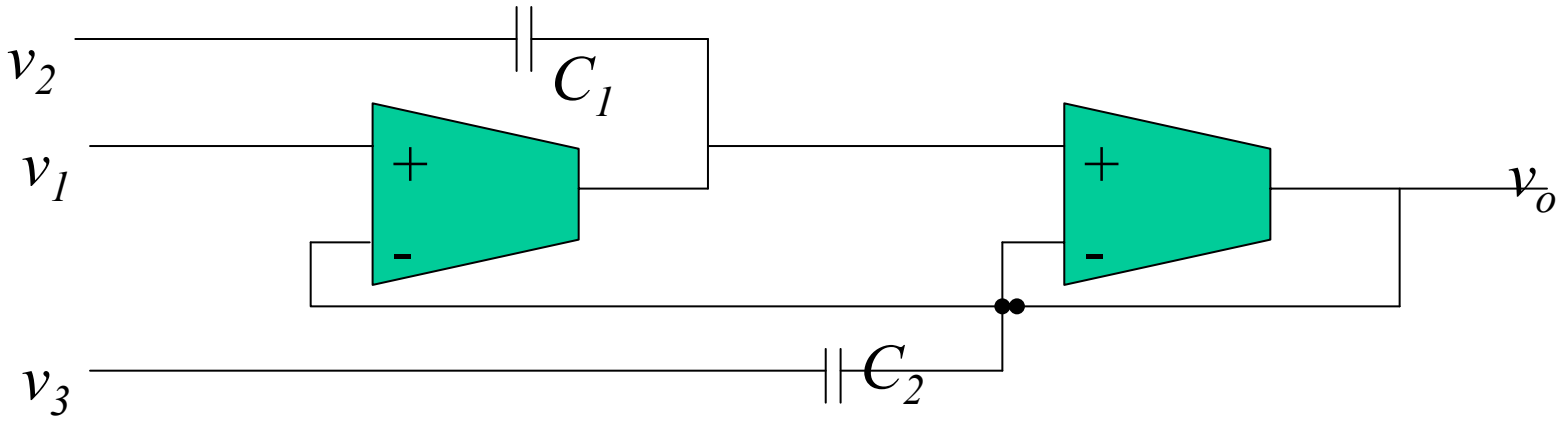
$$\frac{v_o}{v_i} = \frac{1}{1 + G_m / j\omega C}$$

$$\frac{v_o}{v_i} = \frac{j\omega\left(C/G_m\right)}{1 + j\omega\left(C/G_m\right)}$$

High pass filter with cut off frequency of

$$\omega_p = G_m/C$$

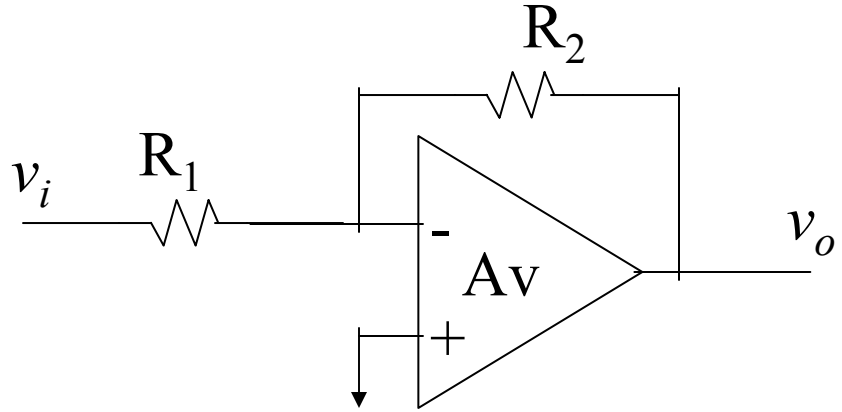
General biquadratic (biquad) configuration



Filter	Input Condition	Transfer function
Low-pass	$v_1 = v_i,\ v_2 = 0\ ,v_3 = 0$	$g_m^2 \Big/ s^2C_1C_2 + sC_1g_m + g_m^2$
High-pass	$v_1 = 0,\ v_2 = 0\ ,v_3 = v_i$	$s^2C_1C_2 \Big/ s^2C_1C_2 + sC_1g_m + g_m^2$
Band-pass	$v_1 = 0,\ v_2 = v_i, v_3 = 0$	$sC_1g_m \Big/ s^2C_1C_2 + sC_1g_m + g_m^2$
Band-reject	$v_1 = v_i,\ v_2 = 0\ ,v_3 = v_i$	$s^2C_1C_2 + g_m^2 \Big/ s^2C_1C_2 + sC_1g_m + g_m^2$

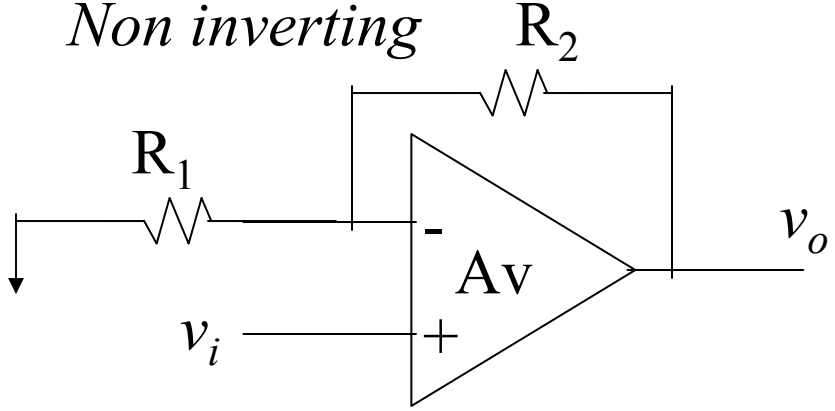
Inverting and Noninverting amplifier

Inverting



$$\frac{v_o}{v_i} = -\frac{R_2}{R_1}$$

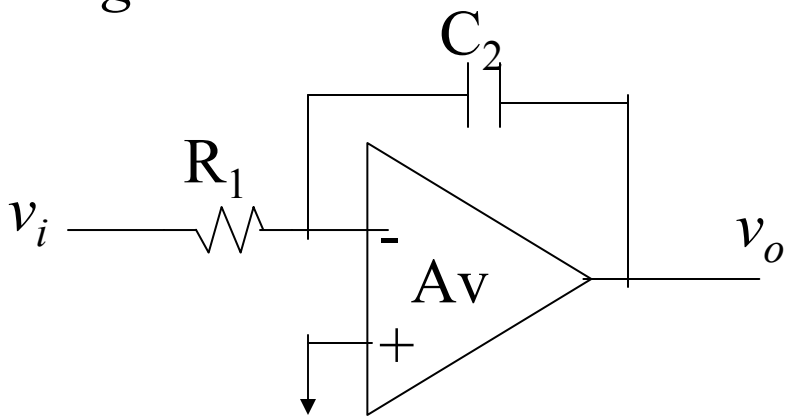
Non inverting



$$\frac{v_o}{v_i} = 1 + \frac{R_2}{R_1}$$

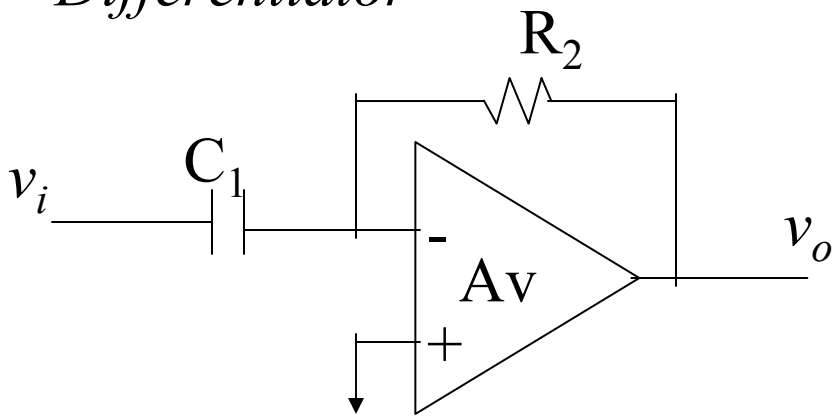
Integrator and Differentiator

Integrator



$$v_o = -\frac{1}{R_1 C_2}\int v_i dt$$

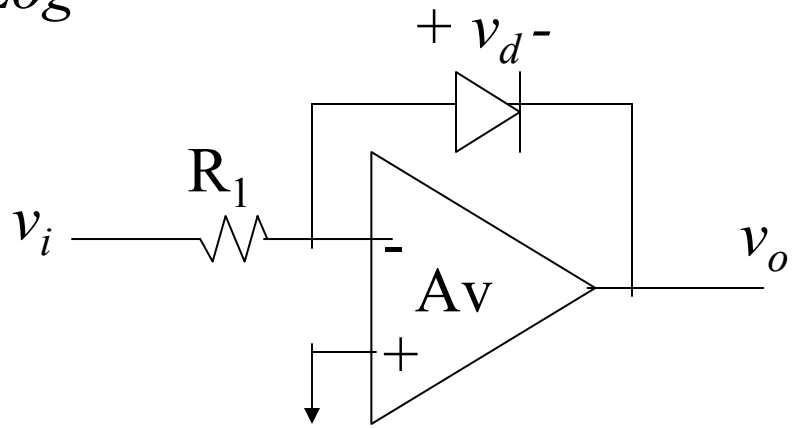
Differentiator



$$v_o = -R_2 C_1 \frac{dv_i}{dt}$$

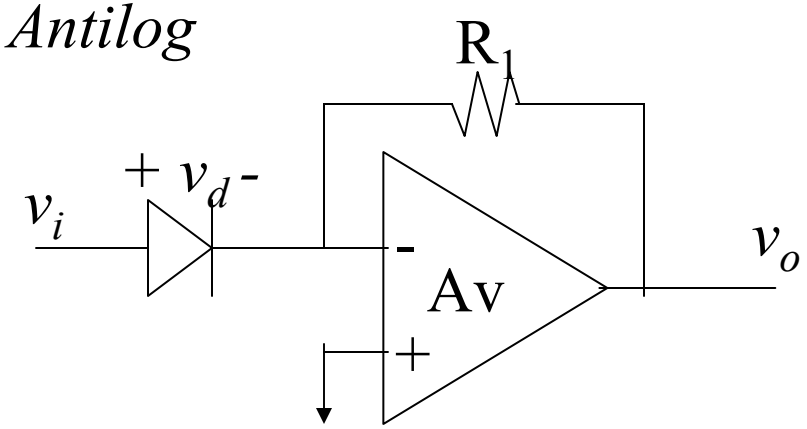
Log and Antilog Amplifier

Log



$$v_o = -V_T \ln \frac{v_i}{R_1 I_o}$$

Antilog



$$v_o = -I_o R_1 e^{\frac{v_i}{v_T}}$$

Sample and Hold Circuit

This is an essential requirement for discrete time systems (sampled data systems)

Applications:

ADCs,

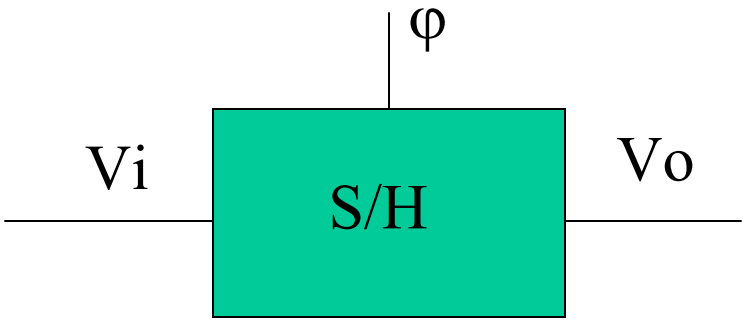
Switched capacitor filters

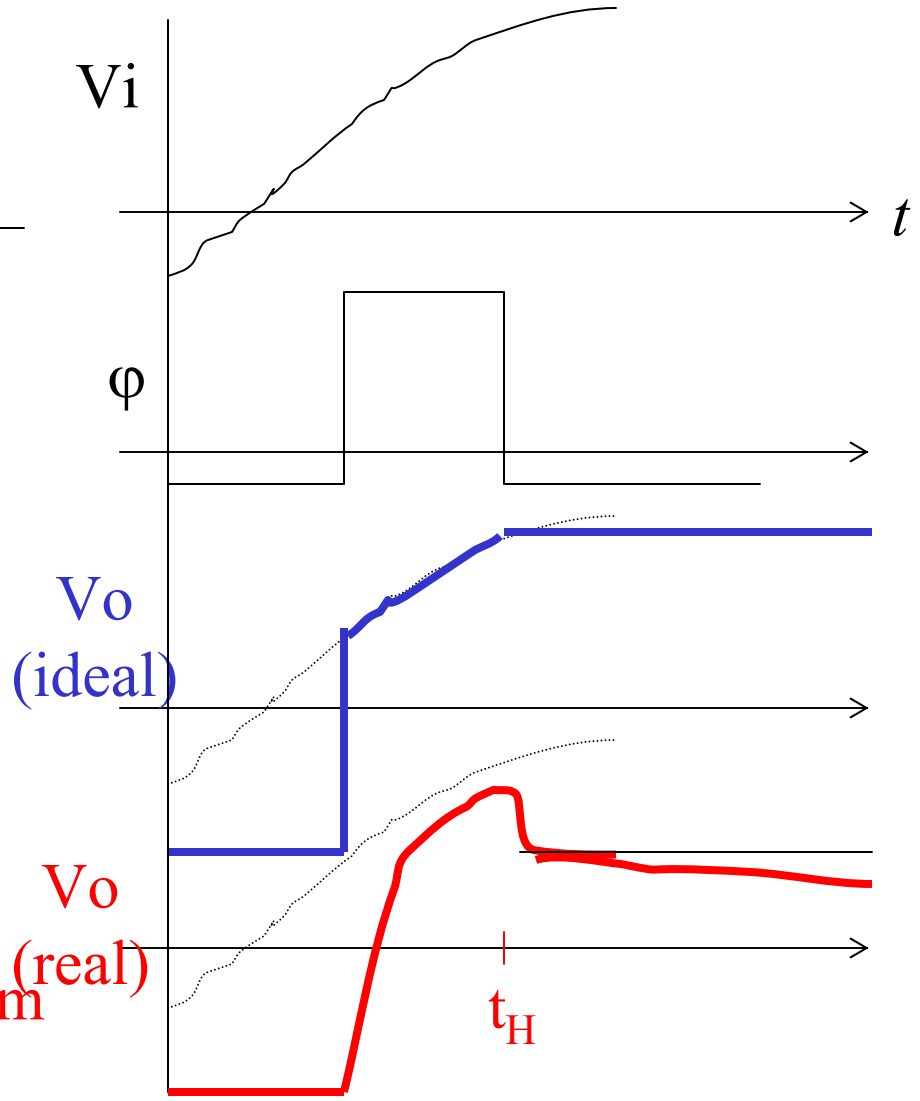
Comparators etc.

Requirement of discrete time operation:

1. Switches to perform sampling
2. High input impedance to sense the charge without corrupting (ideally suited for CMOS and not for BJT)

Requirements for S/H circuit





Advantages of MOSFET over BJT as a switch

1. ON but zero current
2. S/D voltages are not pinned to gate voltage
3. Conducts well in both the directions

But it is still does NOT perform Ideal Sampling function!

MOSFET switch issues

Finite acquisition time

Finite bandwidth in sample mode

DC offset in sample mode (Vos1)

Finite aperture delay (Δt)

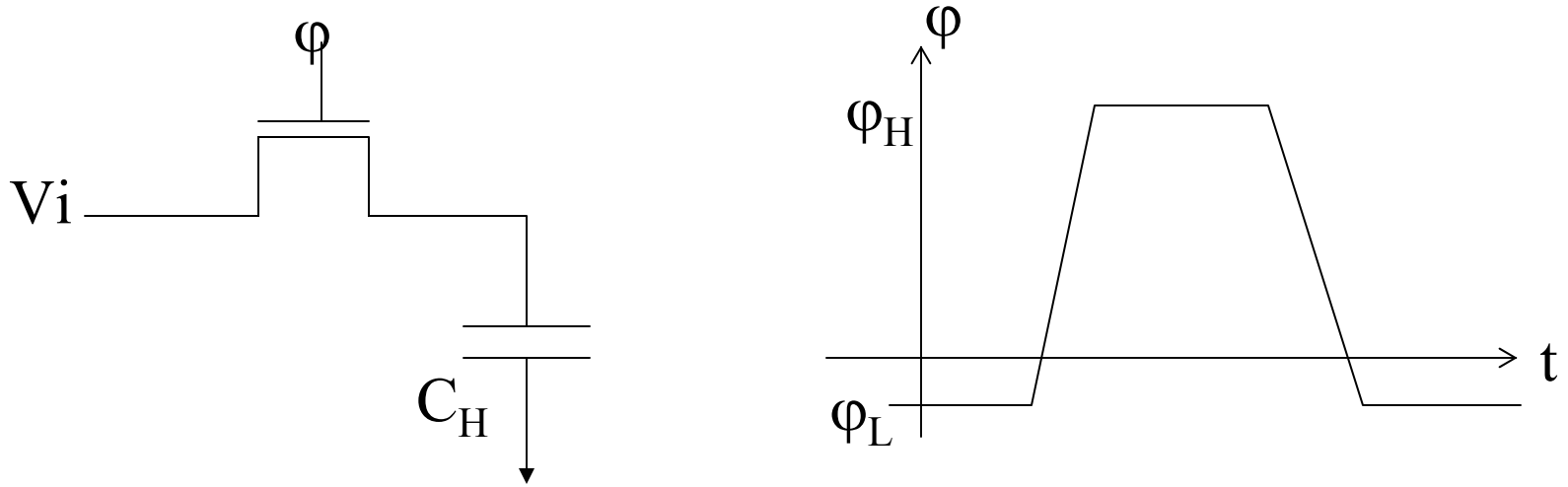
Pedestal error (Vos2) : (Charge injection and Clock feed through)

Droop in Hold mode

$$For\ t > t_H + \Delta T$$

$$V_o(t) = V_i(t_H + \Delta t) + V_{os1} + V_{os2} + \Delta V(t)$$

MOSFET sampling



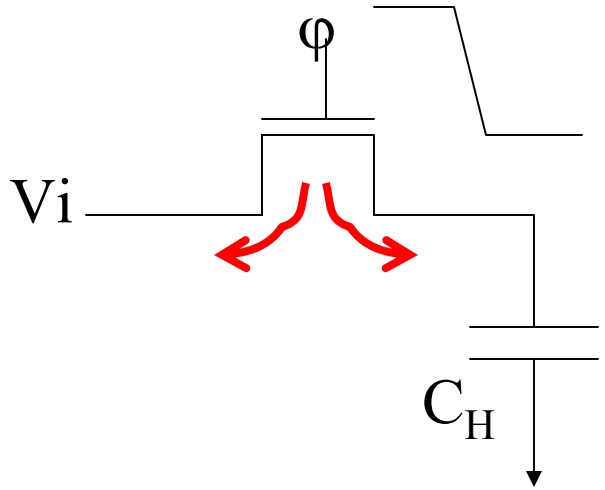
Acquisition time $\tau = R_{on}C_H$ (RC time constant of channel)

$$R_{on} = \frac{1}{\mu Cox \frac{W}{L}(V_{gs} - V_t)}$$ In linear region

Bandwidth in sample mode = 1/τ

$V_{os1}=0$ provided MOSFET is in linear region (i.e. $Vin < \varphi_H - Vt$)
Otherwise $Vo \neq Vin$ instead $Vo = \varphi_H - Vt$

Channel charge injection



When switch is ON, channel charge is

$$Qc=WLCox(\varphi_H\text{-}Vi\text{-}Vt)$$

When φ goes low, the switch turns off and the channel charge must exit out

An approximation is, 50% of this charge Goes to the out put node

The fraction that goes to output node is a complex function of parameters such as impedance seen at each node to the ground, clock transition time etc.
(ex: if clock makes slow transition all the charge could be absorbed at input)

$$\Delta V = -\frac{Q_c}{2C_H}$$

$$\Delta V = -\frac{WLC_{ox}(\phi_H - V_i - V_t)}{2C_H}$$

Effect of charge injection

$$V_o = V_i - \frac{WLC_{ox}(\phi_H - V_i - V_t)}{2C_H}$$

Vt is impacted by body effect

$$Vo = Vi\left(1 + \frac{WLC_{ox}}{2C_H}\right) + \gamma\frac{WLC_{ox}}{2C_H}\sqrt{2\varphi_b + V_i} - \frac{WLC_{ox}}{2C_H}\left(\phi_H - V_{t0} + \gamma\sqrt{2\phi_b}\right)$$

Gain error *Nonlinearity* *DC offset*

Speed-Precision product : $\tau\Delta V$

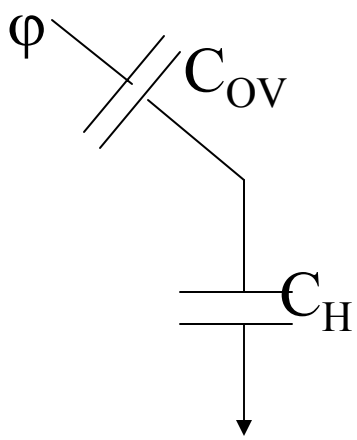
$$\tau \cdot \Delta V = \frac{L^2}{2\mu}$$

Interesting trade-off!

Depends only on L and is independent of transistor width and the value of the sampling capacitance

Clock feedthrough

When the switch is being turned off, the clock transition capacitively couples to the output



$$\Delta V = (\phi_H - \phi_L)\frac{C_{ov}}{C_{ov} + C_H}$$

$$C_{ov} = nC_{ox}WL_d$$

Note: If clock makes slow transition (quasi static)
Then the clock feed through error is significantly less

Example for error values

W=10μm, L=2μm, Vt=0.7V, Cox=1.38fF/μm^2,
C_{ov}=3fF, C_H=1pF, φ_H=5V, φ_H=0V

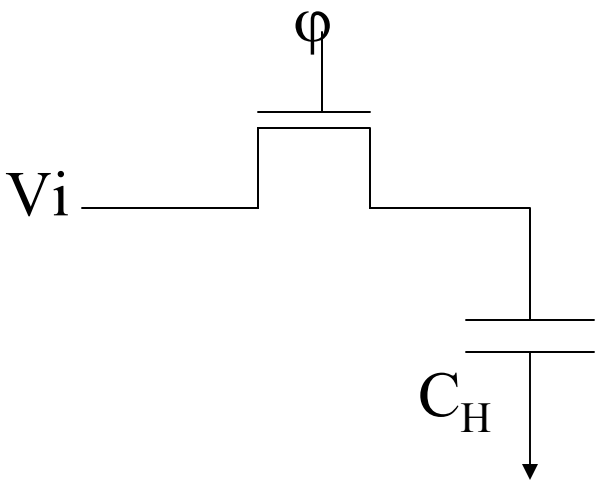
Gain error = 1.1%

Charge injection offset = 47mV

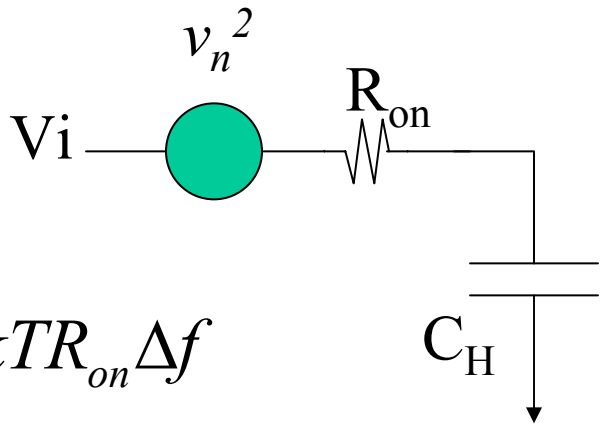
Clock feed through offset = 15mV

Total offset = 62mV

kT/C noise



Equivalent ckt in sample mode



$$\overline{v_n^{\,2}} = 4kTR_{on}\Delta f$$

$$H(f) = \frac{1}{1 + j2\pi f R_{on} C_H}$$

$$\overline{v_{oT}^{\,2}} = 4kTR_{on}\int_0^{\infty} \frac{1}{\left|1 + j2\pi f R_{on} C_H\right|^2} df$$

$$\overline{v_{oT}^{\,2}} = \frac{kT}{C_H}$$

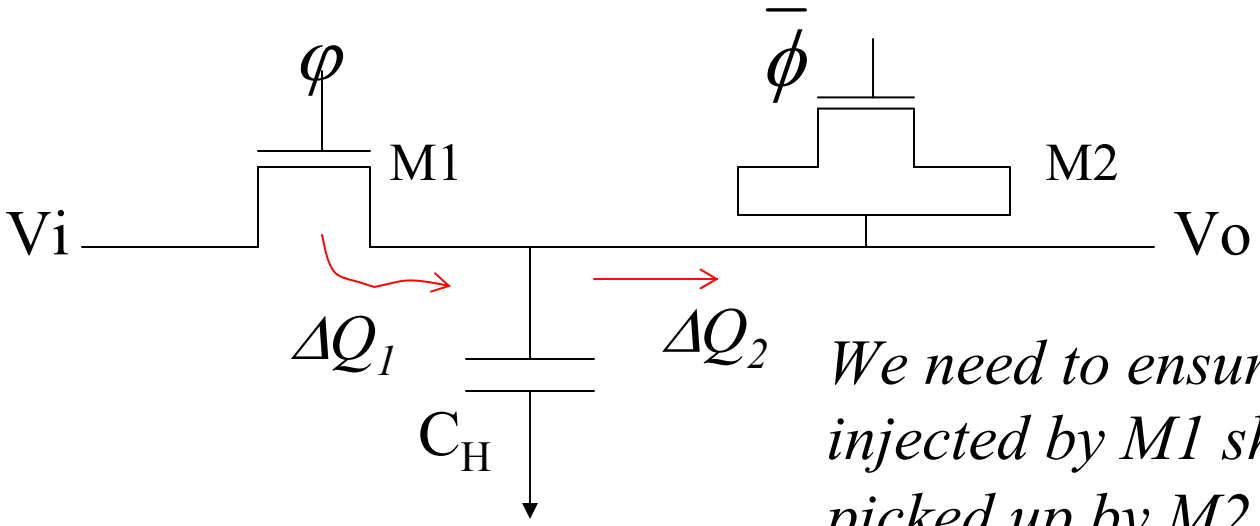
$$v_{oT}(rms) = \sqrt{\frac{kT}{C_H}}$$

For C_H=1pF, T=300oK,

$V_{oT}(rms) = 64.3\mu V$

The lowest limit!

Offset cancellation with dummy switch



We need to ensure that ΔQ_1 injected by M1 should be picked up by M2 (ΔQ_2)

$\Delta Q_1 = 0.5 W_1 L_1 C_{ox}(V_{DD}-Vi-Vt)$ $\Delta Q_2 = W_2 L_2 Cox(V_{DD}-Vi-Vt)$

Choose $L_1=L_2$ and $W_2= W_1/2$ to cancel the charge injection

Note that the clock feed through error is also cancelled

$$\Delta V_{cft} = -\Delta\phi \frac{C_{ov}}{C_{ov}+C_H} + \Delta\phi \frac{C_{ov}}{C_{ov}+C_H} = 0$$