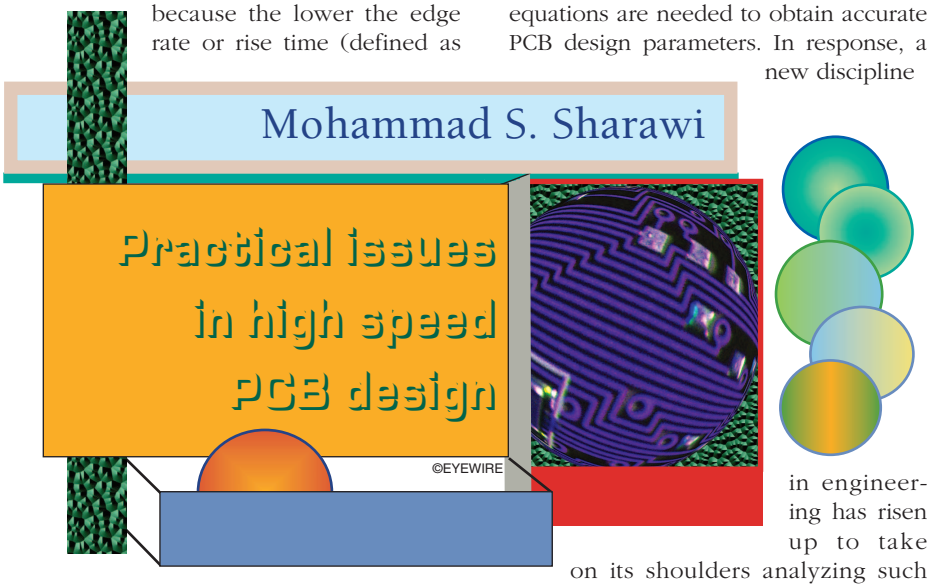
Signal integrity is a key component in high speed Printed Circuit Boards (PCBs) that work well. But obtaining it is getting trickier. For instance, with increasing higher bandwidth and faster data edge rate demands, designers must analyze interconnects and data communication busses as transmission lines; because the lower the edge rate or rise time (defined as the time it takes the signal to change from 10% to 90% of its final level), the higher the frequency content of the signal is (by Fourier analysis). At a high enough frequency, the wire parasitic (Resistance, Capacitance and Inductance) will delay and distort the signal as it travels from source to load chips. If such parameters are not handled or designed properly, the signal can fail partially or even totally.



To build a digital system, a card or a computer motherboard, we have to interconnect various types of Integrated Circuits (ICs) with various functions so they can communicate, exchange data and process it. Thus, after mounting the ICs on a PCB, they are connected via traces of copper (the most common conductor used). In the past, this process was not that critical because the frequencies of data transfers were not fast enough to cause trouble (i.e. the old-and-slow 8080 and 8086 processors). However, high frequency effects start to show up when the edge rate of the data (or the so-called rise time, see Fig. 1) is lower than the propagation delay of the PCB trace. Then, the signal traveling on the PCB is no longer a simple digital signal going through a lumped Resistor Capacitor (RC) network, because it begins to behave like a wave traveling along a transmission line. The electrical signal now has an E-field (Electric field) and an H-field (Magnetic field) component when traveling through a PCB trace; i.e., it operates like a Transverse ElectroMagnetic (TEM) wave. In this instance, the E and the H components of the signal are orthogonal to each other.

For such fast edge rates, Maxwell's equations are needed to obtain accurate PCB design parameters. In response, a new discipline in engineering has risen up to take on its shoulders analyzing such parameters of the PCB and signal behavior, it is Signal Integrity.

What is a transmission line?

The material is the medium, or structure, that forms all or part of a path for directing the transmission of energy, such as electric currents, magnetic fields, acoustic waves or electromagnetic waves from one place to another. The simplest structure is a two-wire line that connects both source ends to component/load ends to form a closed circuit. In low frequency circuits, such wires are modeled with a RC equivalent circuit, or sometimes simply with an equivalent resistance (resistance of the material).

As the frequency of operation increases, and the wavelength ($\lambda=c/f$, c is the speed of light, f is the frequency of operation) of the highest frequency component of the signal approaches the circuit's physical size, the transmission line must be handled as a distributed series of inductors, resistors and capacitors. The main parameters that define the behavior of a transmission line are its characteristic impedance, propagation delay and losses. We will talk and define such parameters and their impact on high-speed PCB analysis and design.

A PCB cross section

Current high-speed PCBs are multilayered, where one PCB may have more than 20 layers. Of course, more layers complicate the design and increase the cost of the board. However, it also allows more room for routing nets especially if the design contains a lot of busses and nets.

A typical PCB will have around six layers, of which two are Power/Ground planes and four are signal layers for routing. Such a board will have its layers either set up as Strip-lines or Microstrip lines (see Fig. 2). For a strip-line, the signal traces are sandwiched between the two plane layers (either Power or Ground, or both). The gap between them is filled with a dielectric material with a dielectric constant ε_r around 4.2 (a typical value for an FR4 material). Such a dielectric constant has an important role in the value of the propagation delay of the trace (acting like a transmission line) and its characteristic impedance. Usually, current high-speed designs have most of their signals routed in a strip-line fashion, since most of the E and the H fields are contained within the two plane layers, and are not radiated outside.

The other type of traces belongs to the Microstrip family (see Fig. 2b). Here, the signal trace is etched on a dielectric material over a plane (either Ground or Power planes). For this type of trace, some of the E and the H field lines get radiated outside (having the trace between air and dielectric lowers the effective er). This action affects the values of the characteristic impedance and propagation delay. As a result, routing the traces using the microstrip type (i.e. TOP and BOTTOM layers of a PCB) is usually avoided, because the

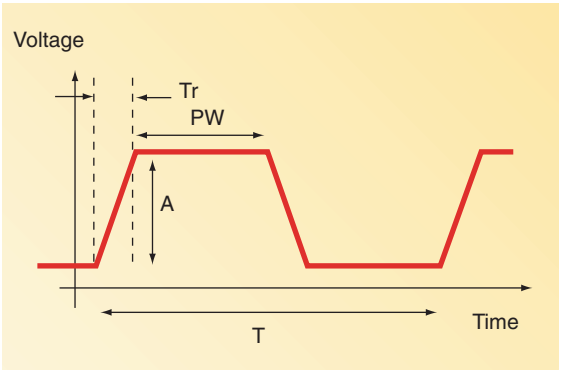


Fig. 1 Digital signal parameters (Tr is rise time, A is amplitude, T is period of signal.)

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signal speed on these layers will be faster than the internal ones. Extra care should be taken when routing on the outside layers.

Characteristic impedance

A PCB trace is described by its characteristic impedance. That is, the impedance that the incident wave sees when it enters the transmission line mode. Also, the propagation delay of the trace is the time it takes the wave to reach the end of the line from the time it was incident on it. The characteristic impedance of a lossless transmission line is given by:

$$Z_o = \sqrt{\frac{L}{C}} ohms \qquad (1)$$

where L is the inductance of the T-line, and C is the capacitance of the T-line with respect to the ground plane. The propagation delay is given by:

$$T_{PD} = \sqrt{LC} sec \qquad (2)$$

Usually, the characteristic impedance varies with the frequency of operation, and the T-line is usually a lossy one, so the formula for lossy Z_o is given by:

$$Z_o = \sqrt{\frac{R+j\omega L}{G+j\omega C}} ohms \qquad (3)$$

where R is the series resistance of the inductor, and G is the parallel conductance of the capacitor, and ω is the radial frequency (which is $\omega=2\pi f$). These parameters can be obtained from a field solver, or calculated using some formulas depending on the trace geometry. For a trace like the one shown in Fig. 2, the equations for Z_o and T_{PD} are given by:

stripline:

$$Z_o = \frac{60}{\sqrt{\varepsilon_r}} \ln\left(\frac{4(H+B)}{0.67\pi(T+0.8W)}\right)$$

for H = B, if H ≠ B then refer to

$$T_{PD} = \frac{\sqrt{\varepsilon_r}}{c} \qquad (4)$$

microstrip:

$$Z_o = \frac{87}{\sqrt{\varepsilon_r+1.41}} \ln\left(\frac{5.98H}{(T+0.8W)}\right)$$

$$T_{PD} = \frac{\sqrt{\varepsilon_e}}{c} \qquad (5)$$

where c is the speed of light, ε_r is the dielectric constant, and ε_e is the effective dielectric constant between air and the microstrip ε_r. These two equations are the ones used by the board designer as a rough and close estimate of the trace characteristics in his or her design.

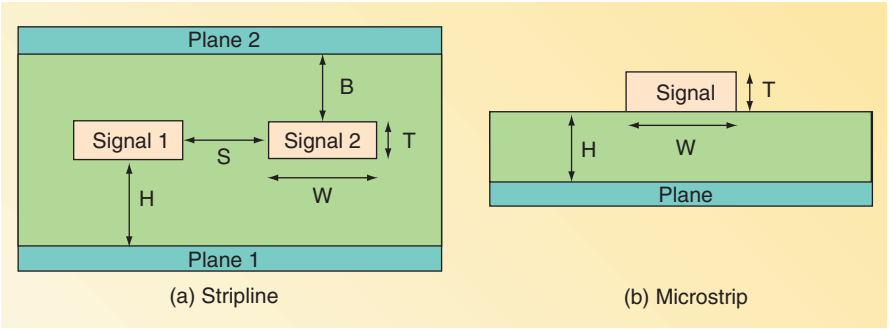

Fig. 2 PCB transmission line types

As mentioned earlier, no lossless traces exist. The loss in signal levels is due to resistive losses through the trace (transmission line). Losses can be divided into Direct Current (DC) losses and Alternating Current (AC) losses. Any conductor has a specific conductivity, which means it has a specific resistivity for the DC flow.

We all know the well-known resistance equation of a conductor that is given by:

$$R_{DC} = \frac{\rho L}{A} = \frac{\rho L}{WT} \qquad (6)$$

where ρ is the resistivity of copper and L is the trace length.(see Fig 2 for T,W). Such DC losses become significant for long lines, where buffers are needed to boost the signal levels. At high frequencies, the current tends to flow closer to the surface of conductors, instead of flowing uniformly throughout the conductor cross section. Such behavior is called the *Skin Effect*. The higher the frequency, the farther the current will be from the center of the conductor. This fact means a lower T that results in a higher resistance in the conductor to the current flow. This variable thickness is called the *Skin Depth*, and it is a function of frequency. It is given by:

$$\delta = \sqrt{\frac{\rho}{\pi f \mu}} \qquad (7)$$

where f is the frequency of operation, μ is the permeability of free space ($\mu = 4\pi\times10^{-7}$ henries/meters).

The AC resistance is usually taken from plots of T-line resistance with the frequency. An approximate formula is given by as (to be used only when the skin depth is less than the conductor thickness),

$$R_{AC} \approx \frac{\rho}{W\delta} = \frac{\sqrt{\rho\pi\mu f}}{W} \qquad (8)$$

The actual resistance of the line is a combination between the DC and AC parts, and can be approximately found by

$$R_{Total} = \sqrt{R_{DC}^2 + R_{AC}^2} \qquad (9)$$

This result is, of course, not taking the current density in the ground plane into account. (Usually, it's small and we can ignore it as a first order approximation.)

However, other effects like dielectric losses and variations in dielectric constant should be accounted for in a more complicated design. They might have a significant effect at higher frequencies. So a board designer must take some rough calculations, and know the frequencies of operation in worse case scenarios, to be able to analyze and characterize the design parameters to increase

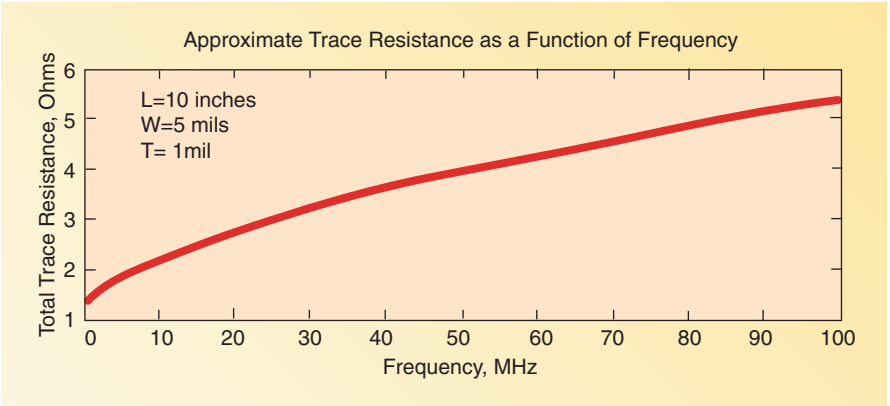

Fig. 3 Approximate trace resistance as a function of frequency

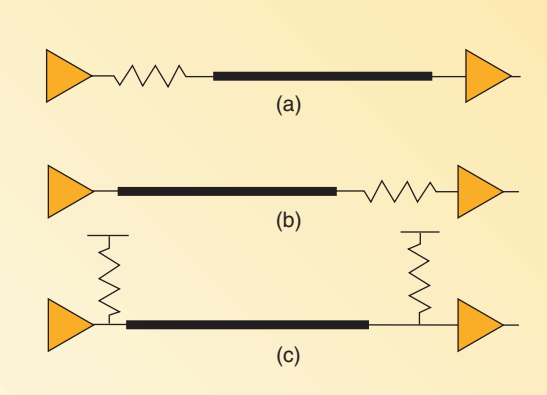

Fig. 4 Termination schemes

the percentage of a first run success.

Reflection and impedance matching

As the rise time of the digital signal gets smaller, the high frequency content of the signal increases. Then the signal should be treated as an incident wave on the transmission line. When a wave of light passes through a medium different than the original one, some of the signal actually passes through, but a portion gets reflected in the same medium. The same behavior occurs with EM waves, some of the incident wave's energy passes through the line but the remaining portion is reflected.

The amount of reflection actually depends on the characteristic impedance of the transmission line. If the characteristic impedance of the transmission line matches the source or load impedance, the wave incident is delivered totally without reflections. If there is a slight mismatch, part of the wave will pass, and the other part will be reflected towards the path it came from. The parameter that describes the amount of reflection is called the *Reflection Coefficient.* It is given by:

$$\Gamma = \frac{R - Z_0}{R + Z_0} \qquad (10)$$

where R is the source/load impedance, and Z_0 is the line characteristic impedance. Γ is calculated for both ends of the transmission line. A Γ value of 1 means that 100% signal reflection occurs. So no power will be delivered to the load. This happens when the value of R is much higher than Z_0, or when the T-line load is an open circuit.

When Γ is -1, the signal is reflected but in the opposite direction (i.e. 180 degrees phase shifted). This happens when the load is a short circuit. When the transmission line and the load/source impedances are matched, Γ will be Zero. Then the entire signal is transmitted with no reflection. All other values of Γ between 1 and -1 represent the percent of the wave reflected.

In board designs for high-speed applications, we make sure that we match the impedance of the trace (transmission line) to the external circuitry on both ends of the line. (In microwave circuit design, stub matching can be done with open circuit transmission line stubs, see Rao in *Read more about it* for details.) So when we qualify a certain Input/Output (I/O) driver or receiver circuit (i.e. a buffer), we check its output/input impedance values.

If they do not match the characteristic impedance of the trace, we either add external components to get the matching, or tweak our PCB geometry to match the impedances. Impedance matching is very important for maximum power transfer. Severe reflections will affect the signal quality and timing of the system, in which case the design could fail.

Termination topologies

Various termination techniques for impedance matching exist. They usually depend on the design topology used; the types of I/O cells used and the design specifications. Figure 4 shows some termination topologies. In Fig. 4a), a source termination topology is shown. Such a termination is used to match the source/driver output impedance to that of the transmission line. This termination scheme is used to reduce the amount of overshoot. It is used with Complementary Metal Oxide Semiconductors (CMOS) I/O cells, among others.

Load termination is shown in Fig. 4b). The trace is serially terminated before it connects to the load. Usually, a load series termination is used to reduce the amount of reflected wave coming back to the transmission line towards the source. Some high-speed digital standards require what is called parallel termination (Fig. 4c), which means there is a pull up resistor on both ends of the line. Such standards include the High-Speed Transceiver Logic (HSTL), the Stub Series Terminated Logic (SSTL), and the Gunning Transistor Logic (GTL, used in Intel Pentium processors). The values of the termination resistors depend on the topology and I/O cells used.

Coupling and crosstalk

Another issue in high-speed PCBs that is becoming more problematic as the switching speeds increase, and higher density PCBs are designed, is Crosstalk. It is well known from electromagnetic theory that adjacent Electric and Magnetic fields affect each other. The signals, or waves, incur a coupling behavior due to the interference of their propagating fields. This phenomenon is not different than what happens between traces on a PCB bus. When signals start behaving as incident waves on transmission lines, the coupling/interference between signals on adjacent lines can become significant and cause faulty signaling if not being designed properly.

There are two types of coupling between lines. Capacitive coupling that is due to the electric field, and inductive coupling that is due to the magnetic fields. Crosstalk is the resultant effect of both the capacitive and inductive coupling among a group of nets. Usually the coupling from the nearest neighbors is the most significant in a design, and creates the major interference effect.

In Fig. 5, we show three strip-line traces, where the middle trace is the one called the victim net, and the two on the sides are called the aggressor

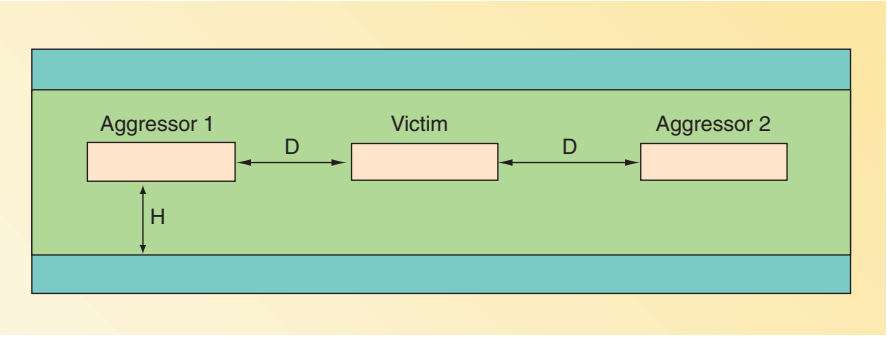

Fig. 5 Crosstalk

nets. When the aggressor nets start switching, they actually induce some voltage and current into the victim net due to the mutual inductance and capacitance, respectively.

There are various types of crosstalk noise depending on the switching patterns of the aggressor nets, actual board layout and the PCB bus structures. Usually, data busses suffer from crosstalk if they are not designed with care. This crosstalk lowers the noise margins for these signals and degrades the signal quality. Sometimes it leads to timing problems as well.

One rule of thumb is to increase the separation between the adjacent traces; a 4W (i.e. 4 times the width of the trace) trace separation is usually a good margin. But busses must be simulated to insure the proper operation with various topologies and trace geometry. Also, minimizing the height from the reference plane (H) will strongly couple the trace to its ground and minimize mutual coupling. An approximate formula for calculating the crosstalk percentage is given by,

$$\%Crosstalk = \frac{1}{1+\left(\frac{D}{H}\right)^2} \qquad (11)$$

Crosstalk contributions from various aggressors add to the total crosstalk on the victim net.

Vias and interconnect models

A via is a drill in the PCB that connects various layers together. Usually, when routing a trace, an obstacle stands in the way such as a chip, a component, or even another routed trace that we cannot cross in the same layer. Thus, we create a via to go to a different layer, and continue routing the trace until we reach the end point of the connection.

There are several types of vias. A very well known one is the ***Through Hole Via***. It goes all the way through the PCB, from the top layer to the bottom layer, connecting a net on the internal/external layers to another net on another internal/external layer.

A via is considered a discontinuity in the wave path, i.e. it has a different characteristic impedance and propagation delay. This difference affects the signal flow between the various layers. Based on the PCB geometry and trace lengths, separations, and thickness, Vias are designed/chosen to minimize reflections/attenuation based on the current design parameters. Figure 6 shows a ***Through Hole Via*** in a 3-layer PCB, and its circuit model.

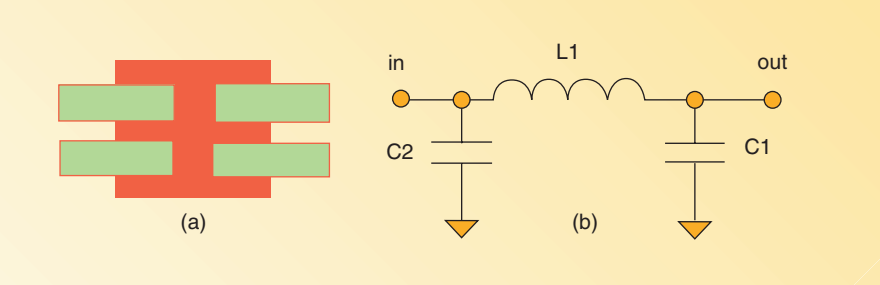

Fig. 6 A simple via model

Connector models also contribute to the integrity of the design. Thus, as the speed of the data increases, more accurate models for various interconnects are needed. Depending on the specific application and operating frequency, a model can be obtained from the vendor of the component/interconnect, or it can be simulated and approximated based on laboratory measurements and modeling techniques. Various connectors like Peripheral Component Interconnect (PCI) slots, Megarray connectors and Accelerated Graphics Ports (AGP) connectors fall into this category.

To have a more accurate modeling of Vias and connectors, it is usually best to use a 3D electromagnetic field solver (e.g. Maxwell from *Ansoft*) to get better approximations for such values. Most players in the high-speed design industry these days (Intel, SGI, IBM, etc.) use field solvers with transistor level design tools (i.e. HSPICE from *Avanti*). The goal is to get as accurate results and models as possible in their designs to ensure first run operation. This is accompanied with lab measurements under various test conditions to ensure the reliability of the model and design.

Conclusion

Current high-speed PCB designs need extra care due to the frequency of operation and reduced rise time signals. In this article, we presented the main issues and parameters that a PCB designer has to consider and analyze before a board layout is created. First order approximation equations for various parameters were presented based on the geometry of the PCB traces. Some useful design practices were also mentioned. As the speed of operation increases, the variables that were neglected at the lower frequency/higher rise time become more significant. Such parameters increase the complexity of the design. Three-dimensional analysis becomes a must to calculate and model interconnects accurately. This is where field solvers and the role of the Signal Integrity engineer come into play.

Read more about it

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About the author

Mohammad S. Sharawi was born in Wolfsburg, Germany in 1977. He obtained his B.S. degree (highest honors) in Electronics Engineering from ***Princess Sumaya University for Technology***, Amman-Jordan, and a M.S. degree in Electrical and Computer Engineering from ***Oakland University***, Michigan, in 2000 and 2002 respectively. He was a Hardware Design Engineer at ***Silicon Graphics Inc.*** (SGI), California, USA during 2002-2003. Currently, he is a faculty member at the Computer Engineering Department at ***Philadelphia University***, Amman-Jordan. His research interests are in high-speed PCB and interconnect design/modeling, circuit design and digital/wireless communications.