Pad Stack Design And Fine Hole Pitch Components, Part 1

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What happens when you try to route two traces between pins on 1mm pitch BGAs?

As noted in the previous article on pad stack design and fabrication, there are a number of factors that need to be taken into account when it's time calculate the complete dimensioning of the finished hole size on a plated through-hole in a PCB. When it comes to fine pitch components, there are always questions regarding what happens when 1mm and smaller pitch components are placed on high layer count PCBs and, specifically, why you shouldn't try to route two traces between the pins of these components.

This two-part article will describe the physical factors that have to be taken into account in terms of the final size of a plated through-hole, and what needs to be done in order to successfully mount 1mm and smaller pitch components on thick PCBs. Part 1 reviews the various aspects of the unplated holes in the pad stack while Part 2 will address how you go about routing the traces associated with these fine pitch components.

A Little Bit of History

The whole issue regarding the mounting of fine pitch components on a PCB holds its origins in the application notes coming from some component vendors. Specifically, these notes describe how it is possible to save layers in a PCB (fewer layers = lower cost) by routing two traces between pins on 1mm pitch BGAs. One of the leading FPGA vendors actually indicated that doing this would enable customers to use their very high pin count components in a low layer count PCB. Ultimately, what happens when this is done is that often, if not always, the resulting PCB will have very poor yields and unreliable operations when it is used in a final product running under actual conditions (as opposed to one operating in a laboratory or when it is a prototype that has been built in small volumes in a specialty shop).

What Needs to Happen

In order to better understand how the space in a multilayer PCB can be used to route traces in the signal layers, it's useful to re-examine how plated through-holes (vias) are created, and the various requirements that must be met for the final PCB to operate as specified. Figure 1 is a section through a plated through-hole showing the signal and plane layers.

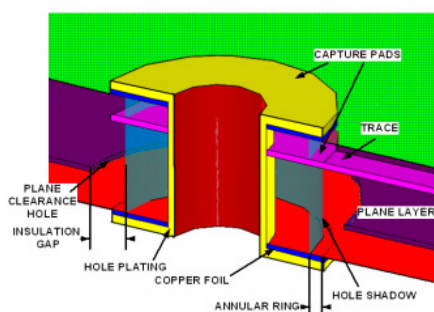

Figure 1. A Section Through a Plated through-hole in a PCB

As noted in part 1 of my article on pad stack design and fabrication, the dimensions of the features in Figure 1 are what are referred to when we use the term "pad stack design."

The elements within a pad stack design include:

- The finished hole.
- The size of the drilled hole.
- The size of the capture pad in a signal or surface layer used to connect to traces and component leads.

- The size of the clearance hole or antipad in the plane layers.
- The things that must be accounted for include:
- Minimum thickness of copper plating in the hole.
- Allowance for drill wander in the fabrication process.
- Allowance for misregistration between the layers of the PCB.
- The minimum insulation thickness between the plating in the hole and the metal in the signal and plane layers.
- Adequate copper bonding between the traces and the plating in the hole.

As will be illustrated, the dimensioning involved in designing pad stacks is done from the edges of then drilled, plated hole to the features inside the PCB or the drill size. Traditionally, the PCB design process was begun with the diameter of the finished, plated through-hole. And, the choice of drill size was left to the individual PCB fabricator. Furthermore, the size of clearance holes and capture pads in signal layers was made large enough that there was ample room for a wide range of drill sizes. As the pitch between device pins shrunk over the years, relying on this practice resulted in PCBs with poor manufacturing yields and unreliable operations.

To address this problem, it's become necessary that the PCB pad stack designer assume the lead on specifying the drill size as well as the finished hole size. In order to get from the finished hole size to the drill size, you only need to add 4 mils (.102 mm) to the finished hole size. Then the pad stack design process can proceed from the chosen drill size. It's important to note that once these dimensions have been determined and the drill size chosen, it must not be changed. If the drill size is made smaller than what was originally specified, the aspect ratio may become too large and the plating may not go all the way through the hole. If the drill size becomes too large, the clearances to copper in adjacent layers may be too small, or the drill may break out the side of the capture pad on a signal layer.

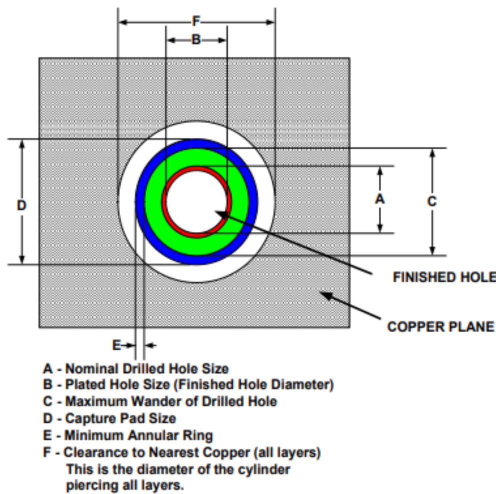

Figure 2. A Top-Down View of a Plated through-hole

Figure 2 is the top-down view of the plated through-hole or via. It shows the clearance hole or pad in a power plane of the F diameter. This is the minimum opening in the power planes needed to guarantee that there is enough room for the drilled hole, the drill wander, and the minimum insulation to nearest copper in any layer, be it signal or power. In Figure 3, an array of vias or holes spaced on a 1mm pitch is shown. The web between clearance pads is what is available for traces on signal layers, and for copper in the plane layers to conduct the current used by the ICs and other devices on the PCB. (It should be noted that if the trace width were the same as the web in the plane, the impedance of the trace would raise several ohms as it passes over the array of holes under a BGA. To minimize this effect, the web should be wider than the trace by about 2:1).

Calculating the Width of the Plane Webs and the Routing Channels in Signal Layers

The width of a plane web is the hole pitch minus the diameter of the clearance pad or hole. What needs to be determined is what the diameter of the clearance hole needs to be to satisfy the following constraints:

- Is the drilled hole large enough to insure proper plating?
- Is there enough room around the drilled hole to allow for drill wander?
- What is the minimum insulation thickness required?

Minimum Drilled Hole Size

Determining the minimum drill size needed to insure proper copper plating requires that you know the maximum aspect ratio of the drilled hole. This aspect ratio is defined as the ratio of hole length to diameter.

For now, the maximum aspect ratio for the top fabricators in the world is 10:1 for volume production. For the mid-tier fabricators it is 8:1, and for the low-end fabricators it is 6:1. The minimum drill size is also influenced by the thickness of the PCB. For example, if the PCB is 120 mils thick and is being built by a top-tier fabricator the minimum drill size would be 12 mils. For a mid-tier fabricator it would be 15 mils and for a low-end fabricator it would be 20 mils. (As will be seen from the following analysis, with component lead pitches of 1mm or more, a 12-mil drill works well. For this reason, this is the default smallest drill size we recommend even if the PCB thickness is less than 120 mils). Most of the high performance PCBs designed today are often 120 mils thick. This analysis will be for such a PCB built by a top-tier fabricator.

Allowance for Hole Wander

As noted in Part 1 of my article regarding pad stack design, drilled holes are often not exactly where they are designed to be. This is referred to as drill wander. Each fabricator has characterized its overall process and has arrived as its own drill tolerance which is what is used to define the hole shadow of each drilled hole. Based on various factors, the fabricator arrives at a measurement known as the TIR (total included radius) of the TID (total included diameter). And, as noted previously, the top tier fabricators can hold a TIR of 5 mils (TID 10 mils) across an 18"x24" panel. This is the most commonly used panel size for fabricating PCBs.

Based on the foregoing, there needs to be an allowance of 5 mils per side for drill wander. We refer to this as the hole shadow. The drilled hole casts this shadow all the way through the PCB. This shadow defines where copper, which is connected to the via or the trace, might be found. The distance from which the shadow in all the layers must be maintained is defined by the insulation requirement of the PCB.

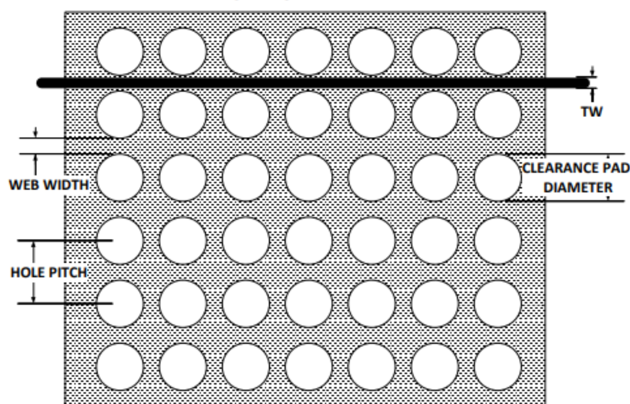

Figure 3. A View of a Plane With a Trace Traveling Over It

Minimum Insulation Requirement

Most laminate has a breakdown voltage on the order of 1000 volts per mil of thickness. Many systems require a minimum breakdown voltage, or hipot test, of at least 500 volts. Most Internet or Telco products require 2000 volts. Being conservative, it is good to design for the more difficult requirement or 2000 Volts. This would require a minimum of 2 mils of dielectric between opposing circuits or between traces or planes and the plating in the hole. This would require the clearance hole diameter to be 4 mils larger in diameter than the hole shadow.

The problem with the foregoing small dimension is that it does not account for the fact that the chemistry involved in etching, cleaning and plating will wick along the glass fibers in the weave of the laminate layers. Figure 4 is a section through a plated through-hole showing wicking along the glass fibers. To lend some scale to the photo, the copper layers are 0.5 mils thick. Some of the wicking is as much as six times this or 3 mils. This wicking is conductive. Therefore, it effectively increases the diameter of the plated through-hole by this amount per side or 6 mils total. Adding the 2 mils per side required for insulation and 3 mils per side for wicking, the total insulation thickness required to meet the insulation requirement is 5 mils per side.

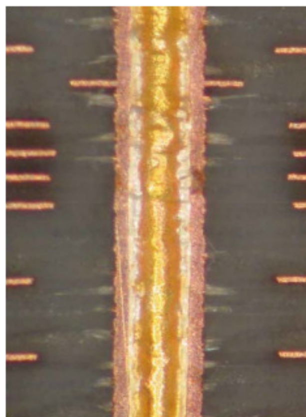

Figure 4. A Section Through A Plated through-hole Showing Wicking Along Glass Fibers

What Happens When You Have a 1mm Pitch BGA?

We can now use all the foregoing information to determine the plane web available for conducting current, and the space available for routing traces between the pins of a 1mm pitch BGA. For the 120- mil thick PCB, the minimum drill size is 12 mils. Referring to Figure 2, the diameter of the finished hole size would be 4 mils less than this, or 8 mils nominal. The hole shadow would be the 12-mil drill plus 10 mils for hole wander or 22 mils. The clearance hole in a plane would be 22 mils plus 10 mils for insulation allowance or 32 mils.

The hole-to-hole distance of a 1mm pitch BGA is 39.37 mils. Subtracting 32 mils from this results in a web width or trace routing channel width of 7.37 mils. This is ample room for a 5 or 6 mil trace. If one attempted to route two traces between holes (assuming they are 3 mil traces with a 4 mils space) the total width required would be 10 mils. Clearly, one of the requirements spelled out above would be violated and there would be yield problems with the resulting PCB.

Preventing Breakout of Capture Pads on Signal Layers

The connection between a trace and a plated through-hole is made by flashing a pad on the signal layer that is connected by its edge to the plating in the hole. This can be seen in Figure 4 on the second layer from the top. The size of this pad has a direct relationship to the overall reliability of the assembled PCB.

If the contact between the trace and the plating in the hole is just the cross section of the trace, aka a butt connection, this bond is not strong and is likely to be broken during soldering or rework. This results in a PCB that operates intermittently. The solution to this problem is to make the capture pads on the signal layers larger than the hole shadow by enough to guarantee no butt connections ever occur no matter where the drilled hole lands within the shadow. This allowance is referred to as an annular ring. Depending on the reliability level required of a product, the annular ring may be 1 mil, 2 mils or 0 mils.

Products that are intended for the consumer market have a lower reliability requirement than those destined for computers, military equipment or the Telco markets. In the latter case, the minimum annular ring for a capture pad in a signal layer is 1 mil. This means that these capture pads must be larger than the hole shadow by 2 mils. In the above analysis, the hole shadow was calculated to be 22 mils. This would require a capture pad 24-mils in diameter.

When the insulation requirement of 5 mils per side is added to this, the result is 34 mils. Subtracting this from the 39.37 mil pitch of the BGA, one arrives at a useful space for traces of only 5.37 mils. Clearly, there isn't even room for a 6 mil trace much less two traces.

Adding it All Up

As noted above, all of the features associated with a drilled hole are referred to as the pad stack. In the foregoing example, the pad stack is as follows:

- Drill size 12 mils
- Finished hole size 8 mils nominal
- Capture pad size 24 mils

- Annular ring 1 mil
- Clearance hole 32 mils
- Web with 1mm pitch 7.37 mils
- Maximum trade width 5.37 mils

In order to preserve routing space throughout the signal layers, the minimum pitch of routing vias or component holes for surface mount parts is 1mm. Any via or hole for connecting the lead of a surface mount part to an internal layer should use this pad stack.

All other plated through-holes should have their pad stacks designed as follows:

- Drill size = finished hole size + 4 mils
- Capture pad size = drilled hole size + 12 mils
- Clearance hole size = drilled hole size + 20 mils
- Minimum hole pitch = (d1 +d2) + 20mils + minimum web requirement (usually no less than 7 mils)

Conclusions

Based on the above, routing two traces between the pins of a 1mm pitch BGA will result in a low yielding and unreliable PCB. Once it is agreed that it is only possible to route one trace between pins, as long as the trace width is 5 mils or less, it is possible to specify a minimum drill size of 12 mils. There is no good reason to specify a smaller drill size as it would result in difficulties especially those that would potentially involve unreliable plating.

If a product developer is fortunate enough to have access to 50-mil pitch (1.27 mm) BGAs, the space available for traces is 50 mils, less 32 mils or 18 mils. This is plenty of room for two traces between pins and the space needed to separate them. Any time there is a choice between a 1mm pitch component and a 50- mil pitch component, the choice is clear.

Part 2 of this article will address the challenges associated with trying to route two traces between the pins of 0.8mm pitch components.

Would you like to find out more about how Altium can help you with your next PCB design? Talk to an expert at Altium or learn more about planning your multilayer PCB stackup in Altium Designer®.

References:

1. Ritchey, Lee W. and Zasio, John J., “Right The First Time, A Practical Handbook on High-Speed PCB and System Design, Volume 2.”
2. Ritchey, Lee W., “Why Not Route Two Traces Between Pins on a 1 mm Pitch BGA?” Current Source Newsletter, Issue 7, October 2007