Multilayer PCB Stackup Planning

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This Application Note details tried and proven techniques for planning high speed Multilayer PCB Stackup configurations.

Planning the multilayer PCB stackup configuration is one of the most important aspects in achieving the best possible performance of a product. A correctly stacked PCB substrate can effectively reduce electromagnetic emissions, crosstalk and improve the signal integrity of the product. An inferior stackup can increase emissions, crosstalk and also make the product more susceptible to outside noise. These issues can cause intermittent operation due to timing glitches and interference dramatically reducing the products performance and reliability.

Suppressing the noise at the source rather than trying to elevate the problems once the product has been built makes sense. Having the project completed 'Right First Time' on time and to budget means that you cut costs by reducing the design cycle, have a shorter time to market and an extended product life cycle.

Planes, in multilayer PCB's, provide significant reduction in radiated emission over two layer PCBs. As a rule of thumb, a four-layer board will produce 15 dB less radiation than a two-layer board.

Boards containing planes allow signals to be routed in either microstrip or stripline controlled impedance transmission line configurations creating much less radiation than the indiscriminate traces on a two layer board. The signals are tightly coupled to the planes (either ground or power) reducing crosstalk and improving signal integrity.

Ground and power planes in high speed digital systems perform three critical functions:

1. Provide stable reference voltages for exchanging digital signals
2. Distribute (low inductance) power to all logic devices
3. Controls crosstalk between signals

When selecting a multilayer stackup we should consider the following:

- A signal layer should always be adjacent to a plane.
- Signal layers should be tightly coupled (<10 MIL) to their adjacent planes
- A power plane (as well as a ground) can be used for the return path of the signal.
- Determine the return path of the signals (which plane will be used). Fast rise time signals take the path of least inductance which is normally the closest plane.
- Cost (the boss's most important design parameter).

Soldermask – Affects on Impedance

Since PCB's are normally covered in Soldermask then the affects of the conformal coating should be considered when calculating impedance. Generally, soldermask will reduce the impedance by 2 to 3 ohms on thin traces. As the trace thickness increases the soldermask has less affect.

ICD Stackup Planner – www.icd.com.au 21/9/2010

Layer		Material	Dielectric		Copper	Trace		Impedance	Edge Coupled	Broadside Coupled	
Number	Name	Type	Constant	Thickness	Thickness	Clearance	Width	Characteristic(Zo)	Differential(Zdiff)	Differential(Zdbs)	Description
1	Top	Conductive			0.7	4	4	57.95	100.43		Signal
		Dielectric	4.3	3							Prepreg
2	GND	Conductive			1.4						Plane
		Dielectric	4.3	5							Core

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Layer		Material	Dielectric		Copper	Trace		Impedance	Edge Coupled	Broadside Coupled	
Number	Name	Type	Constant	Thickness	Thickness	Clearance	Width	Characteristic(Zo)	Differential(Zdiff)	Differential(Zdbs)	Description
		Dielectric	3.3	0.5							Soldermask
1	Top	Conductive			0.7	4	4	55.93	96.93		Signal
		Dielectric	4.3	3							Prepreg
2	GND	Conductive			1.4						Plane
		Dielectric	4.3	5							Core

Figure 1 – Affects of Soldermask coating

Figure 1 illustrates the affect of soldermask coating on microstrip impedance. This example is of commonly used liquid photoimageable soldermask having a thickness of 0.5 MIL and a Dielectric Constant of 3.3.

The soldermask drops the microstrip characteristic impedance by 2 ohms and the differential impedance by 3.5 ohms. So, if you don't consider soldermask then the calculation could be out by as much as 3 to 4%.

Dielectric Materials

The most popular Dielectric material is FR4 and may be in the form of core or prepreg (pre-impregnated) material.

The core material is thin dielectric (cured fibreglass epoxy resin) with copper foil bonded to both sides. For instance: Isola's FR406 materials - include 5, 8, 9.5, 14, 18, 21, 28, 35, 39, 47, 59 and 93 MIL cores. The copper thickness is typically ½ to 2 oz (17 to 70 um).

The prepreg material is thin sheets of fibreglass impregnated with uncured epoxy resin which hardens when heated and pressed during the PCB fabrication process. Isola's FR406 materials – include 1.7, 2.3, 3.9 and 7.1 MIL prepregs that may be combined to achieve the desired prepreg thickness.

The most common stackup called the 'Foil Method' is to have prepreg with copper foils bonded to the outside on the outer most layers (top and bottom) then core alternating with prepreg throughout the substrate. An alternate stackup is called the 'Caped Method' which is the opposite of the Foil Method and was used by old-school military contractors.

Let's take a look at the most common multilayer configurations.

4 Layer Stackup

A typical four layer board stackup is shown below. The Characteristic and Differential Impedances of the substrate are calculated using the ICD Stackup Planner (available for download @ www.icd.com.au).

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Layer		Material	Dielectric		Copper	Trace		Impedance	Edge Coupled	Broadside Coupled	
Number	Name	Type	Constant	Thickness	Thickness	Clearance	Width	Characteristic(Zo)	Differential(Zdiff)	Differential(Zdbs)	Description
		Dielectric	3.3	0.5							Soldermask
1	Top	Conductive			0.7	12	8	52.21	99.41		Signal
		Dielectric	4.3	5							Prepreg
2	GND	Conductive			1.4						Plane
		Dielectric	4.3	47							Core
3	VCC	Conductive			1.4						Plane
		Dielectric	4.3	5							Prepreg
4	Bottom	Conductive			0.7	12	8	52.21	99.41		Signal
		Dielectric	3.3	0.5							Soldermask

Figure 2 - 4 Layer Stackup

To improve the EMC performance of a four-layer board it is best to space the signal layers as close to the planes as possible (< 5 MIL), and use a large core (~ 50 MIL) between the power and ground plane keeping the overall thickness of the substrate to ~ 62 MIL. This is the most cost effective way to improve the performance of a four layer PCB. This has three advantages:

1. The signal loop areas are smaller and therefore produce less differential mode radiation. For the case of 5 MIL spacing (trace layer to plane layer), this can amount to ~ 10 dB reduction in the trace loop radiation compared a stackup with equally spaced layers.
2. The tight coupling between the signal trace and the ground plane reduces the plane impedance (inductance) hence reducing the common-mode radiation from the cables connected to the board.
3. The close trace to plane coupling will also decrease the crosstalk between traces.

A good range of impedance (Zo) is from 50 to 60 ohms. Keep in mind that lower impedance will increase the dI/dt and dramatically increase the current drawn (not good for the PDN) and higher impedance will emit more EMI and also make the design more susceptible to outside interference.

6 Layer Stackup

Six layer boards typically consist of four signal routing layers and two planes. Basically, a four layer board with two extra signal layers added between the planes. From an EMC perspective a six-layer board is preferred over a four-layer board because it provides two buried layers for high-speed signals and two surface layers for routing low speed signals.

The signal layers should be placed very close to there adjacent planes and the desired board thickness (62 MIL) made up by the use of a thicker centre core. It is always a

compromise between trace impedance, trace width and prepreg/core thickness and it is best to use a stackup calculator to provide quick 'what if' analysis of the possibilities.

The ICD Stackup Planner calculates characteristic impedance plus edge coupled and broadside coupled differential impedance. The latter for embedded dual stripline layers only. Differential pairs are becoming common place in high speed design reducing noise by using differential mode signalling.

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Layer		Material	Dielectric		Copper	Trace		Impedance	Edge Coupled	Broadside Coupled	
Number	Name	Type	Constant	Thickness	Thickness	Clearance	Width	Characteristic(Zo)	Differential(Zdiff)	Differential(Zdbs)	Description
		Dielectric	3.3	0.5							Soldermask
1	Top	Conductive			0.7	8	12	54.82	89.48		Signal
		Dielectric	4.3	8							Prepreg
2	GND	Conductive			1.4						Plane
		Dielectric	4.3	14							Core
3	Inner 3	Conductive			0.7	8	12	52.64	84.43	76.95	Signal
		Dielectric	4.3	12							Prepreg
4	Inner 4	Conductive			0.7	8	12	52.64	84.43	76.95	Signal
		Dielectric	4.3	14							Core
5	VCC	Conductive			1.4						Plane
		Dielectric	4.3	8							Prepreg
6	Bottom	Conductive			0.7	8	12	54.82	89.48		Signal
		Dielectric	3.3	0.5							Soldermask

Figure 3 - 6 Layer Stackup

8 Layer Stackup

An eight layer board can be used to add two more routing layers or to improve EMC performance by adding two more planes. It is not recommended to have more then two adjacent signal layers between the planes as this creates impedance discontinuities (~20 ohms difference in impedance of signal layers) and increases crosstalk between these signal layers.

Although we see examples of both cases the majority of eight layer board stackups are used to improve EMC performance rather than add additional routing layers. If EMC is a concern and you need six routing layers then a ten layer board should be used.

In the case below, two plane layers are added to the centre of the substrate. This allows tight coupling between the centre planes and isolates each signal plane reducing coupling hence crosstalk dramatically. This configuration is commonly used for high speed signals of DDR2 and DDR3 designs where crosstalk due to tight routing is an issue. If you are risk aversive – then this is the stackup to use.

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Layer		Material	Dielectric		Copper	Trace		Impedance	Edge Coupled	Broadside Coupled	
Number	Name	Type	Constant	Thickness	Thickness	Clearance	Width	Characteristic(Zo)	Differential(Zdiff)	Differential(Zdbs)	Description
		Dielectric	3.3	0.5							Soldermask
1	Top	Conductive			0.7	5	5	50.05	90.4		Signal
		Dielectric	4.3	3							Prepreg
2	GND	Conductive			1.4						Plane
		Dielectric	4.3	6							Core
3	Inner 3	Conductive			0.7	5	5	48.25	85.81		Signal
		Dielectric	4.3	6							Prepreg
4	VDD	Conductive			1.4						Plane
		Dielectric	4.3	24							Core
5	GND	Conductive			1.4						Plane
		Dielectric	4.3	6							Prepreg
6	Inner 6	Conductive			0.7	5	5	48.25	85.81		Signal
		Dielectric	4.3	6							Core
7	VCC	Conductive			1.4						Plane
		Dielectric	4.3	3							Prepreg
8	Bottom	Conductive			0.7	5	5	50.05	90.4		Signal
		Dielectric	3.3	0.5							Soldermask

Figure 4 - 8 Layer Stackup

10 Layer Stackup

A ten layer board should be used when six routing layers are required and EMC is of concern. Ten layer boards, therefore, usually have six signal layers and four planes.

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Layer		Material	Dielectric		Copper	Trace		Impedance	Edge Coupled	Broadside Coupled	
Number	Name	Type	Constant	Thickness	Thickness	Clearance	Width	Characteristic(Zo)	Differential(Zdiff)	Differential(Zdbs)	Description
		Dielectric	3.3	0.5							Soldermask
1	Top	Conductive			1.4	7	4	53.53	101.58		Signal
		Dielectric	4.3	3							Prepreg
2	GND	Conductive			1.4						Plane
		Dielectric	4.3	5							Core
3	Inner 3	Conductive			1.4	7	4	50.69	90.13	74.2	Signal
		Dielectric	4.3	5							Prepreg
4	Inner 4	Conductive			1.4	7	4	50.69	90.13	74.2	Signal
		Dielectric	4.3	5							Core
5	VDD	Conductive			1.4						Plane
		Dielectric	4.3	12							Prepreg
6	GND	Conductive			1.4						Plane
		Dielectric	4.3	5							Core
7	Inner 7	Conductive			1.4	7	4	50.69	90.13	74.2	Signal
		Dielectric	4.3	5							Prepreg
8	Inner 8	Conductive			1.4	7	4	50.69	90.13	74.2	Signal
		Dielectric	4.3	5							Core
9	VCC	Conductive			1.4						Plane
		Dielectric	4.3	3							Prepreg
10	Bottom	Conductive			1.4	7	4	53.53	101.58		Signal
		Dielectric	3.3	0.5							Soldermask

Figure 5 - 10 Layer Stackup

A very common and nearly ideal stackup for a ten-layer board is shown above. The reason that this stackup has such good performance is the tight coupling of the signal and return planes, the shielding of the high speed signal layers, the existence of multiple ground planes, as well as a tightly coupled power/ground plane pair in the center of the board. High speed signals normally would be routed on the signal layers buried between planes (layers 3-4 and 7-8 in this case).

The way to pair signals layers in this configuration would be to pair layers 1 & 10 (carrying only low frequency signals), as well as pairing layers 3 & 4, and layers 7 & 8 (both carrying high speed signals). By paring signals in this manner, the planes on layers 2 and 9 provide shielding to the high frequency signal traces on the inner layers. In addition the signals on layers 3 & 4 are isolated from the signals on layers 7 & 8 by the center power/ground plane pair. For example, high speed clocks might be routed on

one of these pairs, and high speed address and data buses routed on the other pair. In this way the bus lines are protected, against being contaminated with clock noise (crosstalk), by the intervening planes.

12 Layer Stackup

Twelve layers is the largest number of layers that can usually be conveniently fabricated in a 62MIL thick board. Occasionally you will see 14 to 16 layer boards fabricated as a 62MIL thick board, but the numbers of fabricators capable of producing them are limited to those that can produce HDI boards.

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Layer		Material	Dielectric		Copper	Trace		Impedance	Edge Coupled	Broadside Coupled	
Number	Name	Type	Constant	Thickness	Thickness	Clearance	Width	Characteristic(Zo)	Differential(Zdiff)	Differential(Zdbs)	Description
		Dielectric	3.3	0.5							Soldermask
1	Top	Conductive			1.4	4	4	53.53	92.77		Signal
		Dielectric	4.3	3							Prepreg
2	GND	Conductive			1.4						Plane
		Dielectric	4.3	5							Core
3	Inner 3	Conductive			0.7	4	4	53.25	88.28	80.74	Signal
		Dielectric	4.3	5							Prepreg
4	Inner 4	Conductive			0.7	4	4	53.25	88.28	80.74	Signal
		Dielectric	4.3	5							Core
5	VDD	Conductive			1.4						Plane
		Dielectric	4.3	5							Prepreg
6	Inner 6	Conductive			0.7	4	4	53.25	88.28	80.74	Signal
		Dielectric	4.3	5							Core
7	Inner 7	Conductive			0.7	4	4	53.25	88.28	80.74	Signal
		Dielectric	4.3	5							Prepreg
8	GND	Conductive			1.4						Plane
		Dielectric	4.3	5							Core
9	Inner 9	Conductive			0.7	4	4	53.25	88.28	80.74	Signal
		Dielectric	4.3	5							Prepreg
10	Inner 10	Conductive			0.7	4	4	53.25	88.28	80.74	Signal
		Dielectric	4.3	5							Core
11	VCC	Conductive			1.4						Plane
		Dielectric	4.3	3							Prepreg
12	Bottom	Conductive			1.4	4	4	53.53	92.77		Signal
		Dielectric	3.3	0.5							Soldermask

Figure 6 - 12 Layer Stackup

High layer count boards (ten plus) require thin dielectrics (typically 5MIL or less on a 62MIL thick board) and therefore they automatically have tight coupling between layers. When properly stacked and routed they can meet all of our high speed requirements and will have excellent EMC performance and signal integrity. The above twelve layer stackup provides shielding on six of the internal layers.

14 Layer Stackup

The fourteen layer stackup below is used when eight routing (signal) layers are required plus special shield of critical nets is required. Layers 6 and 9 provide isolation for sensitive signals while layers 3 & 4 and 11 & 12 provide shielding for high speed signals.

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Layer		Material	Dielectric		Copper	Trace		Impedance	Edge Coupled	Broadside Coupled	
Number	Name	Type	Constant	Thickness	Thickness	Clearance	Width	Characteristic(Zo)	Differential(Zdiff)	Differential(Zdbs)	Description
		Dielectric	3.3	0.5							Soldermask
1	Top	Conductive			1.4	4	4	53.53	92.77		Signal
		Dielectric	4.3	3							Prepreg
2	GND	Conductive			1.4						Plane
		Dielectric	4.3	5							Core
3	Inner 3	Conductive			1.4	7	4	50.69	90.13	74.2	Signal
		Dielectric	4.3	5							Prepreg
4	Inner 4	Conductive			1.4	7	4	50.69	90.13	74.2	Signal
		Dielectric	4.3	5							Core
5	VDD	Conductive			1.4						Plane
		Dielectric	4.3	7							Prepreg
6	Inner 6	Conductive			1.4	4	4	52.87	88.46		Signal
		Dielectric	4.3	7							Core
7	VCC	Conductive			1.4						Plane
		Dielectric	4.3	5							Prepreg
8	GND	Conductive			1.4						Plane
		Dielectric	4.3	7							Core
9	Inner 9	Conductive			1.4	4	4	52.87	88.46		Signal
		Dielectric	4.3	7							Prepreg
10	VSS	Conductive			1.4						Plane
		Dielectric	4.3	5							Core
11	Inner 11	Conductive			1.4	7	4	50.69	90.13	74.2	Signal
		Dielectric	4.3	5							Prepreg
12	Inner 12	Conductive			1.4	7	4	50.69	90.13	74.2	Signal
		Dielectric	4.3	5							Core
13	VCC	Conductive			1.4						Plane
		Dielectric	4.3	3							Prepreg
14	Bottom	Conductive			1.4	4	4	53.53	92.77		Signal
		Dielectric	3.3	0.5							Soldermask

Figure 7 - 14 Layer Stackup

16 Layer Stackup

A sixteen layer PCB provides ten layers of routing and is normally used for extremely dense designs. Generally, you see 16 layer PCB's where the routing technology used in the EDA application doesn't have ability to route the design to completion. "If it won't route - just keep adding layers". Although this is a common saying it is not good practice.

If a board won't route to completion then there may be a number of reasons. Poor placement is often the course. Open routing channels, reduce the number of crossovers in the rats nets, place vias on a 25 MIL grid to allow through routing and basically help the router as much as possible.

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Layer		Material	Dielectric		Copper	Trace		Impedance	Edge Coupled	Broadside Coupled	
Number	Name	Type	Constant	Thickness	Thickness	Clearance	Width	Characteristic(Zo)	Differential(Zdiff)	Differential(Zdbs)	Description
		Dielectric	3.3	0.5							Soldermask
1	Top	Conductive			0.7	4	4	55.93	96.93		Signal
		Dielectric	4.3	3							Prepreg
2	GND	Conductive			1.4						Plane
		Dielectric	4.3	5							Core
3	Inner 3	Conductive			0.7	7	4	49.86	91.26	60.48	Signal
		Dielectric	4.3	3							Prepreg
4	Inner 4	Conductive			0.7	7	4	49.86	91.26	60.48	Signal
		Dielectric	4.3	5							Core
5	VDD	Conductive			1.4						Plane
		Dielectric	4.3	5							Prepreg
6	Inner 6	Conductive			0.7	7	4	49.86	91.26	60.48	Signal
		Dielectric	4.3	3							Core
7	Inner 7	Conductive			0.7	7	4	49.86	91.26	60.48	Signal
		Dielectric	4.3	5							Prepreg
8	VCC	Conductive			1.4						Plane
		Dielectric	4.3	5							Core
9	GND	Conductive			1.4						Plane
		Dielectric	4.3	5							Prepreg
10	Inner 10	Conductive			0.7	7	4	49.86	91.26	60.48	Signal
		Dielectric	4.3	3							Core
11	Inner 11	Conductive			0.7	7	4	49.86	91.26	60.48	Signal
		Dielectric	4.3	5							Prepreg
12	VSS	Conductive			1.4						Plane
		Dielectric	4.3	5							Core
13	Inner 13	Conductive			0.7	7	4	49.86	91.26	60.48	Signal
		Dielectric	4.3	3							Prepreg
14	Inner 14	Conductive			0.7	7	4	49.86	91.26	60.48	Signal
		Dielectric	4.3	5							Core
15	VCC	Conductive			1.4						Plane
		Dielectric	4.3	3							Prepreg
16	Bottom	Conductive			0.7	4	4	55.93	96.93		Signal
		Dielectric	3.3	0.5							Soldermask

Figure 8 - 16 Layer Stackup

There is really no limit to the number of layers that can be fabricated in a multilayer PCB (please check the capabilities of your fabricator first though). Of course, the board thickness increases as the layer count goes up to accommodate the minimum thickness of materials used. Also the aspect ratio (board thickness to smallest hole diameter) has to be considered. Generally this is 10:1 for boards thicker then 100MIL. For example, a 200 MIL thick substrate has a minimum hole size of 20 MIL.

How do you calculate the characteristic and differential impedance of the entire stackup using the established design rules?

Well this one I have made easy for you. In-Circuit Design Pty Ltd has developed a Stackup Planner. This new release builds on the familiar ease of use of the popular In-Circuit Design online Impedance Calculator that has been utilized by tens of thousands of Engineers and PCB Designers world wide since 1996. You can download an evaluation copy from www.icd.com.au

For those who are new to multilayer PCB stackup planning, standard 2 to 16 layer stackups have been provided that are commonly used. However, you can edit, rename and save a favourite custom stackup to use again.

The generic stackups use default values for all variables that can be adjusted to achieve the desired Characteristic (Zo), Edge Coupled (Zdiff) and Broadside Coupled (Zdbs) Impedance. The Dielectric Constant (also called Relative Permittivity), Dielectric Thickness, Copper Thickness, Trace Width and Trace can be varied.

For further information, please contact Barry Olney | +61 4123 14441 | b.olney@icd.com.au

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