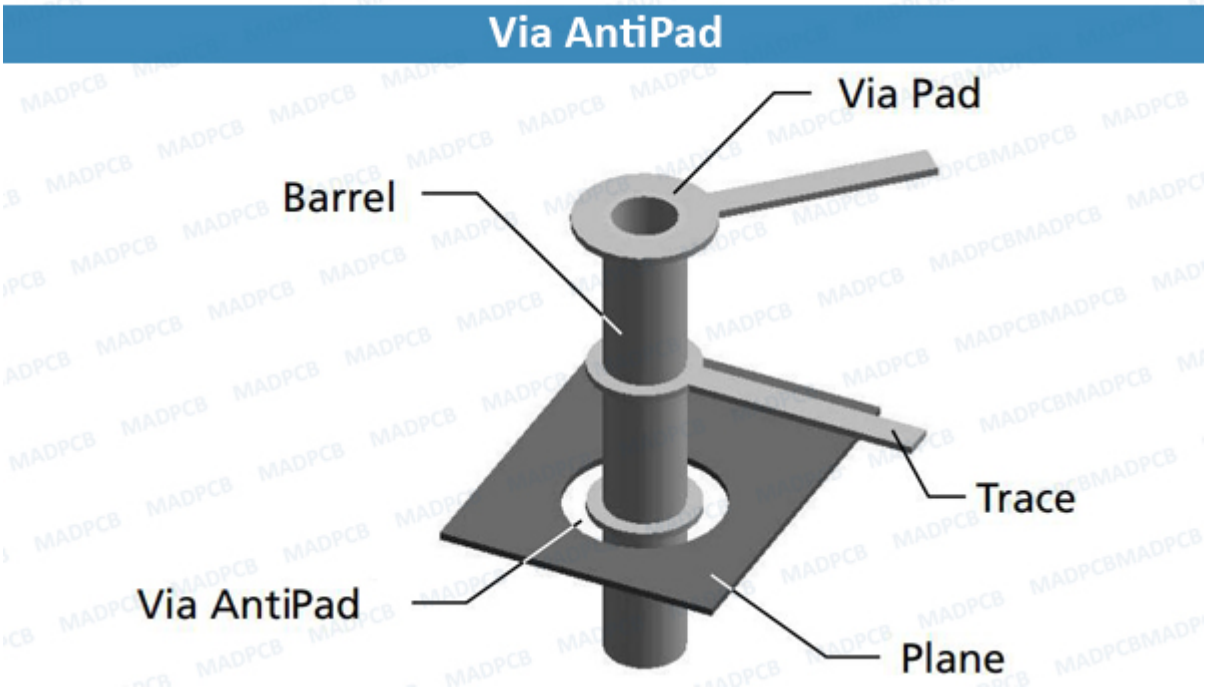
Antipad, Anti Pad or Anti-pad: PCB Design & Manufacturing | MADPCB

What's an Antipad in PCB?

An **Antipad**, **Anti Pad** or **Anti-pad** in printed circuit board (PCB) refers to the void area around a via on internal plane layer, and which restricts other signal traces that should not be connected to that particular plated through-hole (PTH).



Via Antipad

Antipads on vias and landing pads are a point of contention in modern PCB design, and he debate around the use of these elements in a multilayer PCB is framed as a binary choice. Like thermal reliefs, ground plane splits, and orthogonal routing, the debate around antipads on landing pads and vias is framed as an always/never choice. With today's modern PCBs, it pays to understand the effects of antipads on signal integrity (SI).

How to Model a Via and Its Antipads?

A via antipad is applied automatically by your design software based on the clearance rules anytime you use a plated-through hole (PTH) to transition through a solid plane. If you're routing through a plane layer, your options are to completely remove a large section of the plane around the via or encircle the via in the remaining conductor to create an antipad. No matter what happens, there must be some void between the via wall and any planes in order to prevent shorting.

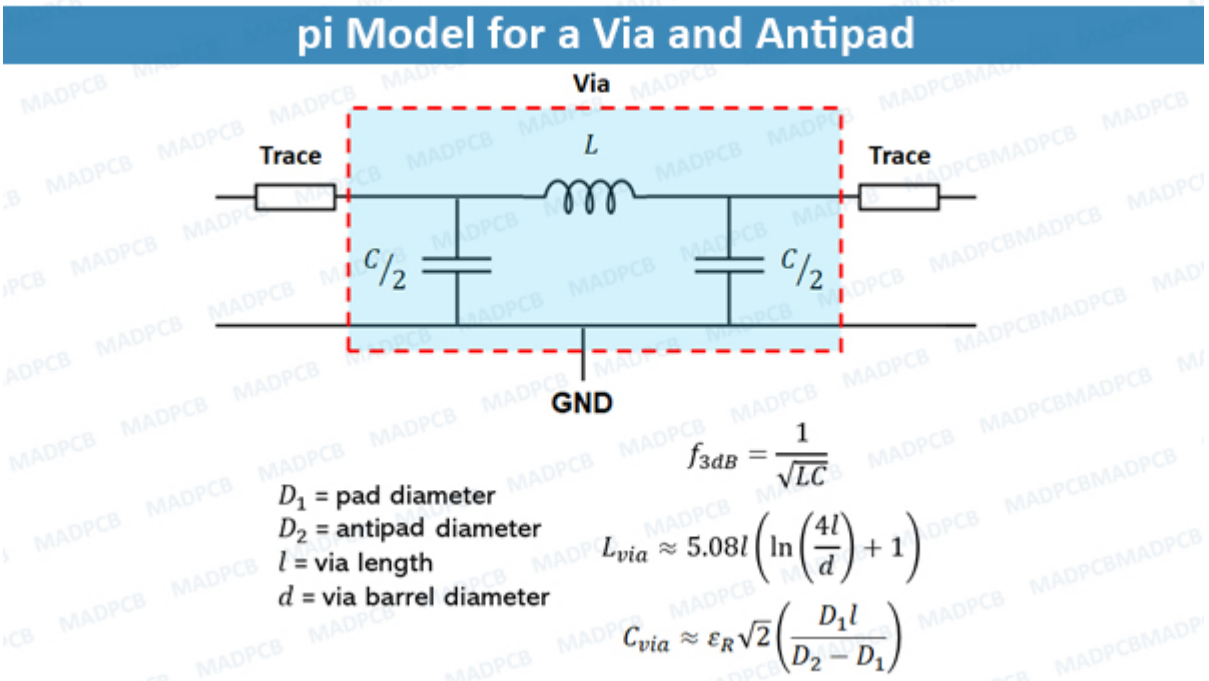
At this point, if you're routing through a solid plane, the question is not whether you should use a

via antipad or cut away the plane around the, but rather how large should the antipad extend past the via pad and any internal non-functional pads. Like many potential problems in high-speed design, all vias have parasitics:

Inductance: A via taken in isolation is basically any inductor, and the inductance of the via depends on the via aspect ratio.

Capacitance: The presence of the plane around creates some parasitic capacitance between the via pads and ground.

Each pad at the end of the via and the intervening plane creates two capacitors in parallel. When combined with an inductor, we have a standard pi model describing a via and their anti-pads, as shown below. Note that the capacitance equation shown below is only an approximately as it does not consider fringing fields. The via inductance equation is also an approximation.



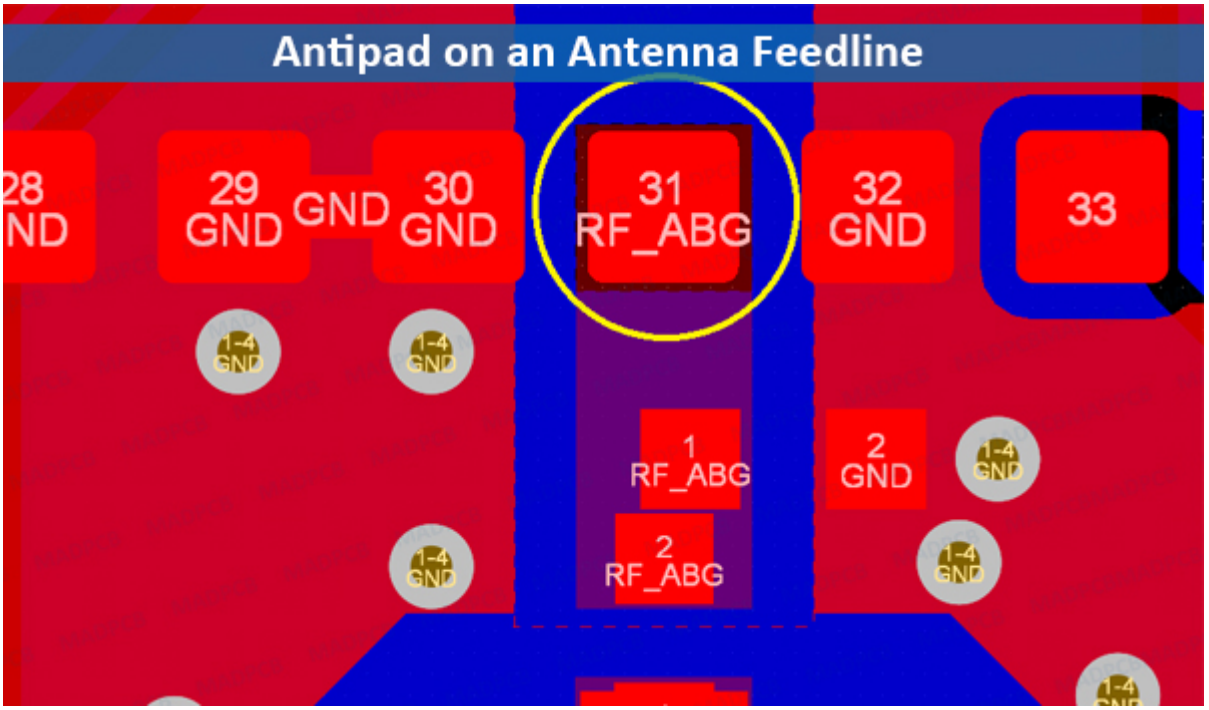
pi Model for a Via and Antipad

What happens next (in terms of electrical behavior) depends on a number of factors. First, just like any pi circuit, the CLC pi model is basically a low-pass filter with a 3dB cutoff frequency defined above. Suppose you want to extend the bandwidth of your via + antipad arrangement. In that case, you'll need to reduce the aspect ratio (shorter via or wider barrel diameter), or decrease the pad-plane-pad capacitance (larger antipad).

Here, you have a difficult set of options to balance. Modern designs are getting denser with smaller features, so there is a danger your aspect ratio becomes quite large, the 3dB frequency would decrease and limit bandwidth. Once you get to the mmWave regime, you'll have other signal integrity challenges involving routing through vias. Additional parasitics become dominant at these frequencies and contribute to overall insertion loss along an interconnect.

How an Antipad on a Landing Pad Affect Signals?

Placing an antipad on a landing pad involves cutting away some ground plane beneath a pad on a component. An example on an antenna feedline is shown below (pad + antipad is circled in yellow). The antipad in the blue ground plane region is shown below and was placed as a polygon cutout.



Antipad on an Antenna Feedline

There is one good reason to do this, but there are other reasons you should not do this, and they outweigh each other at different frequencies and in certain situations. In the above case, placing the antipad eliminates some parasitic capacitance; the field carried by a signal then couples back to the ground plane only through fringing fields. This is one alternative to using a smaller landing pad.

The above example is a bit contrived, and I would not do this in a customer's board without validation through simulations, but it illustrates a good point about return path planning. Even though there is a ground cutout below the pad, there is still a clear return path through nearby vias and ground pour, so a major impedance discontinuity is not created in this process. Without such assistance from ground pour and vias back to a reference plane, you'd create a significant impedance discontinuity due to a large return path.

If you want to control via bandwidth and parasitics, you have a few levers you can pull. Antipads on vias give you a simple way to tune the parasitic capacitance to match the inductance for a given via aspect ratio. The dielectric constant (Dk value only) can also be used as a tool for controlling via capacitance.

Regarding antipads on landing pads, you'll create a small impedance discontinuity, which can create some small insertion loss and return loss at the pad. In high speed channels where bandwidths can extend up to 100 GHz and beyond, every last bit of insertion loss you can avoid is critical. My view is to play it safe and not use any antipads on landing pads unless you absolutely

need to do this to set a landing pad's impedance to some specific value, thereby reducing return loss. Antipad PCB manufacturing should take much care on layers registration.