PCB Breakout Routing for High-Density Serial Channel Designs Beyond 10 Gbps

AN-651-1.0 Application Note

Altera® Stratix V® FPGAs offer up to 66 transceiver channels per device for fast data rates to meet increasing system bandwidth demands. As a result of the high transceiver count, board designers may find it difficult to route all the channels while keeping control of the board cost. This application note compares several serial channel breakout routing techniques to help you meet 10 Gbps to 28 Gbps data rate channel performance while balancing the performance versus cost trade-offs. Specifically, the channel breakout underneath the ball-grid array (BGA) has an impact on the board signal integrity and cost.

This application note discusses how to appropriately design the channel breakout in the BGA via field region while reducing PCB cost. Detailed layout design examples and simulation results are presented to compare the performance of the routing topologies. Simulation results of insertion loss, return loss, and crosstalk performance are compared to demonstrate the impact of the different breakout routing schemes.

Transceiver Breakout

Figure 1 shows a typical via pattern for a Stratix V GX device with 66 transmitter (TX) and receiver (RX) transceiver pairs in a 1760 pin FPGA package, arranged symmetrically as 33 TX and RX pin pairs per side (gold pins) surrounded by GND pins (black pins).

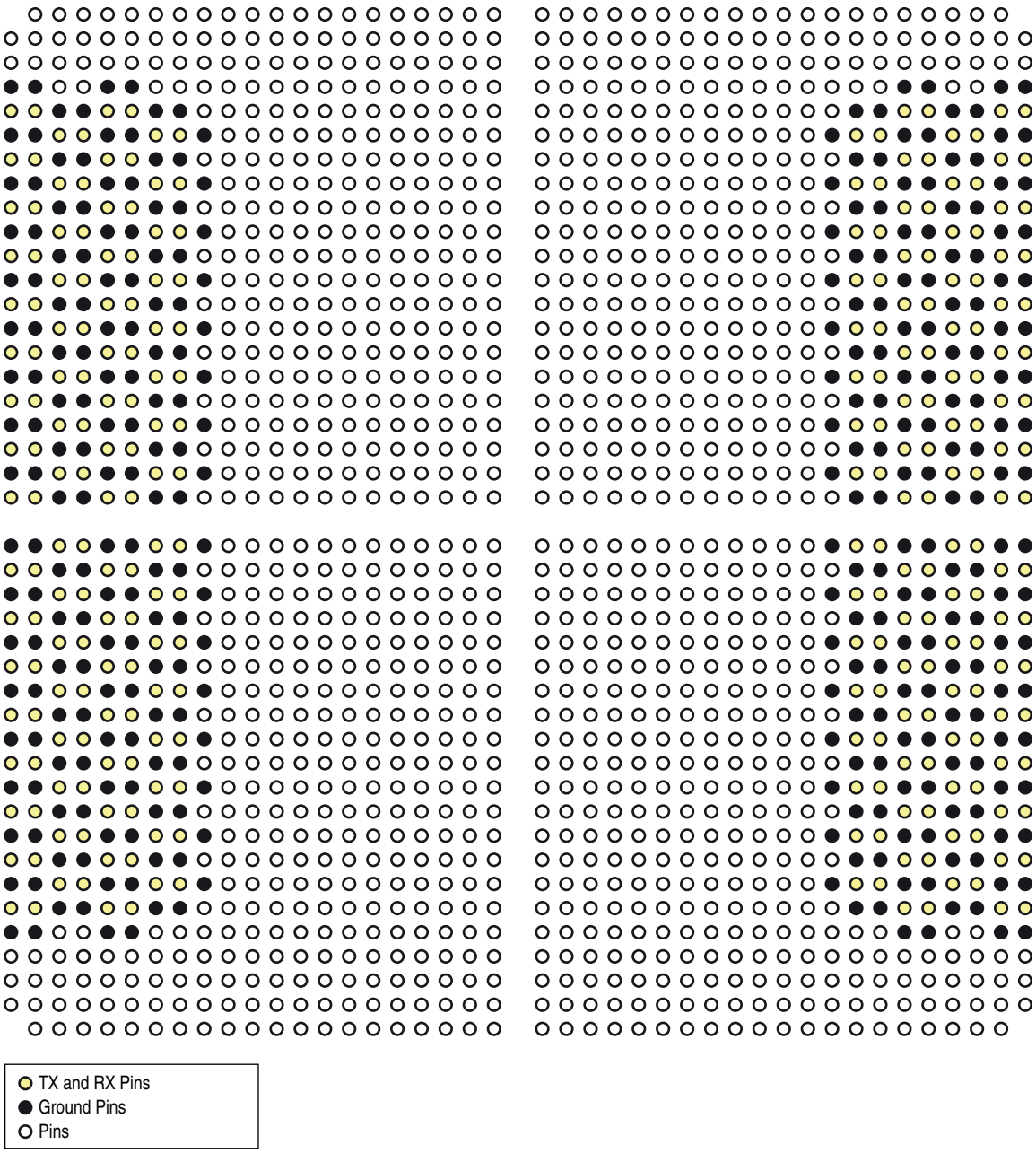
101 Innovation Drive
San Jose, CA 95134
www.altera.com

© 2011 Altera Corporation. All rights reserved. ALTERA, ARRIA, CYCLONE, HARDCOPY, MAX, MEGACORE, NIOS, QUARTUS and STRATIX words and logos are trademarks of Altera Corporation and registered in the U.S. Patent and Trademark Office and in other countries. All other words and logos identified as trademarks or service marks are the property of their respective holders as described at www.altera.com/common/legal.html. Altera warrants performance of its semiconductor products to current specifications in accordance with Altera's standard warranty, but reserves the right to make changes to any products and services at any time without notice. Altera assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Altera. Altera customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services.

ISO 9001:2008 Registered

Subscribe

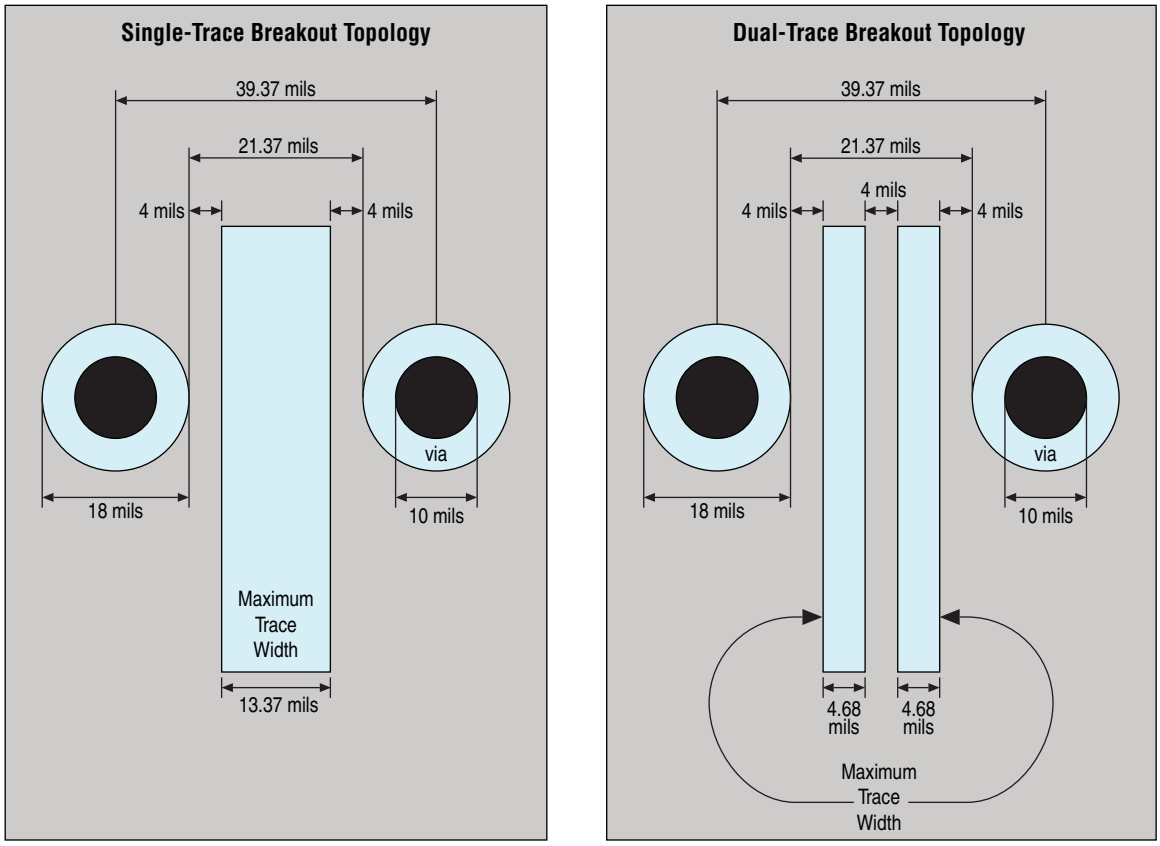
Figure 1. 66 Transceiver Stratix V GX in a 1760 FPGA Package



With a 1 mm (39.37 mil) ball pitch FPGA package, you can use two signal breakout routing options on the standard PCB fabrication technology that uses 4 mil minimum copper-to-copper clearances and a 10 mil drill with an 18 mil via pad. Figure 2 shows these two breakout routing topologies and the resulting maximum allowable trace width that can be used based on the minimum copper clearance requirements. A single trace with a maximum width of 13.37 mils may be routed between the 39.37 mil

via pitch. Similarly, the resulting maximum trace width is reduced to 4.68 mils when dual-trace breakout is used. Ideally, all transceiver TX and RX pin pairs should be routed as either 100-Ω or 85-Ω differential pairs for the best transceiver signal performance depending on the target mating connections. For this application note, 100-Ω target impedances are assumed.

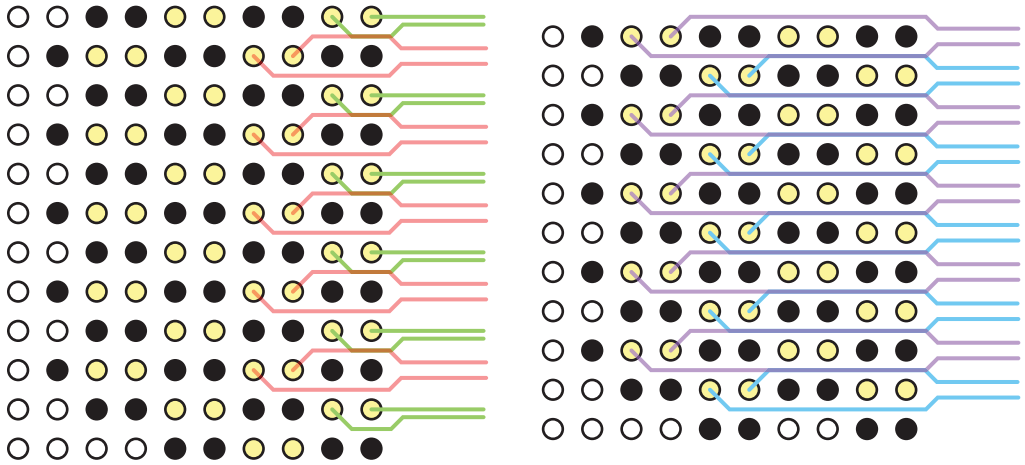
Figure 2. Single and Dual Trace Breakout Topology



Single Trace Breakout

In the single trace breakout topology, four layers are required to fully route all the TX and RX transceiver signals, because only one trace is routed between the BGA via grid per layer. Figure 3 shows a portion of the routing pattern when using the single trace breakout approach. The breakout pattern is actually repeated throughout the entire left and right side of the device for all 66 TX and RX channels.

Figure 3. Single Trace Breakout Layer Usage



Using this topology requires more signal layers and increases PCB cost, but allows you to maintain a constant trace width for the entire trace route because of the adequate via-to-copper clearances. Additionally, when using this routing topology, the inner to outer most transceiver pairs must be successively routed on lower layers of the PCB to allow optimum use of backdrilling as shown in Figure 4. In Figure 4, four different backdrill depths can be achieved to minimize via stubs on all transceiver routing layers. If this layer assignment rule is not strictly enforced, the backdrill depth must be compromised to avoid cutting into signal traces routed on lower layers.

Figure 5 shows an example of a poor transceiver layer assignment where the inner most transceiver signals are routed on the lowest layer of the PCB. This specific case results in limiting all backdrills to just a single depth. The end result is excess via stubs for the remaining transceiver signals routed on higher layers and degraded transceiver signal performance.

Figure 4. Optimum Layer Assignment for Effective Backdrill

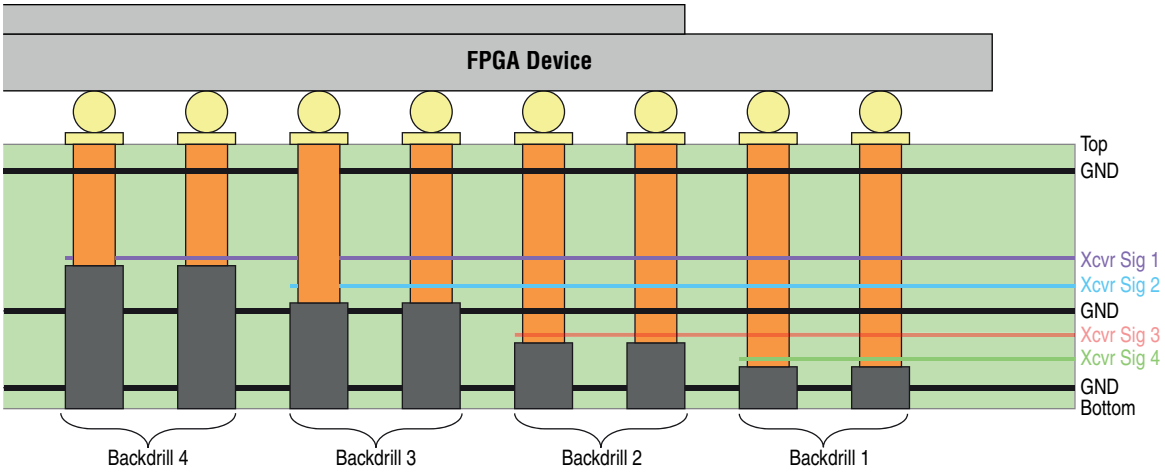
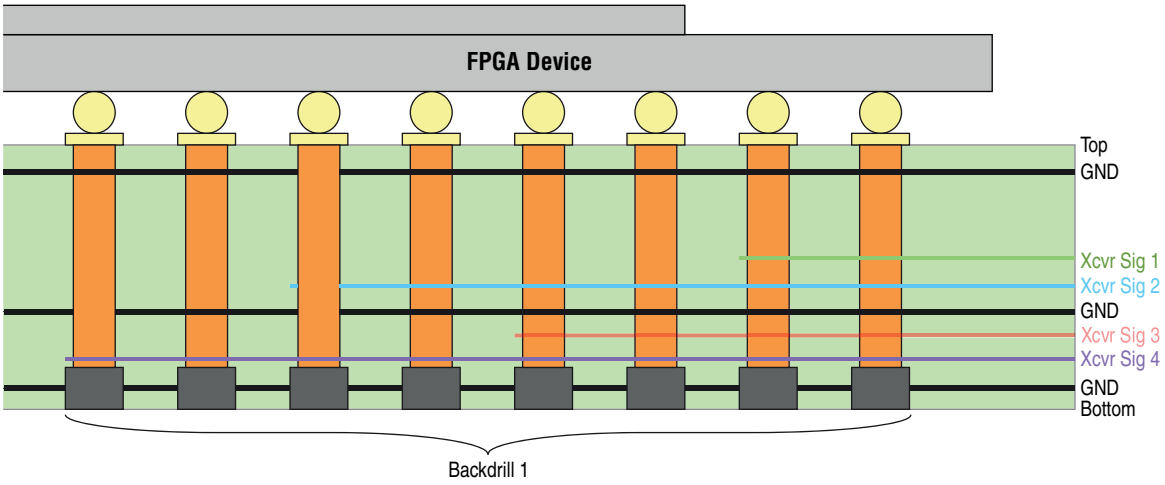


Figure 5. Poor Layer Assignment Limits Backdrill Effectiveness

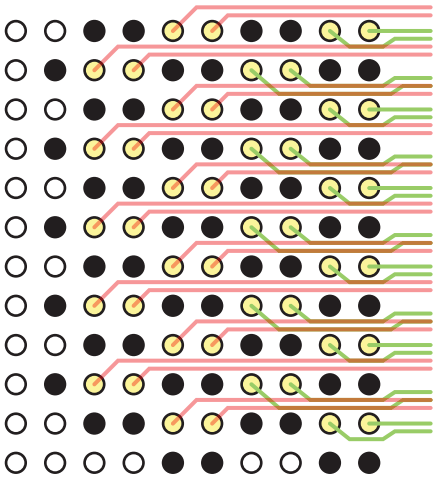


Dual Trace Breakout

In the dual trace breakout topology, both the signal and its complement in the differential pair are routed between the BGA via grid. To meet the minimum 4 mil copper-to-copper clearance requirement, the maximum allowable trace width between the BGA via field is 4.68 mils. This maximum allowable trace width results in a trace neck-down where the 100-Ω trace reduces to 4.68 mils as it enters the BGA via field. This trace neck-down occurs because the 100-Ω differential transceiver trace routes typically use wider trace widths (5 to 7 mils, depending on the PCB stackup construction) to compensate for higher skin effect losses at higher frequencies.

The neck-down causes an impedance discontinuity on the critical transceiver trace, resulting in degraded signal performance. However, this topology maintains tight trace p-n coupling while reducing layer count and PCB cost. Figure 6 shows the routing pattern for the dual trace breakout topology. Using this breakout consumes only two routing layers for the same 66 transceiver channels. The layer assignment restriction must follow the inner-to-outer, successively higher-to-lower layer assignment rule for optimum backdrill effectiveness, as shown in Figure 4.

Figure 6. Dual Trace Breakout Layer Usage



Crosstalk

For both single and dual trace topologies, crosstalk due to adjacent layer broadside coupling can occur in the BGA grid region since it is difficult to avoid adjacent layer trace overlap in a GND-Signal-Signal-GND (GSSG) stackup construction. The typical solution is to increase the dielectric spacing between the adjacent signal layers, or add an additional GND layer between the adjacent signals for better isolation. Increasing spacing is possible if the total board thickness can be kept under a 10:1 (typical) via aspect ratio. Using via aspect ratios greater than 10:1 can incur a significant cost penalty because the standard PCB via drilling and plating processes cannot be used. Also, adding a GND isolation layer actually involves two layer additions to maintain a balanced PCB stackup. This layer addition increases the total PCB thickness and cost. For this situation, the dual trace topology provides better crosstalk immunity over the single trace topology. The coupled noise is comparable on both traces due to their proximity to the adjacent layer aggressor. As a result, the effect of this crosstalk is easily cancelled for differential signals. In contrast, the common mode noise rejection for the single trace topology is not as effective because the noise coupling is unbalanced compared to the dual trace topology.

Simulation Setup

The following Ansoft HFSS 3D simulations compare the performance of the two routing topologies. Figure 7 shows the simulation model for the single trace breakout and Figure 8 shows the model for the dual trace breakout. In both models, a GSSG stackup construction is used with the dimensions listed in the table in Figure 7. The trace in each simulation is strategically routed on layers near the bottom of the board to minimize the via stubs so that modeling of the via backdrilling is not required. Port

assignments used in the simulation are shown in Figure 7 and Figure 8 for reference. The table in Figure 7 lists the value of the single-ended impedance as 51.3 Ω when the trace width is 5.5 mils. The table in Figure 8 lists the value of the differential impedance as 98.5 Ω in the same stackup when the trace width is 5.5 mils with an airgap of 11.5 mil, and 93.8 Ω when the trace width is necked down to a 4 mil width with a 4 mil airgap as shown in Figure 8.

Figure 7. HFSS Setup for Single Trace Breakout

	Layer Name	Usage	Thickness mils, oz	Er	Target Z0 ohm	Width mils
1	Nelco_4K13EPSI	Substrate	12	3.4		
2	GND	Plane	0.6	<Auto>		
3	Nelco_4K13EPSI	Substrate	4	3.4		
4	SIG1	Signal	0.6	<Auto>	51.3	5.508
5	Nelco_4K13EPSI	Substrate	9.5	3.4		
6	SIG2	Signal	0.6	<Auto>	51.3	5.508
7	Nelco_4K13EPSI	Substrate	4	3.4		
8	GND	Plane	0.6	<Auto>		
9	Nelco_4K13EPSI	Substrate	12	3.4		

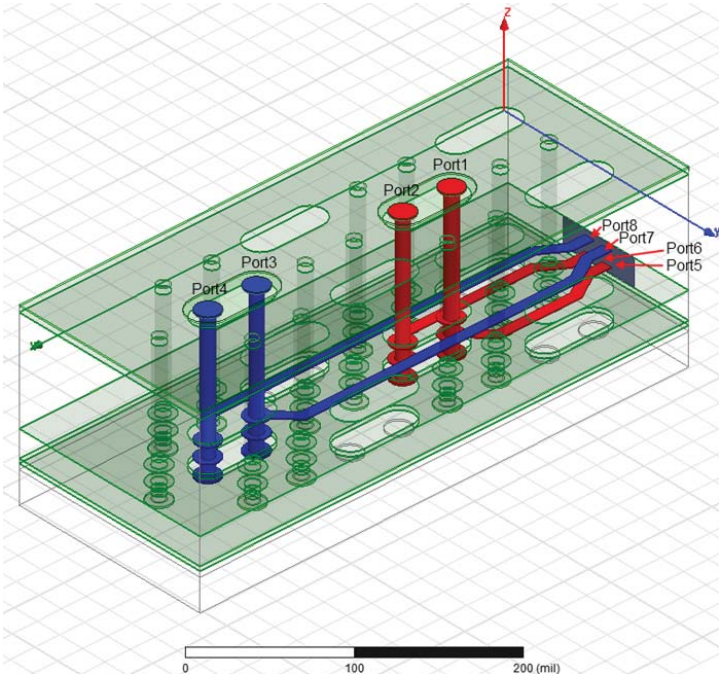
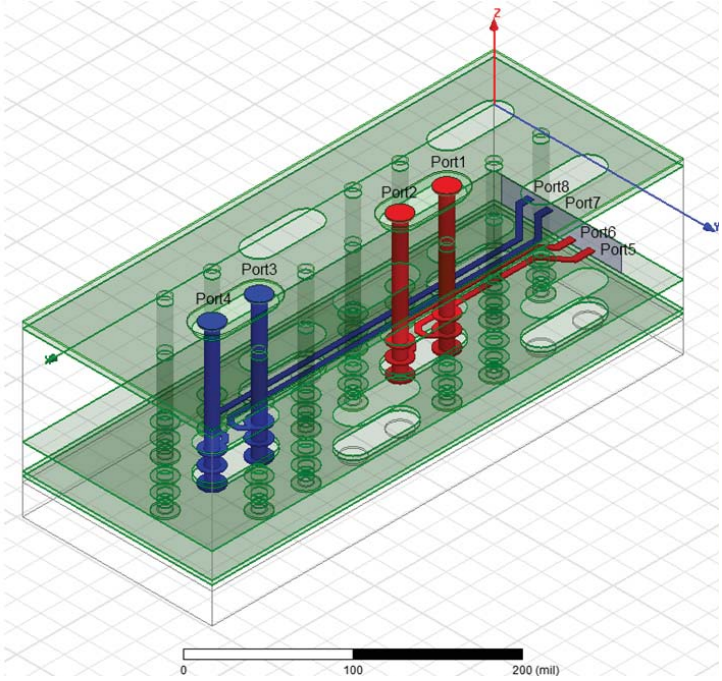


Figure 8. HFSS Setup for Dual Trace Breakout

	Layer Name	Usage	Thickness mils, oz	Er	Diff Z0 ohm	Width mils	Gap mils
1	Nelco_4K13EPSI	Substrate	12	3.4			
2	GND	Plane	0.6	<Auto>		1	
3	Nelco_4K13EPSI	Substrate	4	3.4			
4	SIG1	Signal	0.6	<Auto>	98.5	5.5	11.555
5	Nelco_4K13EPSI	Substrate	9.5	3.4			
6	SIG2	Signal	0.6	<Auto>	93.8	4	4.003
7	Nelco_4K13EPSI	Substrate	4	3.4			
8	GND	Plane	0.6	<Auto>		1	
9	Nelco_4K13EPSI	Substrate	12	3.4			



Simulation Results

The following simulation results compare the impact of the two breakout topologies in terms of differential insertion and return losses, and crosstalk.

Figure 9 and Figure 10 show the differential insertion loss (Sdd21) and return loss (Sdd11) for the deep trace (port3, port4) versus the shallow trace breakout (port1, port2) for both the single and dual trace breakout topologies.

In Figure 9, the differential insertion loss difference between the two breakout schemes for data rates between 10 Gbps to 28 Gbps is minimal (0.2 dB maximum for Nyquist frequencies between 5 GHz to 14 GHz). However, the return loss comparison is higher (up to 5 dB maximum for the deep trace breakout at the 5 GHz to 14 GHz Nyquist as a result of reflections from the trace neck-down discontinuity).

Figure 9. Insertion and Return Loss to Deep Trace Breakout

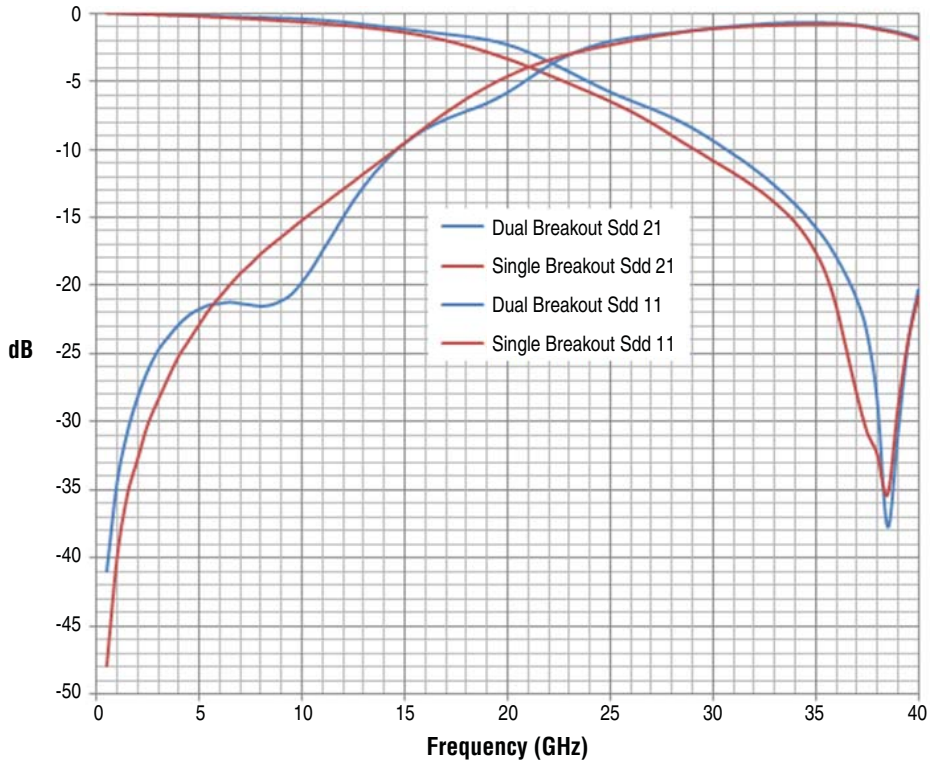


Figure 10. Insertion and Return Loss to Shallow Trace Breakout

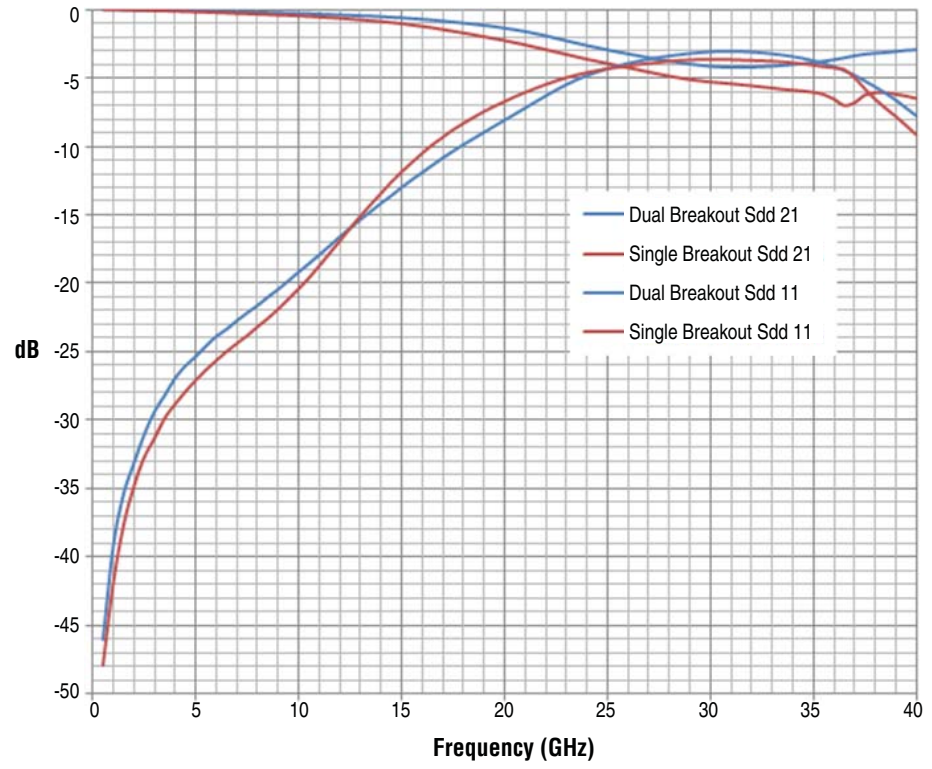


Figure 11 and Figure 12 can be compared to show the common mode rejection and crosstalk immunity for both breakout topologies. In Figure 11, the common mode rejection of the dual trace breakout topology is better than the single trace breakout by up to 2 dB in the Nyquist frequency range of 6 GHz to 14 GHz. Similarly, Figure 12 shows the differential crosstalk immunity for the dual trace breakout is significantly better than the single trace breakout by up to 10 dB for Nyquist frequencies up to 18 GHz.

Figure 11. Common Mode Rejection

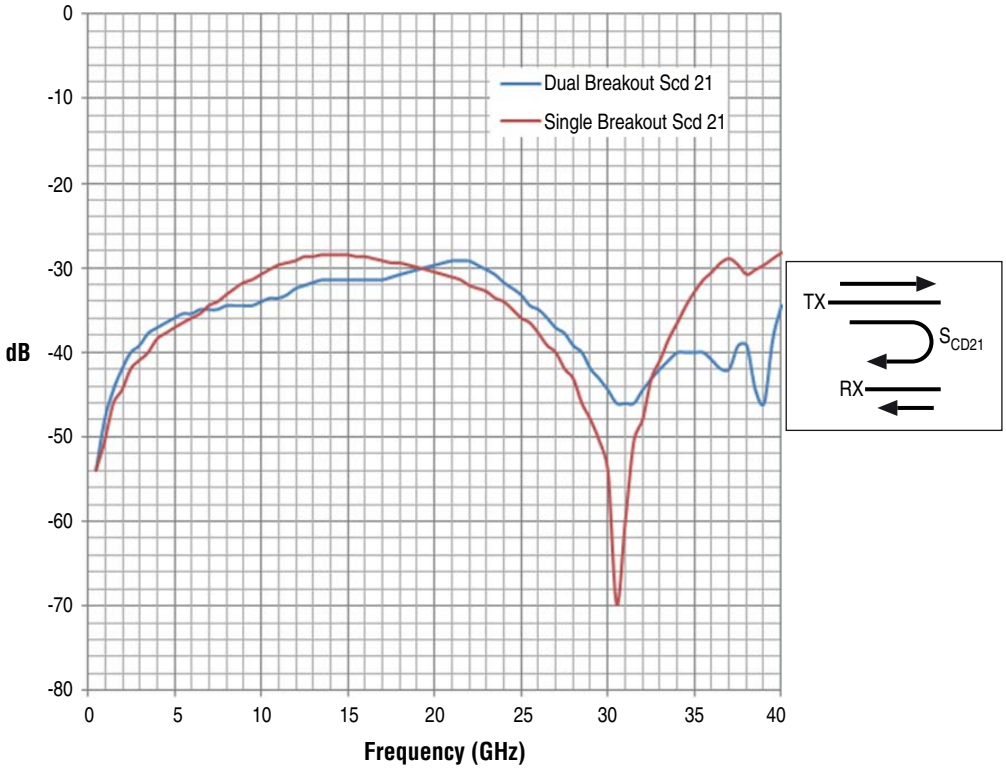
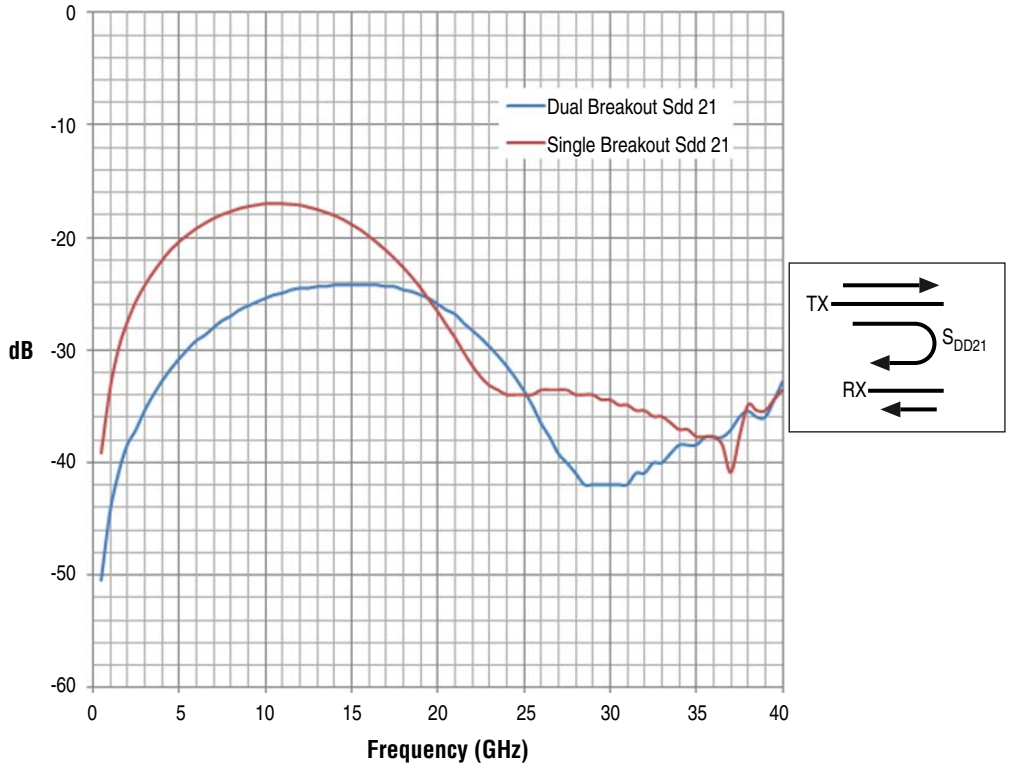


Figure 12. Crosstalk



Conclusion

Simulation results show that both single and dual trace breakout topologies have similar insertion and return loss characteristics. Additionally, the dual trace breakout topology has better common mode noise rejection and crosstalk immunity for 10 Gbps to 28 Gbps applications. As a result, when routing high density transceivers that run at data rates of 10 Gbps–28 Gbps, use the dual trace breakout instead of the single trace breakout topology because it saves PCB cost by reducing layer count and achieves similar performance. In both topologies, signal layer assignment restriction must follow the inner-to-outer, successively higher-to-lower, layer assignment rule to avoid compromising the transceiver signal via backdrilling.

Document Revision History

Table 1 lists the revision history for this document.

Table 1. Document Revision History

Date	Version	Changes
November 2011	1.0	Initial release.