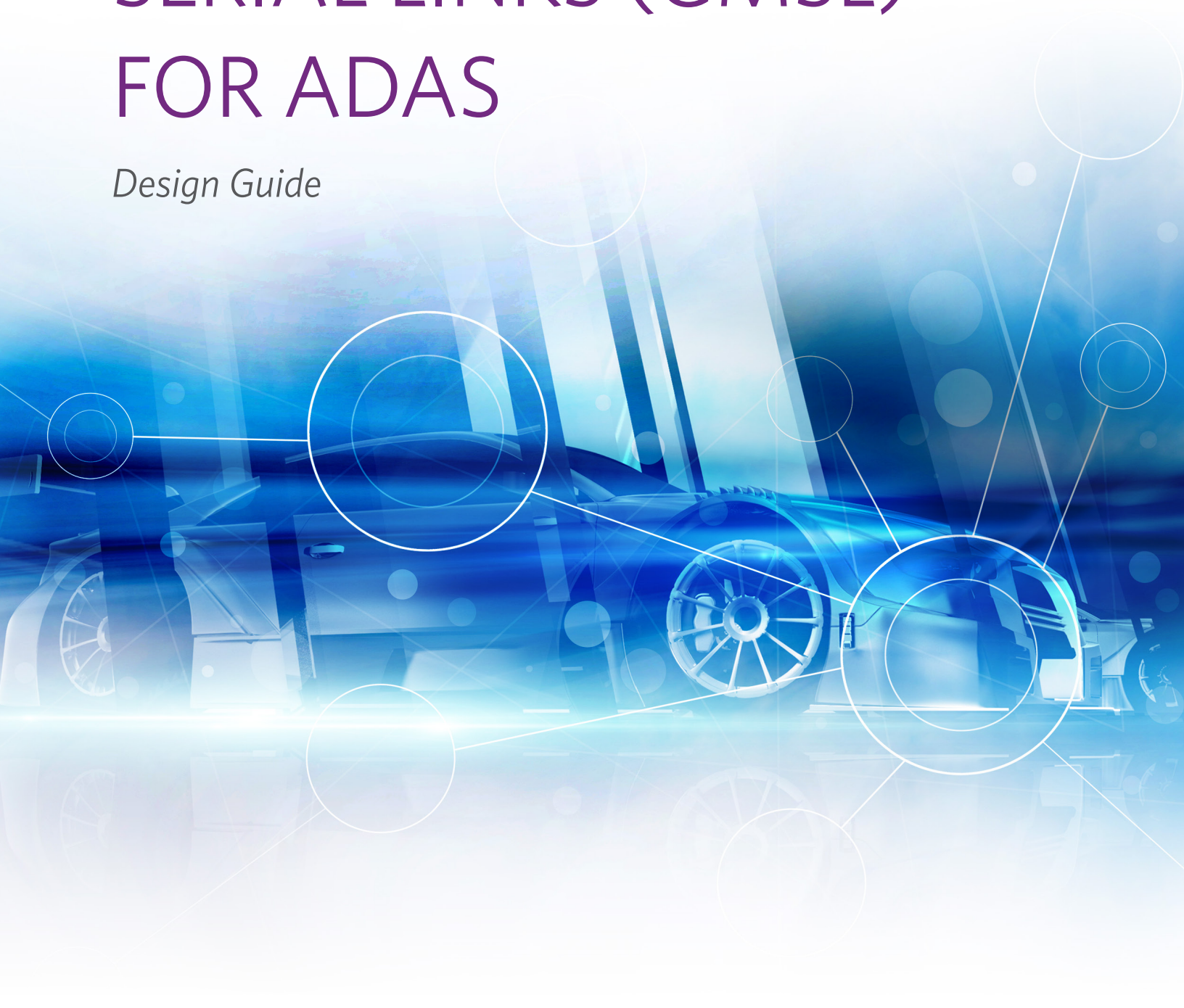
GIGABIT MULTIMEDIA SERIAL LINKS (GMSL) FOR ADAS

Design Guide



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Synopsis

Gigabit Multimedia Serial Links (GMSL) for Camera-Based Systems

Increased road awareness is a critical component for driver safety and the future of self-driving cars. Maxim's Serializer-Deserializer (SERDES) products enable high-performing camera systems with robust, compact, and flexible communication links. The MAX967xx family has new features that demonstrate Maxim's commitment to helping design a safer, smarter car of the future.

ADAS Overview

Road safety has vastly increased due to continued developments in the automotive space known as ADAS. Some technologies take effect autonomously, operating the vehicle with complete control during given events (Table 1). Other technologies provide information to those on-board, such as blindspot detection, but leave control with the driver. As the idea of self-driving cars continues to gain more traction, driver and passenger safety become an increasing concern. Many of the features in ADAS technology are enabled with the increased usage of cameras placed throughout the vehicle (Figure 1).

Table 1. ADAS Technology Applications

Improved Visibility	Enhanced Control	Cabin Safety
Back-Up Assistance	Adaptive Cruise Control	Seatbelt Detection
Surround View	Automated Parking	Driver Distraction
Blind Spots & On-Coming Traffic	Lane Detection & Centering	Airbag Deployment
Road Sign Detection	Head Beam Direction	Driver Drowsiness Detection

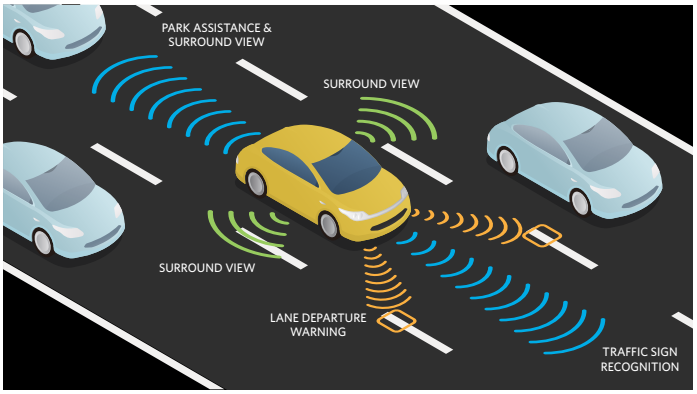

Figure 1. Diagram of ADAS Application Locations

Camera Technology Requirements

In ADAS applications involving cameras (Figure 2), the critical design challenge is to get image data from the camera to the processing unit and from the processing unit to each display as quickly and efficiently as possible. Some of the key tradeoffs in designing ADAS camera systems are image quality, bandwidth, latency, reliability, cost, and power consumption.

- **Bandwidth** - Performance demands are different from each camera depending on its purpose. For example, a back-up assistance camera with wide-angle lens may feature 1.3 megapixels with 18-bit color per pixel at 30fps. Including the control bits and encoding for balance, this single camera would generate > 1Gbps of data!
- **Latency** - At 62.5mph (100km/hr), a vehicle travels 91.13 ft (27.8m) every second. For passenger and traffic safety, every second counts.
- **Reliability** - Adapting to wear and tear over the lifetime of a vehicle and detecting when service is required is essential to keeping everything running smoothly.
- **Power Consumption** - As more electronic systems are added to vehicles, staying within battery capacity and distribution constraints becomes an increasing challenge.
- **Cost** - Reducing the number of components and cables while increasing system capability is essential to keeping system costs low and the technology competitive.
- **Image Quality** - ADAS that is based on vision-based object detection relies on the images it needs to process. Hence, high-quality images are absolutely essential.

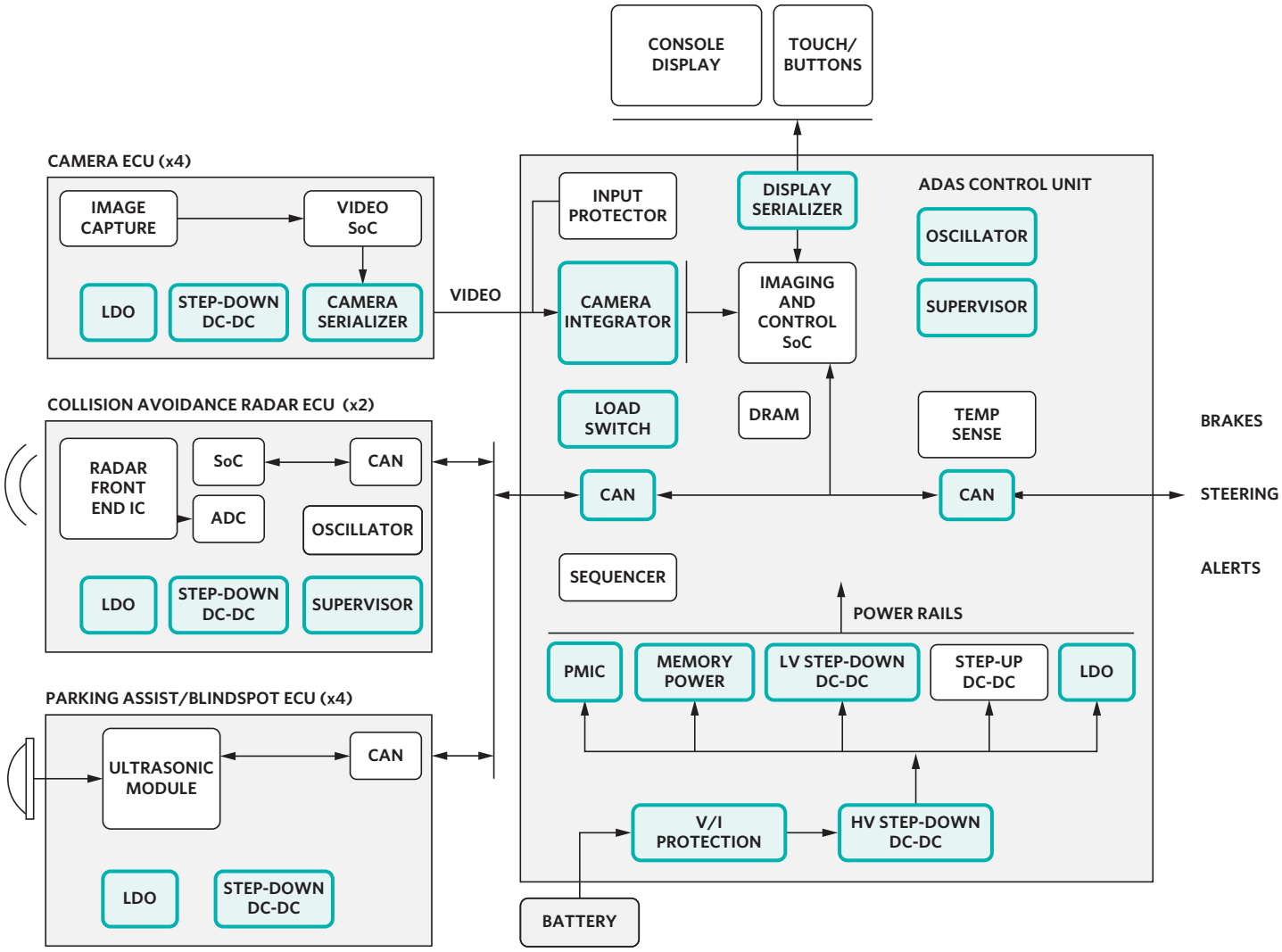

Figure 2. ADAS Block Diagram

MAX967xx GMSL SERDES
Empowering Design Innovation

The latest SERDES products from Maxim Integrated provide increased reliability and flexibility for uncompressed camera feed transmission systems. SERDES chipsets work by taking the uncompressed parallel video output from an image sensor, combining it with control inputs and serializing it into a single high-speed output, transmitting the data across a cable, and then converting the received signal into the original parallel video output on the deserializer side. Many systems are built to provide both power and high-speed bidirectional data through the same cable. The MAX967xx family offers new safety and reliability features specifically for ADAS applications (Figure 3).

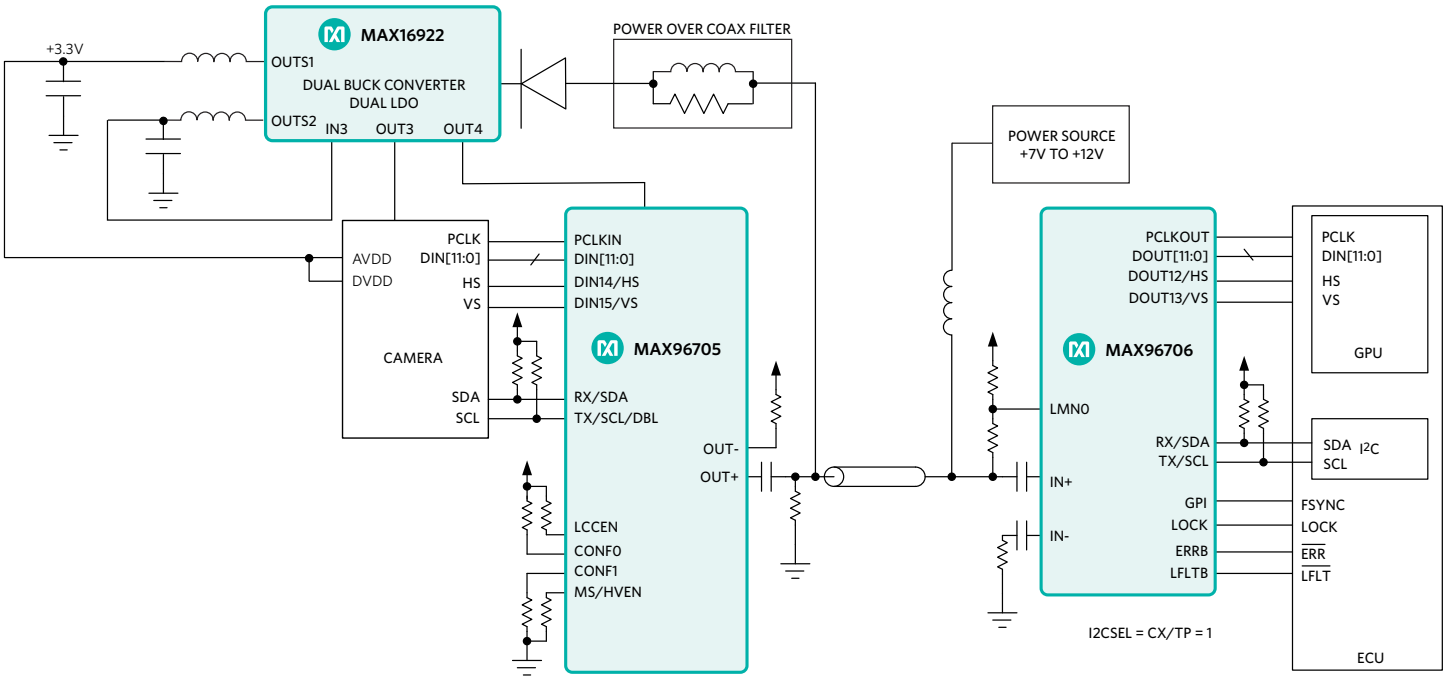

Figure 3. Typical Application Circuit for Back-Up Assistance GMSL SERDES Systems

MAX967xx Features for ADAS Applications

1. Control Channel Error-Detection and Retransmission

- Ensures 100% accuracy when configuring link
- Reliable communication for peripherals accessed through control link

2. Crossbar Switch

- Any parallel input to any parallel output
- Enables different camera modules for one host board
- Enables one camera module for several host boards

3. Reduced EMI/EMC

- Programmable output spread spectrum
- Ability to propagate spread input clock to deserializer
- High-immunity mode for control channel EMC tolerance

4. Enhanced Cable Drive

- 50Ω Coax or 100Ω Shielded Twisted Pair
- Programmable pre-emphasis and de-emphasis allows 15m cables at full speed
- Line-fault monitoring available

5. Eye-Width Monitor & Adaptive Equalization

- Built-in cable equalizer for long cable drive
- Eye-width monitor can trigger equalizer re-tune

6. Flexible Data Input up to 1.74Gbps

- 12.5MHz to 87MHz at 14-bit input + HSYNC and VSYNC
- 36.66MHz to 116MHz at 12-bit input + HSYNC and VSYNC

7. AEC-Q100 Qualified

8. Dedicated Frame Sync GPO

Crossbar Switch

With the inclusion of a crossbar switch, any data input can be configured to route to any data output. This feature allows for easing layout constraints and enabling design reuse, which could significantly cut development costs.

If image sensors with different output buses are supported for a given application, all sensors can interface to the same MAX967xx serializer board (Figure 4). The crossbar switch can be configured in each scenario to ensure the signals applied to the serializer are routed to the appropriate deserializer output. By designing one serializer board that interfaces with different camera modules, instead of one serializer board specific to one image sensor, the total design time is drastically cut.

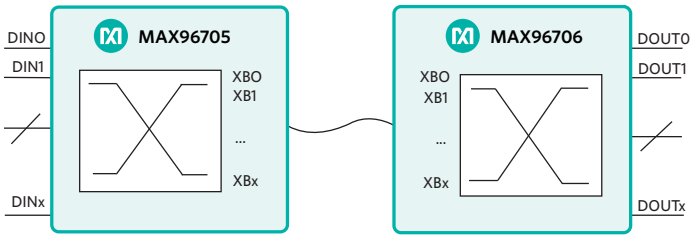

Figure 4. Basic Representation of Crossbar Switch

The same benefit can be realized on the deserializer side. For a single camera module and serializer combination, a number of different deserializer boards and graphics processor combinations can be used to interpret the incoming camera data. The increased compatibility is simply enabled with the use of an internal crossbar switch.

Line Fault Detection

Some parts in the MAX967xx product line feature built-in line fault detection (Figure 5). By attaching an external resistor network from the serial link to the LMN0/LMN1 pins and including a reference voltage between 1.5V and 1.7V, the system can automatically detect the physical state of the serial link. An optional hardware pin, LFLTB/GPIO1, can be used to raise a flag if an open cable, short to battery, or short to ground is detected. Two line fault monitor pins, LMN0 and LMN1, are included for use with single-conductor coax cables and shielded twisted pair (STP) cables.

The normal operating threshold for the LMN0/LMN1 pins is 0.57V to 1.07V. If the cable is shorted to GND, the line voltage is pulled below this threshold. If the cable is open, the line voltage is pulled up to the reference voltage between 1.5V and 1.7V. If the cable is shorted to the battery, the line voltage is pulled higher than 2.5V.

The **MAX96711** serializer contains the line fault detection feature. The **MAX96706** and **MAX96708** deserializers also have this feature.

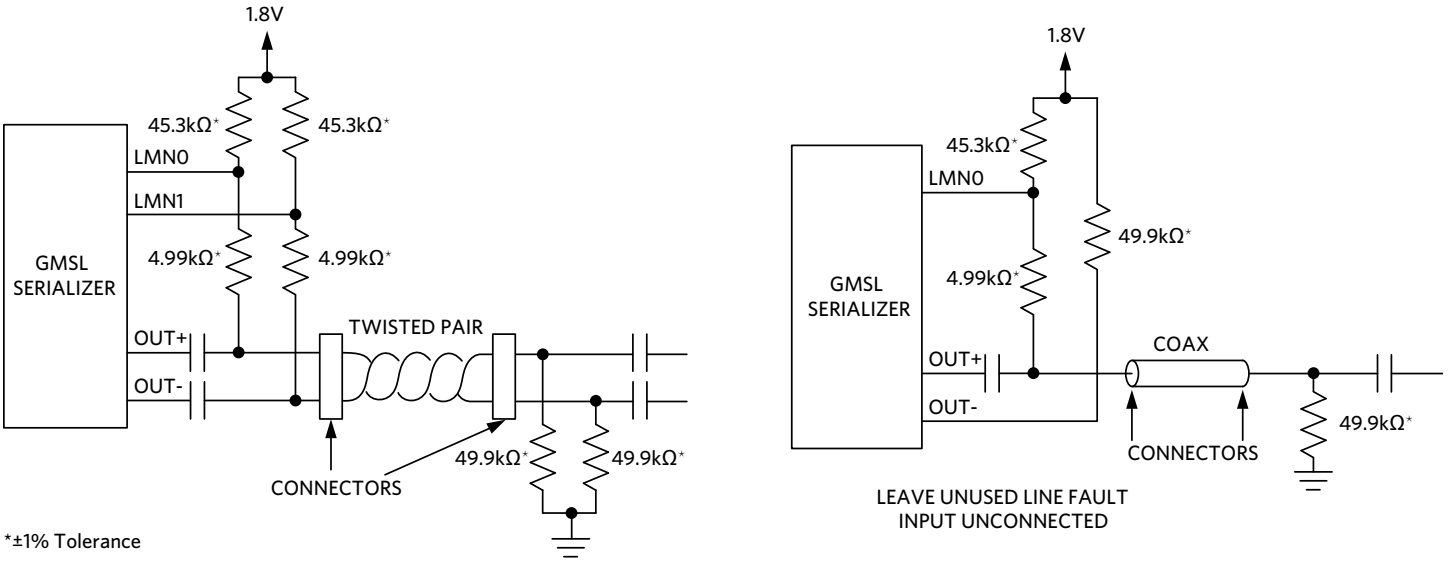

Figure 5. Line Fault Detection for STP (left) and Coax (right) Cables

Power Over Coax

In many systems, one STP cable actually has two pairs inside—one for power and one for data. Using coax cables instead of STP cables for SERDES links has advantages—they're cheaper, lighter, more flexible, and less lossy at high frequencies. To make using a low-cost coax cable competitive, it must also provide both power and data through a single cable. To achieve this, the available frequency spectrum on the inner conductor is divided into three bands—power, reverse-channel data, and forward-channel data (Figure 6). Filtering is used to pass the appropriate frequency band to its corresponding circuit. The data channels are AC-coupled through a series capacitor to the transceiver inputs.

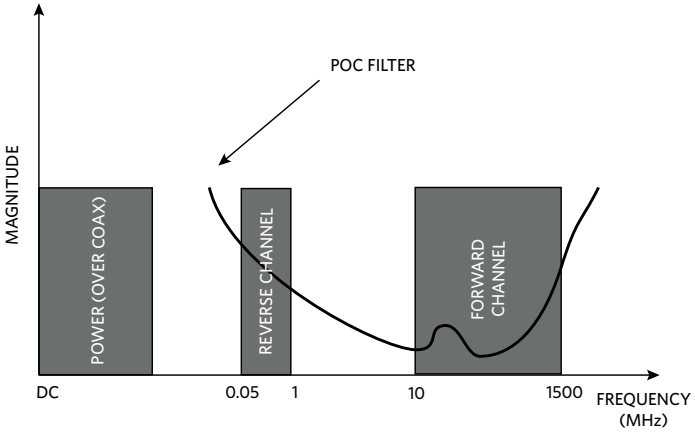

Figure 6. Frequency Bands Used in Coax GMSL Systems

The DC power typically uses the lowpass quality of series inductors to construct filters whose impedance rise above 1kΩ in the reverse-channel and forward-channel frequency bands. Since the data channels operate with 50Ω termination, the 20x increase in impedance is sufficient to couple the DC voltage and filter the high-frequency content. Since every inductor has parasitic capacitance that causes self-resonance and a corresponding drop in impedance at high frequencies, inductors of different sizes are chosen to filter out all the bands of interest.

All of the current delivered across the cable must pass through each inductor in the power filter, which places additional constraints on inductor parameter selection including: saturation current, DC winding resistance, and package size. If a current greater than I_{SAT} flows through an inductor, its magnetic field saturates and the inductance drops steeply. There is a power loss proportional to the current through the inductor and its DCR, which causes self-heating to occur. If there is no voltage margin built into the power delivery rail, the voltage drop across the power filter may cause insufficient voltage levels at the load.

To avoid all three of these potential problems, a higher voltage is applied to the cable, which results in lower cable current. Additionally, inductors with sufficient size and saturation current rating are chosen to handle the required cable current. The MAX967xx product line features best-in-class power consumption to ease the requirements in the power over coax circuit.

Adaptive Equalizer

All cables have a parasitic impedance that degrades signal quality as frequencies increase. Longer cable lengths also contribute to signal degradation. Many high-speed transmission systems compensate for the lowpass nature of a transmission cable by placing a cable equalizer at the front end of the receiver input. Equalizers amplify high-frequency signals of interest such that, when combined with the frequency response of the cable, the receiver can recover broadband signals with higher fidelity.

The MAX967xx deserializers have built-in adaptive equalizer circuitry. With 12 different compensation levels, the equalizer allows the SERDES system to handle up to 30m coax and 15m STP cable lengths.

The adaptive equalizer can be programmed to readapt periodically, or it can be triggered manually to compensate for any changes in the transmission environment. As cables are worn over time and replaced, the system can adapt itself for optimal operation by automatically setting the adaptive equalizer level (Figure 7).

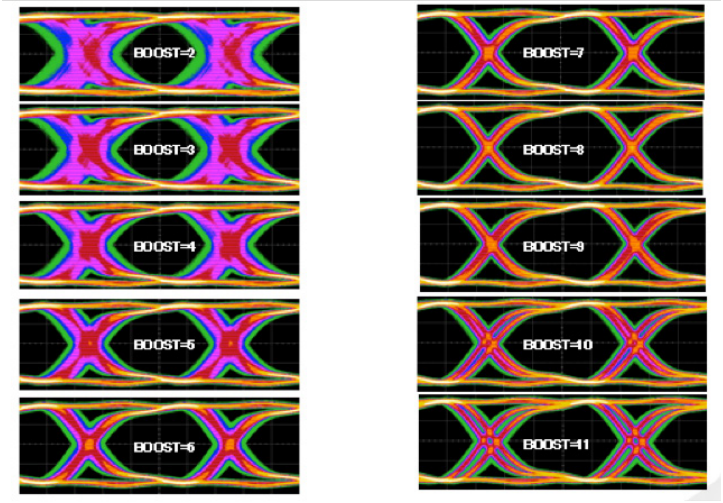

Figure 7. Eye Diagram at GMSL Receiver with Varying Settings

Eye-Width Monitor

Another feature for increasing the robustness of high-speed communication over a long cable is the addition of eye-width monitoring circuitry. By sending a pseudo-random bit sequence (PRBS) across a transmission line and plotting the transitions, a persistent plot is generated that represents an eye. With a stable clock and compensated cable, the transitions in an eye diagram are narrow, resulting in an 'open' eye. As cable quality decreases or cable length increases, the high-frequency content of each transition is attenuated and the eye starts to close.

The MAX96706 includes an eye-width monitor that senses the eye-width opening. If it senses the eye width decreasing below a threshold, it raises a flag on the ERRB output pin or even triggers a re-tuning of the adaptive cable equalizer (Figure 8). By constantly measuring the eye width and adjusting the system settings when performance drops, the optional eye-width monitor circuitry provides an additional level of reliability to the SERDES link.

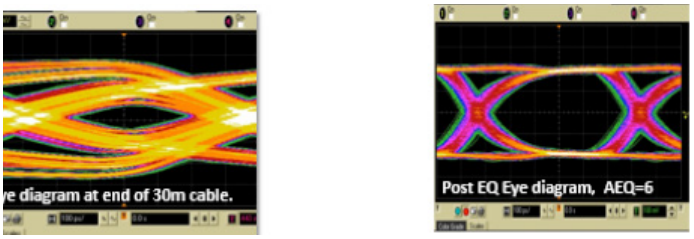

Figure 8. Contrast Between Closed (left) and Open (right) Eye Diagrams

8b/10b Encoding

Understanding 8b/10b encoding is an important prerequisite before determining parameters like pixel clock rate and data bus width in a camera application. Maxim GMSL technology utilizes encoding schemes to enhance the quality of its serial links.

8b/10b encoding uses an algorithm to encode data for a transmission line in which each 8-bit data byte is converted into a 10-bit symbol. An 8b/10b encoded data stream has an equal number of 1s and 0s, and limits the number of consecutive 1s or 0s to 5 bits (Table 2).

Table 2. 8b/10b Encoding Format Examples

Value (Decimal)	Value (Binary)	10-Bit Code	Alternate Code
	HGF EDCBA	abcdei fghj	abcdei fghj
0	000 00000	1000111 0100	011000 1011
1	000 00001	011011 0100	100010 1011
2	000 00010	101101 0100	010010 1011
3	000 00011	110001 1011	110001 0100
4	000 00100	110101 0100	001010 1011
5	000 00101	101001 1011	101001 0100
6	000 00110	011001 1011	011001 0100
7	000 00111	111000 1011	000111 0100
8	000 01000	1110001 0100	000110 1011
9	000 01001	100101 1011	100101 0100
10	000 01010	010101 1011	010101 0100
"	"	"	"

If a transmission line is not DC-balanced, a voltage can accumulate over time on the line, which leads to bit errors. For example, when consecutive 1s are transmitted, the AC-coupling capacitors in a SERDES link develop a DC voltage that appears incorrectly as a '0' at the receiver. 8b/10b encoding tracks the running disparity (RD) of 1s and 0s and ensures that the next generated symbol keeps the running disparity within ±1. Over a long period, the number of 1s and 0s transmitted is split 50-50.

Since the transmission clock is embedded in a SERDES data stream, it must be extracted from the data at the receiver. To do this, the receiver monitors the transitions that occur in the data. Long patterns of 1s or 0s disrupt the ability of the receiver to recover the clock signal. 8b/10b encoding avoids this by limiting the number of consecutive 1s or 0s.

Calculating the Pixel Clock Rate

An image sensor typically outputs information from one pixel for every pixel clock cycle. Thus, the pixel clock for a given camera application is calculated from the image size and number of images displayed every second:

Pixel rows x Pixel columns x frame rate = Pixel Clock (Hz)

When communicating from serializer to deserializer, Maxim GMSL devices internally use data widths of 24, 27, or 32 bits. The use of 8b/10b (and 9b/10b) encoding translates these data widths into 30- or 40-bit packets that are sent across the link. This packet encoding happens automatically and internally, but the user should keep this packet structure in mind when deciding how to choose a pixel clock rate and allocate the parallel data to be sent across the link.

The MAX967xx product family features a maximum serial data rate of 1.74Gbps. Since data is sent in 30- or 40-bit packets, this translates to a maximum packet update rate of 58MHz or 43.5MHz, respectively. Three hardware configuration pins set the allowable pixel clock range that can be applied to a MAX967xx serializer: BWS, DBL, and HIBW (Table 3).

Table 3. PCLK Range for Various Packet Settings

DBL	BWS	HIBW	PCLK Range (MHz)
1	1	0	25 to 87
1	0	0	33.3 to 116
1	0	1	73.3 to 116
0	1	0	12.5 to 43.5
0	0	0	16.7 to 58
0	0	1	36.6 to 58

BWS determines the internal bus width, which is 32 bits when BWS = 1 or 24/27 bits when BWS = 0. BWS is directly related to whether encoded serial packets are 30 or 40 bits wide, which imposes a maximum clock range of 58MHz or 43.5MHz.

DBL controls whether the serializer has single-input mode or double-input mode enabled. Single-input mode serializes one parallel input word into one serial word for transmission, whereas double-input mode combines two parallel input words of half-width into one serial word for transmission. Double-input mode allows for twice the pixel clock to be used, at the expense of the parallel input width.

HIBW enables high-bandwidth mode, and is only active when BWS = 0. HIBW = 1 selects a 27-bit wide internal data bus, and HIBW = 0 selects a 24-bit wide internal data bus.

Selecting Input Data Width

The high flexibility of the MAX967xx SERDES parts allow for a variety of configurations in setting the parallel data width. The calculated pixel clock rate limits the available settings for BWS, DBL, and HIBW. Other settings limit the parallel input mappings available: PXL_CRC, HVEN, and the number of input/output pins (Table 4).

Table 4. MAX967xx Input Data Width Selection

Register Bit Settings					Input Mapping (with MAX96706)	Input Mapping (with Other)
DBL	BWS	HIBW	PXL_CRC	HVEN		
1	1	—	1	1	DIN11:0, HS, VS	DIN11:0, HS, VS
1	1	—	1	0	DIN11:0,	DIN11:0,
1	1	—	0	1	DIN11:0*, HS, VS	DIN13:0*, HS, VS
1	1	—	0	0	DIN13:0*	DIN14:0*
1	0	1	1	—	DIN8.0, HS, VS	DIN8.0, HS, VS
1	0	1	0	—	DIN11:0, HS, VS	DIN11:0, HS, VS
1	0	0	1	1	DIN7:0, HS, VS	DIN7:0, HS, VS
1	0	0	1	0	DIN7:0	DIN7:0
1	0	0	0	1	DIN10:0, HS, VS	DIN10:0, HS, VS
1	0	0	0	0	DIN10:0	DIN10:0
0	1	—	1	1	DIN11:0*, HS, VS	DIN13:0*, HS, VS
0	1	—	1	0	DIN13:0*	DIN15:0*
0	1	—	0	1	DIN11:0*, HS, VS	DIN13:0*, HS, VS
0	1	—	0	0	DIN13:0*	DIN15:0*
0	0	1	—	—	DIN11:0*, HS, VS	DIN13:0*, HS, VS
0	0	0	1	1	DIN11:0*, HS, VS	DIN13:0*, HS, VS
0	0	0	1	0	DIN13:0*	DIN15:0*
0	0	0	0	1	DIN11:0*, HS, VS	DIN13:0*, HS, VS
0	0	0	0	0	DIN13:0*	DIN15:0*

* The input bit width is limited by the number of available serializer inputs and deserializer outputs.

PXL_CRC enables additional error checking on each serial packet sent across the link. If enabled, this feature takes an additional 6 bits of internal bus width.

HVEN enables the HSYNC and VSYNC inputs to be encoded and sent in separate transmissions from the internal data bus, which frees additional slots for parallel input data. This feature is useful when there are more input data pins than slots available in the internal data bus. If disabled, any HSYNC/VSYNC signal must be applied to an input slot.

I/O Pin Count can be a limiting factor to the input data width. If single-input mode is enabled, or if the pixel CRC feature is disabled, there may be many internal data bus slots available. If there are more bits available than parallel inputs or parallel outputs, these slots in the packet go unused and bandwidth is lost.

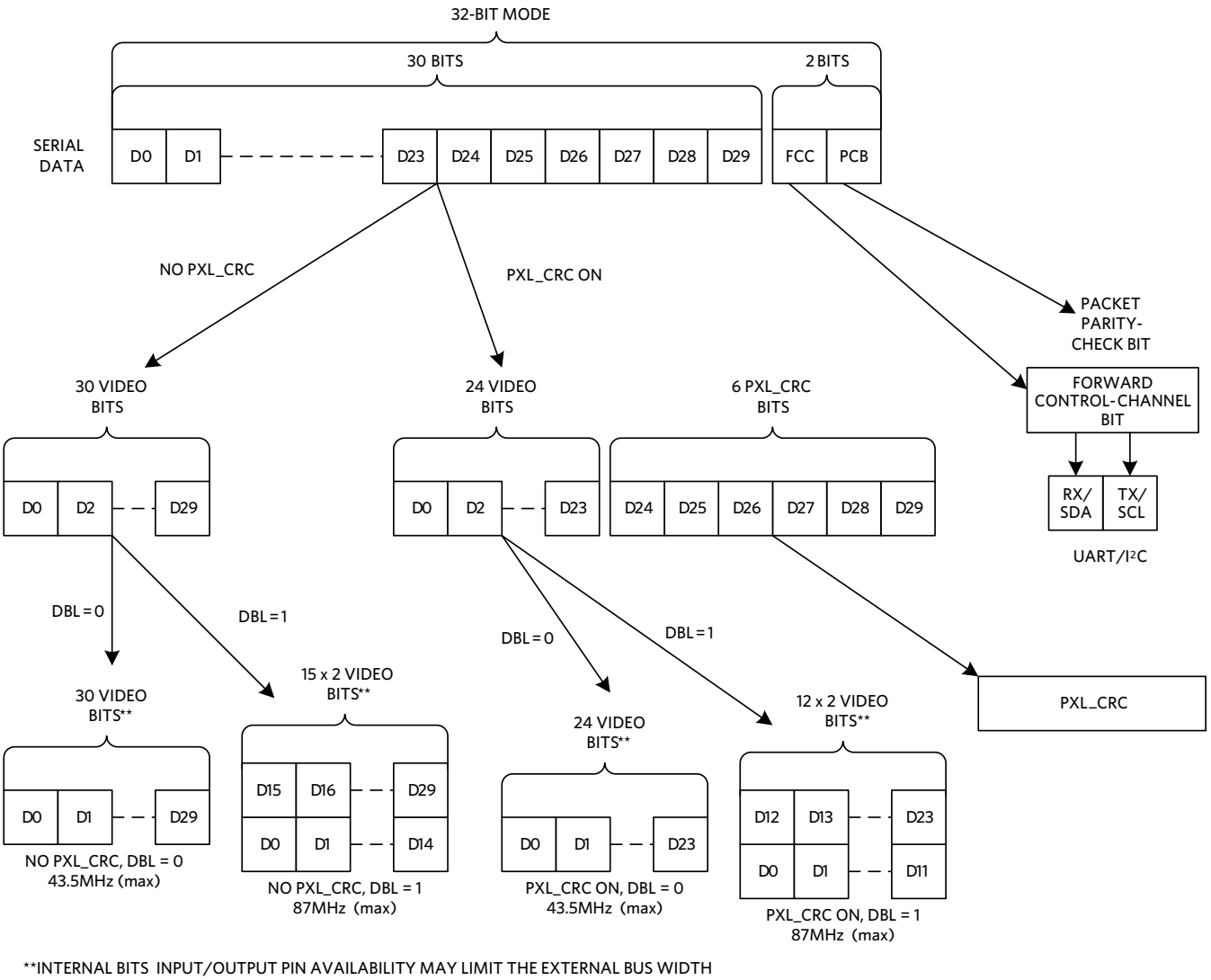

Figure 9. 32-Bit Data Packet Breakdown

In an example using the **MAX96705**/**MAX96706** pair (Figure 9), if BWS (bus width select) = 1, the internal data width is set to 32 bits (40 bits after 8b/10b encoding). Two bits are set aside for control channel and parity information, and the remaining 30 bits can be used for video data. If PXL_CRC is enabled for further error detection, 6 additional bits are taken and the remaining 24 bits are used for video data. If DBL (double-input mode) = 1, the 24 bits are allocated to two 12-bit input words. Since both chips have at least 14 parallel data pins, this configuration works without limitation. If DBL = 0, the 24 bits are allocated to one input word, and the total throughput is limited by the number of parallel data pins on the MAX96705/MAX96706. Since the MAX96706 only has 14 parallel outputs, the parallel data can only appear on 14 parallel inputs (DIN13:0) without dropping information. The other 10 slots in the internal data bus are unused.

Related Resources

Advanced Driver Assistance Systems (ADAS)

Automotive Products, Applications & Solutions

Power Management for ADAS

SERDES Portfolio: ADAS Applications

Serializer Product Selector Guide

Part No.	Inputs	Interface	Speed (Mbps)	Size (mm²)	HDCP	Application
MAX96707	14	CMOS/LVCMOS	1740	16.8		1.74Gbps Compact Cameras
MAX96709	14	CMOS/LVCMOS	1740	16.8		
MAX96705	16	CMOS/LVCMOS	1740	26		
MAX96711	14	CMOS/LVCMOS	1740	26		
MAX9271	16	CMOS/LVCMOS	1500	26		1.5Gbps Camera/Display
MAX9273	22	CMOS/LVCMOS	1500	37.2		
MAX9249	4	LVDS	2500	50.4		2.5Gbps Camera/Display
MAX9259	30	CML	2500	65.6		
MAX9293	—	HDMI	3120	65.6	YES	3.12Gbps Display
MAX9277	4	LVDS	2800	50.4		
MAX9281	4	LVDS	2800	50.4	YES	
MAX9275	30	LVCMOS	2800	65.6		
MAX9279	30	LVCMOS	2800	65.6		
MAX9291	—	HDMI	3120	65.6		

Deserializer Product Selector Guide

Part No.	Inputs	Interface	Speed (Mbps)	Size (mm²)	HDCP	Application
MAX96706	14	CMOS/LVCMOS	1740	26		1.74Gbps Compact Cameras
MAX96708	14	CMOS/LVCMOS	1740	26		
MAX9272A	28	CMOS/LVCMOS	1500	50.4		1.5Gbps Camera/Display
MAX9264	30	CMOS/LVCMOS	2500	65.6	YES	2.5Gbps Camera/Display
MAX9268	4	LVDS	2500	50.4		
MAX9260	30	CMOS/LVCMOS	2500	65.6		
MAX9278A	4	LVDS	3120	50.4		3.12Gbps Display
MAX9282A	4	LVDS	3120	50.4	YES	
MAX9276A	32	CMOS/LVCMOS	3120	65.6		
MAX9280A	32	CMOS/LVCMOS	3120	65.6	YES	
MAX9288	4	CSI-2	3120	50.4		
MAX9278	4	LVDS	3120	50.4		
MAX9286	4	CSI-2	1500	65.6		Quad SER Input for Cameras

Learn more

For more information, visit:
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