Application Report
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High-Speed Layout Guidelines

Alexander Weiler, Alexander Pakosta, and Ankur Verma *Clock Drivers*

ABSTRACT

This application report addresses high-speed signals, such as clock signals and their routing, and gives designers a review of the important coherences. With some simple rules, electromagnetic interference problems can be minimized without using complicated formulas and expensive simulation tools. Section 1 gives a short introduction to theory, while Section 2 focuses on practical PCB design rules. Either section can be read independently.

Contents

Trademarks

1 Theoretical Overview

Some basic understanding is desirable to effectively use the PCB design rules given in this document. It is then easy to identify the undesirable effects that can arise and how to avoid them. The reason PCB layout becomes more and more important is because of the trend to faster, higher integrated, smaller form factors, and lower power electronic circuits. The higher the switching frequencies are, the more radiation occurs on a PCB. With good layout, many EMI problems can be minimized to meet the required specifications.

1.1 Electromagnetic Interference and Electromagnetic Compatibility

Electromagnetic interference (EMI) is radio frequency energy that interferes with the operation of an electronic device. This radio frequency energy can be produced by the device itself or by other devices nearby.

Electromagnetic compatibility (EMC) is the ability of an electronic product to operate without causing EMI that would interfere with other equipment and without being affected by EMI from other equipment or the environment.

The goal is to reduce EMI to meet the requirements given by the Federal Communication Commission (FCC) or the International Special Committee on Radio Interference (CISPR)

A basic EMI model is shown in Figure 1. Every device acts as a source and simultaneously as a sink. It can cause interference through a coupling path and can be affected by interference through the coupling path. The coupling can be:

- Capacitive
- Inductive
- Galvanic
- Radiated power

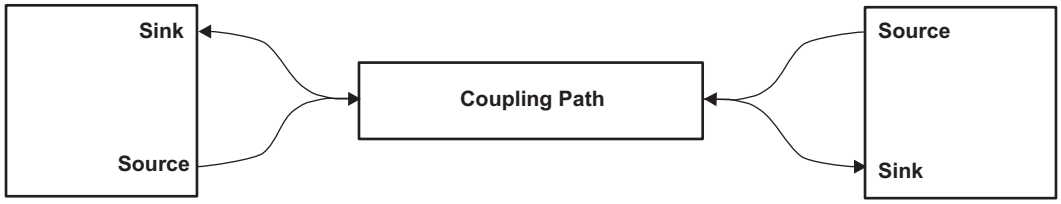

Figure 1. Model of Electromagnetic Interference

There is not just one coupling mechanism present, but rather a combination of them. With proper PCB layout, however, these effects can be reduced.

1.2 Clock Signals

Figure 2 illustrates the time and the frequency domain of a clock signal. Ideally, it is a square wave., but in reality, it is not possible to change from low level to high level (and vice versa) in an infinite short time. Due to the rise and fall time, it has the shape of a trapezoid in the time domain. By means of the Fourier series, the trapezoid consists of a series of sine and cosine signals with different frequency and magnitude. The discrete frequency components have an envelope as is shown in the lower diagram of Figure 2. An important aspect is that in the frequency domain the amplitude of the higher frequency harmonics depends on the rise and fall time of the signal. The longer the rise time, the smaller the magnitude of the harmonics. For example, the harmonics of a 100-MHz clock signal are not negligible, especially the third and fifth. In this case, consideration also should be made with frequencies up to 500 MHz. With the CDCE906 from Texas Instruments, the user can set different rise and fall times to reduce the amplitude of the harmonics. However, take care to ensure these times do not violate the slew rate specifications of the driven devices.

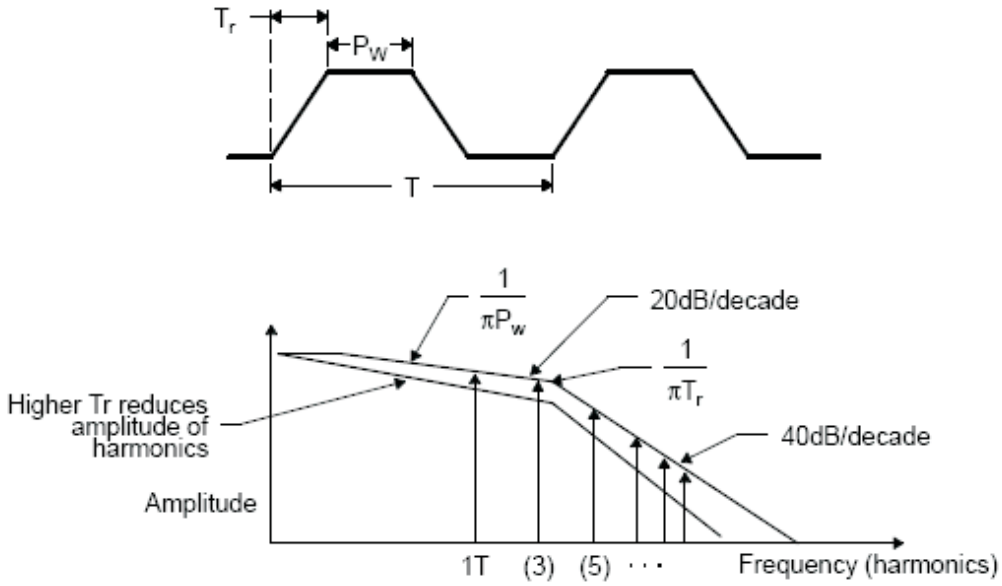

Figure 2. Time Domain and Frequency Domain of a Clock Signal

1.3 Transmission Lines

If the lengths of traces are in the range of the signal's wavelength, then the user has to consider the effects of transmission lines. The problems that a user must deal with are time delay, reflections, and crosstalk. To get a better understanding of these problems and where and how they arise, it is useful to know what transmission lines are. They are simply the traces on a PCB and depend on the length and the frequency of the signals passing through them.

Many different structures of trace routing are possible on a PCB. Two common structures are shown in Figure 3. On the left, a microstrip structure is illustrated, and on the right, a stripline technique. A microstrip has one reference, often a ground plane, and these are separated by a dielectric. A stripline has two references, often multiple ground planes, and are surrounded with the dielectric.

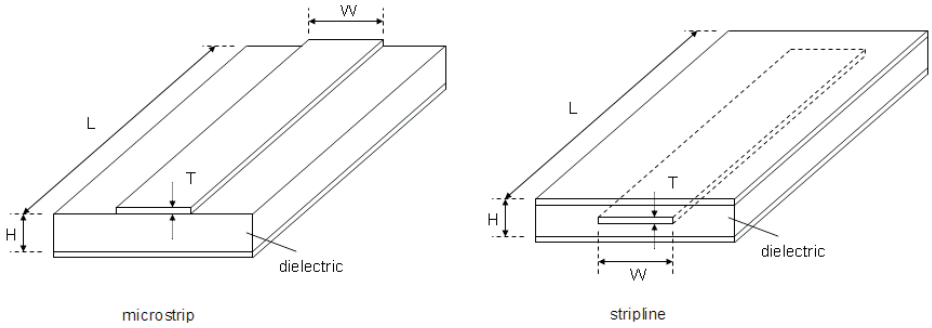

Figure 3. Structure and Dimension of Microstrip and Stripline

The following sections describe some important properties of transmission lines which are significant for PCB design. Many software tools are available to calculate the properties of the several transmission line structures. In this application report, the freeware AppCAD from Agilent is used so that the reader can become familiar with these properties. Figure 4 shows the two structures, microstrip (top) and stripline (bottom). The dimensions, the material, and the frequency are in each case shown on the left. The results that are used in the following sections can be seen on the right. Table 1 defines the symbols used in Figure 3 and Figure 4.

Table 1. Description of the Symbols Used in Figures 3 and 4

SYMBOL	DESCRIPTION
H	Height of the dielectric
W	Width of the trace
L	Length of the trace
Frequency	The frequency on which the calculations are based
Z_0	Characteristic impedance of the trace
1.0 Wavelength	Wavelength λ of the trace at the given frequency and the given effective dielectric $\lambda = \frac{3 \times 10_8 \text{ m/s}}{\sqrt{\epsilon_{\text{eff}}} \times f}$
V_P	Velocity of the signal on this trace with the given dimensions and frequency relative to the speed of light. The absolute velocity is calculated by $V_{P,.\text{absolute}} = V_{P,.\text{relative}} \times 3 \times 10^8$ m/s
ε_{eff}	Combination of the several dielectrics which surrounds the microstrip
W/H	Ratio between trace width and trace length

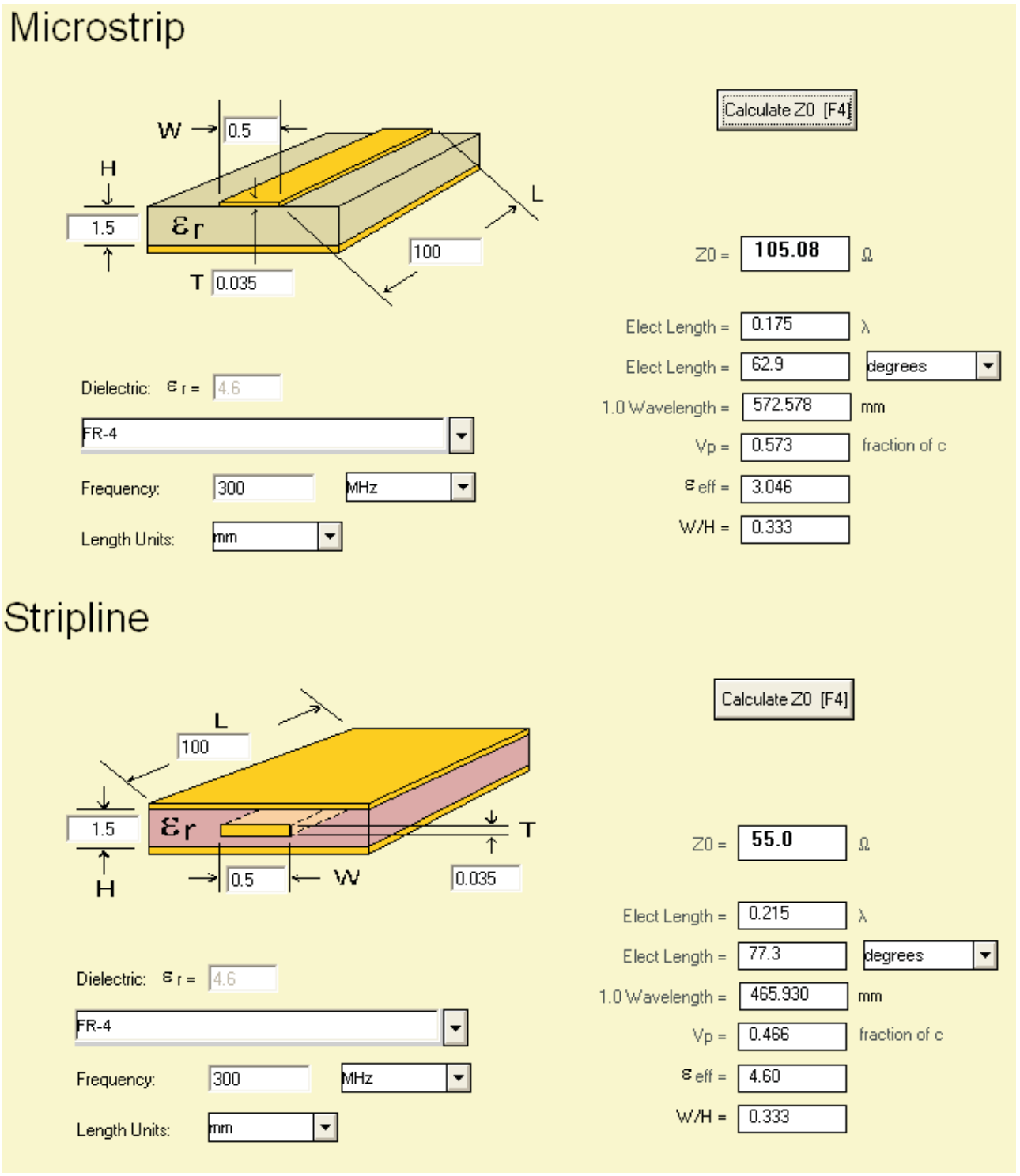

Figure 4. Calculation of Properties of Microstrip and Stripline (AppCAD)

1.3.1 Signal Speed and Propagation Delay Time

A signal cannot pass through a trace with infinite speed. The maximum speed is the speed of light with 3×10^8 m/s. For a certain trace length, the signal needs a certain time to pass it, and this is called the propagation delay time. The standard medium for the speed of light is air. For another medium, the dielectric in a PCB environment, the speed is different than that of the speed of light in air. The formula for the speed on a stripline is:

$$V = \frac{3 \times 10^8 \text{ m/s}}{\sqrt{\epsilon_r}} \quad (1)$$

So, the speed is a function of the dielectric which surrounds the trace. For a microstrip, it is more complicated because the trace is not surrounded by one dielectric. There are at least two: the substrate under the trace and the air above the trace. If the PCB contains a solder mask, a third medium would be present. Therefore, the calculation of an effective ε_r is necessary before determining the signal speed. It depends on the width of the microstrip and the distance to the reference plane. In this case, the speed is a function of the present dielectric, the trace width, and its distance to the reference plane [12].

The signal speed and the propagation delay time, respectively, on a signal trace are important when:

- Timing and skew requirements must be met (clock distribution, buses, and so forth)
- Differential traces were used (for example, LVDS)

1.3.1.1 Examples

The following parameters are the same in each case:

length = 100 mm; thickness = 35 μm; height = 1.5 mm; ε_r = 4.6 (FR4); frequency = 300 MHz

In Table 2, the dependency of signal speed on the trace width at the microstrip structure is shown. Using a stripline, the signal speed is not a function of the trace width. The same is valid for the height.

Table 2. Comparison of Propagation Delay Time

	WIDTH [mm]	$\varepsilon_{r,eff}$	$V_{P,relative}$	$V_{P,absolute}$ [mm/ns]	P_d [(1)] [ps/100 mm]
Microstrip 1	0.5	3.046	0.573	171.9	581.7
Microstrip 2	1	3.165	0.562	168.6	593.1
Stripline 1	0.5	4.6	0.466	139.8	715.3
Stripline 2	1	4.6	0.466	139.8	715.3

(1) P_d is the propagation delay time in ps on the mentioned line with A 100-mm length.
$P_d = \frac{1}{171.9 \text{ mm/ns}} \times 100 \text{ mm}$

1.3.2 Characteristic Impedance, Reflections, and Termination

Another property of a transmission line is the characteristic impedance, Z_0. The microstrip in Figure 4 has for the given attributes a characteristic impedance Z_0 = 105 Ω, and the stripline Z_0 = 55 Ω. If there are any impedance changes in the signal chain (source – trace – vias – connectors – sink, and so forth), reflections occur. These reflections cause over- and undershoots. The two extreme are a transmission line with an open end (R = ∞) and a shorted end (R = 0 Ω). The reflection coefficient ρ is the dimension which expresses the relationship between the impedance of the transmission line and the impedance of the source or sink. It is calculated as $\rho = \frac{R - Z_0}{R + Z_0}$. For the two mentioned cases, the reflection coefficient becomes ρ = +1 for an open end and ρ = –1 for a shorted end. The value 1 means that the complete signal reflects at this impedance change and goes back to the source. To avoid this, the reflection coefficient must be ρ = 0 to get no reflections. This is the case if the impedance at the source has the same value as the characteristic impedance of the transmission line.

In Figure 5, the case with an open end (high-impedance input stage of the sink) is simulated. The clock source has an output of 3.3 V and an impedance of 25 Ω. The red line (dotted) is the ideal shape of the clock output. The green one (dashed) is the real signal at the clock's output and the blue line is at the end of the transmission line. The reflection is the cause of these over- and undershoots. The maximum voltage at the trace end is approximately 4.4 V instead of 3.3 V, and the minimum voltage is approximately –1 V instead of 0 V. These circumstances can damage the input stage of the source and sink.

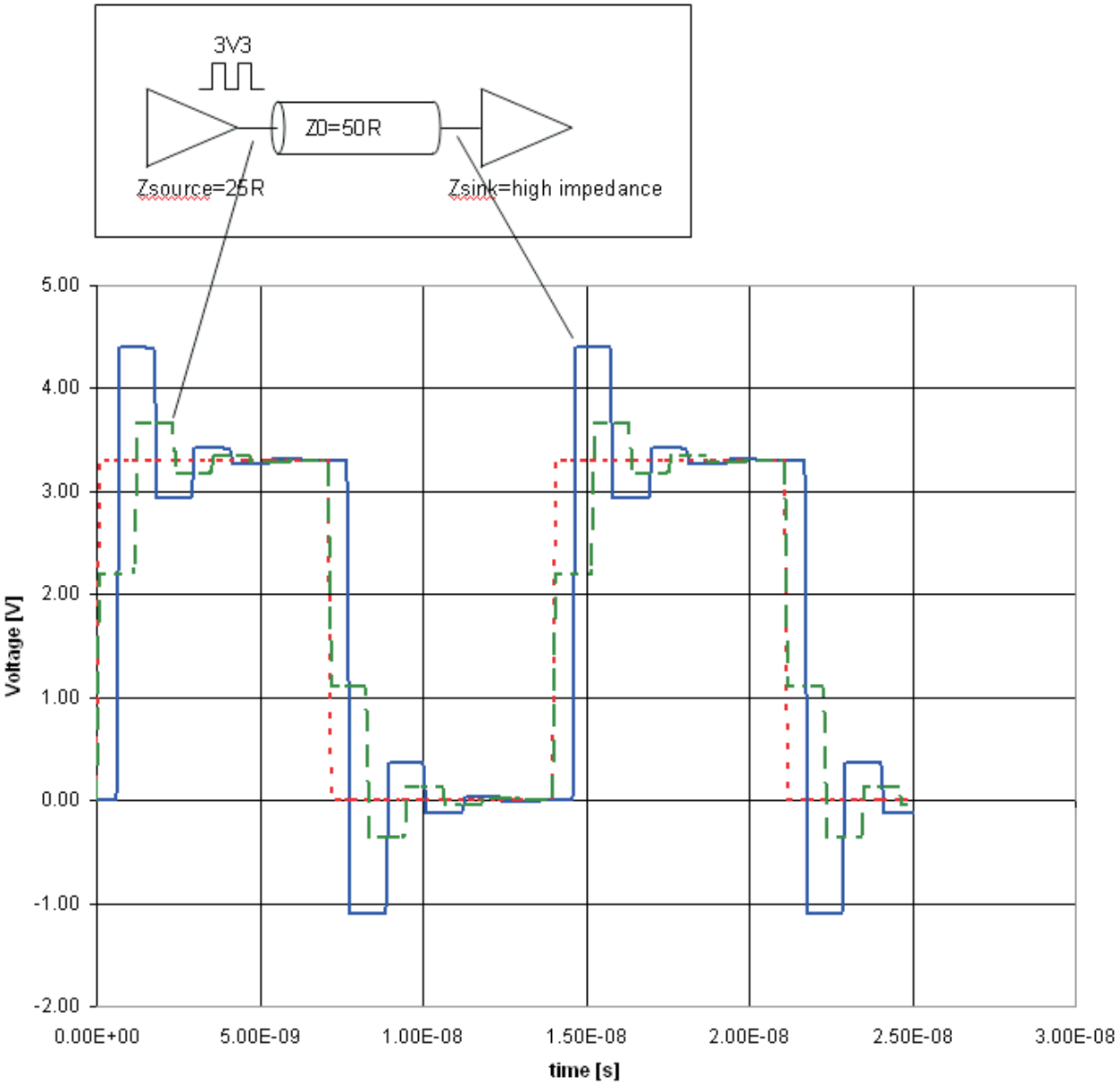

Figure 5. Over- and Undershoots Due to Incorrect Termination

A receiver often has a high-impedance input. To avoid these over- and undershoots, the reflections must be reduced. Therefore, a proper termination is required. The most common termination techniques follow:

- Series termination
- Parallel termination
- Thevenin termination
- AC termination

Each of them has advantages and disadvantages, and the designer has to trade off which one is the best solution for his design.

References: [8], [9]

1.4 Crosstalk

The mutual influence of two parallel, nearby routed traces is called crosstalk. One is called the aggressor (this trace carries the signal) and the other is called the victim (this trace is influenced by the aggressor). Due to the electromagnetic field, the victim is influenced by an inductive and a capacitive coupling. They generate a forward and a backward current in the victim trace whereas in a homogenous environment (for example, stripline) the two induced currents cancel each other. In a microstrip environment, the forward current of the inductive coupling tends to be larger than the influence of the capacitive coupling. To minimize the effects on crosstalk on adjacent traces, keep them at least 2 times the trace width apart.

Transmission lines coupled through a media have crosstalk associated with them. There are two types of crosstalk: forward crosstalk and backward crosstalk. Forward crosstalk travels in same direction as the aggressor. It grows with length and increasing aggressor dV/dt, whereas the backward crosstalk travels in the opposite direction as the aggressor and depends only on the aggressor amplitude. Make sure to measure the crosstalk between channels v/s frequency. IEEE802.3KR specifies Insertion Loss Crosstalk Ratio (ICR) that sums the crosstalk and plot it using S_{21}.

References: [1], [2], [3], [4], [5]

1.5 Differential Signals

In the case of differential signals, the negative effect of crosstalk is a positive one. The signals on each trace are in theory exactly equal in magnitude and opposite in their sign. So, their electromagnetic fields cancel each other and the return current on the ground plane, as well. To achieve this, the traces for both signals must have the same length so that the propagation delay times are equal. The receiver is sensitive to the differences of the signals and not to an absolutely level reference, for example, to ground. If any signal radiated equally into both differential traces, the receiver would not recognize it. Therefore, the designer has to make sure that radiation affects both traces equally. This can be realized by routing the differential traces as close as possible.

References: [1], [6], [7]

1.6 Return Current and Loop Areas

An electrical circuit must always be a closed loop. Up to now, only the signal path was discussed but not the path back to the source – the return current. With DC, the return current takes the way back with the lowest resistance (Figure 6a). With a higher frequency, the return current flows along the lowest impedance (Figure 6b). This is directly beside the signal.

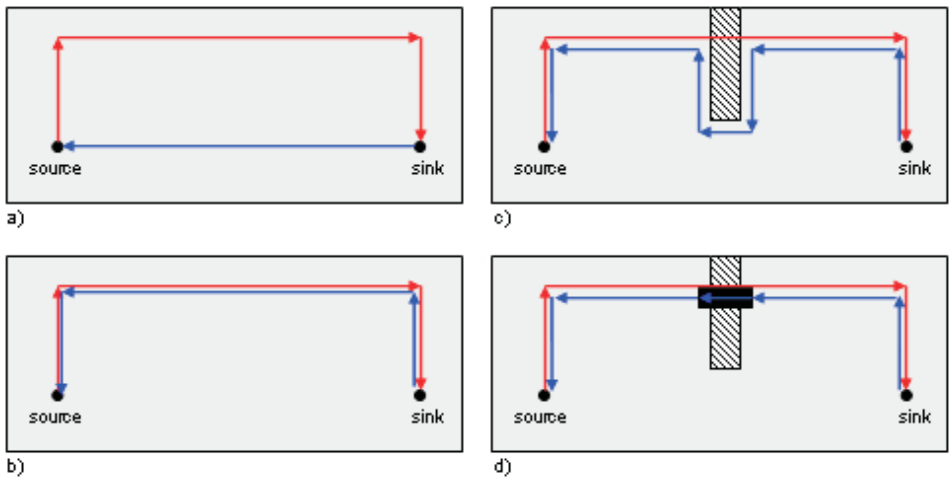

Figure 6. Return Current and Resulting Loop Area

If this return path, mostly the ground plane, has a slot, the return current has to take another way and this results in a loop area (Figure 6c). The larger the area, the more radiation and EMI problems occur. The designer has to make sure that the return current can flow directly underneath the signal trace. One solution is to place a 0-Ω resistor over the slot (Figure 6d). Another is to route the signal the same way as the return current flows. The best solution is to avoid any slots in the ground reference plane.

2 Practical PCB Design Rules

Because many things can affect transmission lines, EMI problems can occur. To reduce these problems, good PCB design is important, and with some simple design rules, the PCB designer can minimize these problems. It is important to make prudent decisions during new circuit design, like the minimum number of layers. The easiest way to get a good, new design is to copy the recommended design from the TI evaluation modules (EVM).

A good PCB layout starts with the circuit design. Do not postpone considerations about the layout. One of the most important aspects affecting the layout is the location of each functional block. Keep their devices and their traces together.

2.1 PCB Considerations During the Circuit Design

- What is the highest frequency and fastest rise time in the system?
- What are the electrical specifications at the inputs and outputs of the sinks and sources?
- Are there sensitive signals to route – for example, think about controlled impedance, termination, propagation delay on a trace (clock distribution, buses, etc.)?
- Is a microstrip adequate for the sensitive signals, or is it essential to use stripline technique?
- How many different supply voltages exist? Does each supply voltage need its own power plane, or is it possible to split them?
- Create a diagram with the functional groups of the system – for example, transmitter path, receiver path, analog signals, digital signals, and so forth
- Are there any interconnections between at least two independent functional groups? Take special care of them. Think about the return current and crosstalk to other traces.
- Clarify the minimum width, separation and height of a trace with the PCB manufacturer. What's the minimum distance between two layers? What about the minimum drill and the requirements of vias? Is it possible to use blind vias and buried vias?

Equipped with this information, a designer can do a lot of basic design.

2.2 Board Stackup

There is no fundamental information about how many layers should be used and how the board stackup should look. Again, the easiest way the get good results is to use the design from the EVMs of Texas Instruments. The magazine *Elektronik Praxis* [11] has published an article with an analysis of different board stackups. These are listed in Table 3 and Table 4.

Generally, the use of microstrip traces needs at least two layers, whereas one of them must be a GND plane. Better is the use of a four-layer PCB, with a GND and a VCC plane and two signal layers. If the circuit is complex and signals must be routed as stripline, because of propagation delay and/or characteristic impedance, a six-layer stackup should be used.

Table 3. Possible Board Stackup on a Four-Layer PCB

	Model 1	Model 2	Model 3	Model 4
Layer 1	SIG	SIG	SIG	GND
Layer 2	SIG	GND	GND	SIG
Layer 3	VCC	VCC	SIG	VCC
Layer 4	GND	SIG	VCC	SIG
Decoupling	Good	Good	Bad	Bad
EMC	Bad	Bad	Bad	Bad

Table 3. Possible Board Stackup on a Four-Layer PCB (continued)

	Model 1	Model 2	Model 3	Model 4
Signal integrity	Bad	Bad	Good	Bad
Self disturbance	Satisfaction	Satisfaction	Satisfaction	High

Table 4. Possible Board Stackup on a Six-Layer PCB

	Model 1	Model 2	Model 3	Model 4	Model 5	Model 6
Layer 1	SIG	SIG	GND	SIG	SIG	SIG
Layer 2	SIG	GND	VCC	GND	GND	GND
Layer 3	VCC	VCC	SIG	VCC	VCC	VCC
Layer 4	GND	VCC	SIG	SIG	GND	GND
Layer 5	SIG	GND	VCC	GND	Not used	SIG
Layer 6	SIG	SIG	GND	SIG	SIG	SIG
Decoupling	Good	Good	Good	Good	Good	Good
EMC	Bad	Good	Satisfaction	Satisfaction	Good	Good
Signal integrity	Bad	Good	Bad	Good	Good	Bad

To determine the right board stackup, consider the following points:

- Define the location of each section on the board by means of the functional diagram. Try to keep the devices together to avoid interaction (crosstalk, influence of noise) between two separate blocks (like transmitter–receiver or analog–digital).
- At which functional block is which supply voltage used?
- It is necessary in high-speed designs to have at least one complete ground plane as a reference for microstrip traces for sensitive signals.
- With a complete power plane as close as possible to the ground plane, it is possible to create capacitive coupling between them to get low impedance at high frequencies. This reduces the amount on small decoupling capacitors at the power pins of the devices. The closer the planes, the less impedance is present [13].

2.3 Power and Ground Planes

As previously mentioned, a complete ground plane in high-speed design is essential. Additionally, a complete power plane is recommended as well. In a complex system, several regulated voltages can be present. The best solution is for every voltage to have its own layer and its own ground plane. But this would result in a huge number of layers just for ground and supply voltages. What are the alternatives? Split the ground planes and the power planes? In a mixed-signal design, for example, using data converters, the manufacturer often recommends splitting the analog ground and the digital ground to avoid noise coupling between the digital part and the sensitive analog part.

Take care when using split ground planes because:

- Split ground planes act as slot antennas and radiate.
- A routed trace over a gap creates large loop areas, because the return current cannot flow beside the signal, and the signal can induce noise into the nonrelated reference plane (Figure 7).
- With a proper signal routing, crosstalk also can arise in the return current path due to discontinuities in the ground plane. Always take care of the return current (Figure 10).

Figure 7: Do not route a signal referenced to digital ground over analog ground and vice versa. The return current cannot take the direct way along the signal trace and so a loop area occurs. Furthermore, the signal induces noise, due to crosstalk (dotted red line) into the analog ground plane.

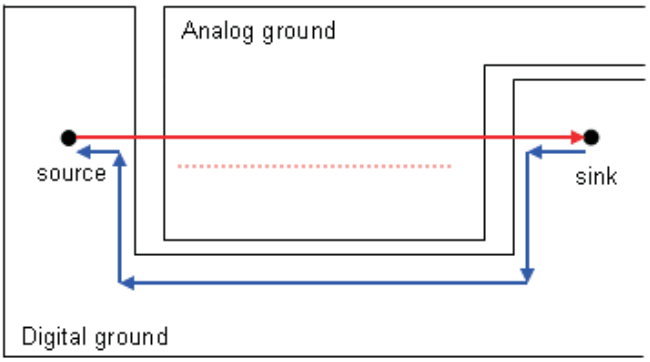

Figure 7. Loop Area and Crosstalk Due to Poor Signal Routing and Ground Splitting

Figure 8: Do not let one ground plane pass another ground plane to get connected to the common ground (a). Every ground plane must have its own path to the common ground to reduce noise (b).

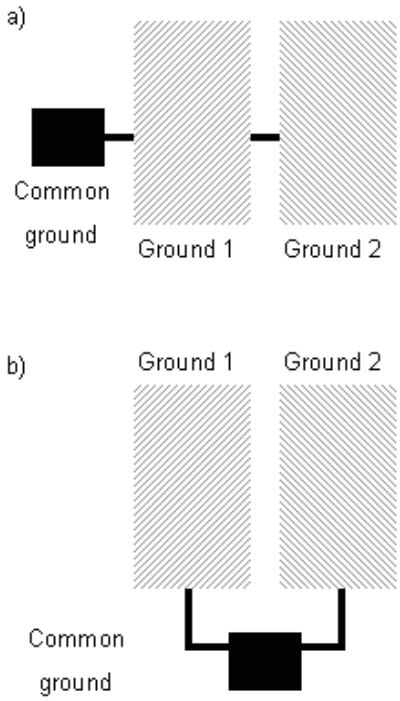

Figure 8. Poor and Good Placement of the Common Ground in a Split Ground Environment

Figure 9: The use of a complete ground plane is a better solution. Place the devices by function and route their signals only in their region. If any interconnection between analog and digital occurs, be careful with crosstalk and the return current path.

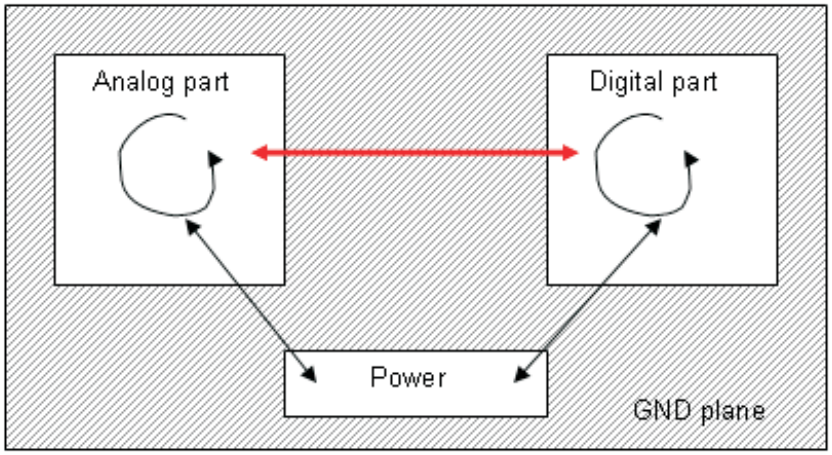

Figure 9. Good Placement of Different Functional Blocks Without the Need of a Split Ground Plane

Figure 10: If the trace routing of two signals is done properly, it is still possible to induce noise in the return current path by means of crosstalk. In this case, a loop area and crosstalk in the return current path have been created.

- If possible, use a continuous ground plane; do not split them. This can be achieved by a proper placement selection. Again, create functional blocks, and place and route them together. By doing this, the traces of a digital part cannot influence any trace of the analog part if these sections do not cross each other.

If split ground planes are essential:

- Do not route signals over a gap. Always strive for the return current flow with the smallest loop area.
- Connect split ground planes only at one point. More common ground connections can create ground loops, and this increases radiation.
- The return current of a subsystem (for example, an analog system or transmitter path) must not be in the path of the other subsystem (digital system or receiver path). The return current should flow directly to the common ground point (Figure 8).
- Power planes should only reference their own ground plane. They should not overlap with another ground plane. This leads to capacitive coupling between the power plane and a not-referenced ground plane. Noise can couple into the other system.
- Do not connect bypass capacitors between a power plane and an unrelated ground plane. Again, noise can be coupled from one supply system into the other. This mistake can occur in the circuit design section.

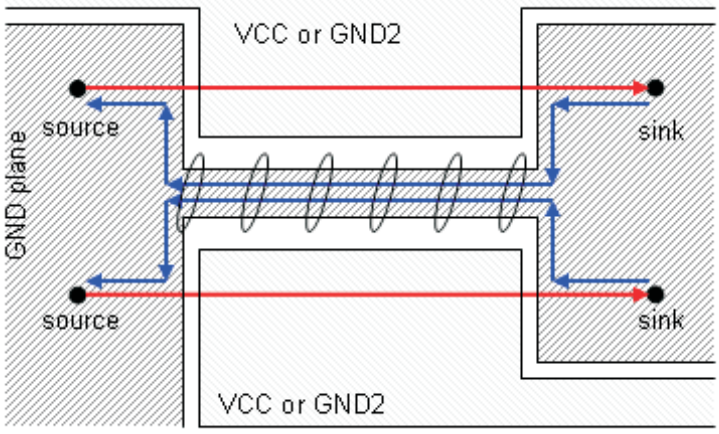

Figure 10. Crosstalk Induced by the Return Current Path

2.4 Decoupling Capacitors

Decoupling capacitors between the power pin and ground pin of the device ensure low AC impedance to reduce noise and to store energy. To reach low impedance over a wide frequency range, several capacitors must be used. This is why, a real capacitor consists of its capacitance and a parasitic inductance and resistance. Therefore, every real capacitor behaves as a resonant circuit. The capacitive characteristics are only valid up to its self-resonant frequency (SRF). Above the SRF, the parasitic effects dominate, and the capacitor acts as an inductor. With the use of several capacitors with different values, low AC impedance over a wide frequency range can be provided.

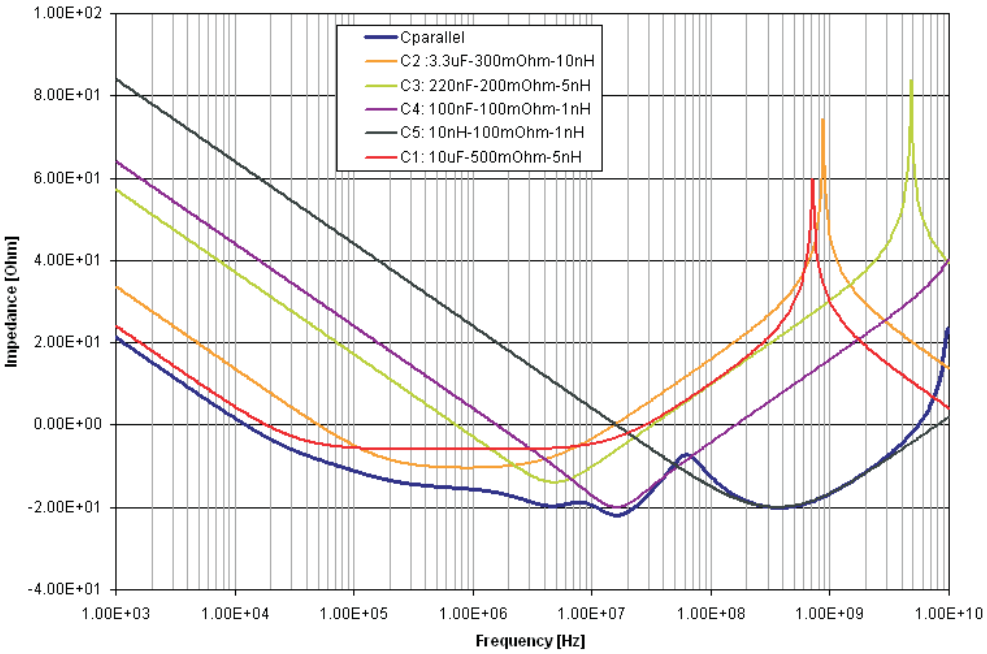

Figure 11. Impedance of Different Capacitors Over a Wide Frequency Range and the Resulting Impedance of Their Parallel Connection

Figure 11 shows this context. Capacitors with high values have low impedance in the lower frequency range and a low SRF, whereas small-valued capacitors have their SRF in the upper frequency range. This depends on the equivalent series resistance (ESR) and the equivalent series inductance (ESL). A good combination of several capacitors leads to a low impedance over a wide frequency range. This is shown with the *Cparallel* curve in Figure 11. The *gap* (increase of the impedance) at around 60 MHz is the result of a missing capacitance. If there were a value between 100 nF and 10 nF, the Cparallel curve would not increase.

As previously mentioned, a power and GND plane can represent a capacitance that ensures low impedance at high frequencies. Therefore, a well-designed board stackup can minimize the number of capacitors required having low-capacitance values.

General rules for placing capacitors:

- Place the lowest valued capacitor as close as possible to the device to minimize the inductive influence of the trace. This is especially important for small capacitor values, because the inductive influence of the trace is not negligible anymore.
- Place the lowest valued capacitor as close as possible to the power pin/power trace of the device.
- Connect the pad of the capacitor directly with a via to the ground plane. Use two or three vias to get a low-impedance connection to ground. If the distance to the ground pin of the device is short enough, you can connect it directly.
- Make sure that the signal must flow along the capacitor.

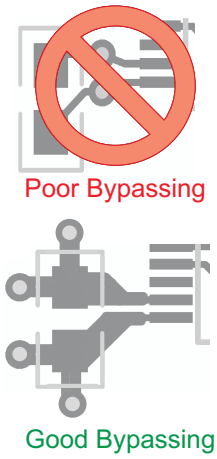

Figure 12. Poor and Good Placement and Routing of Bypass Capacitors

The decoupling or the bypass capacitance must provide the high frequency components of the current. For example for Advanced Driver Assistance Systems (ADAS), the camera current fluctuates between active and blanking periods. Hence, bypass capacitors must take care of the ripple due to non-uniform current within a clock cycle, handle load transients, and filter any noise that could cause the high speed signal to be corrupted. Parallel capacitors are used to give wideband low impedance.

2.5 Traces, Vias, and Other PCB Components

A right angle in a trace can cause more radiation. The capacitance increases in the region of the corner, and the characteristic impedance changes. This impedance change causes reflections.

- Avoid right-angle bends in a trace and try to route them at least with two 45° corners. To minimize any impedance change, the best routing would be a round bend (see Figure 13).
- Separate high-speed signals (for example, clock signals) from low-speed signals and digital from analog signals; again, placement is important.
- To minimize crosstalk not only between two signals on one layer but also between adjacent layers, route them with 90° to each other.

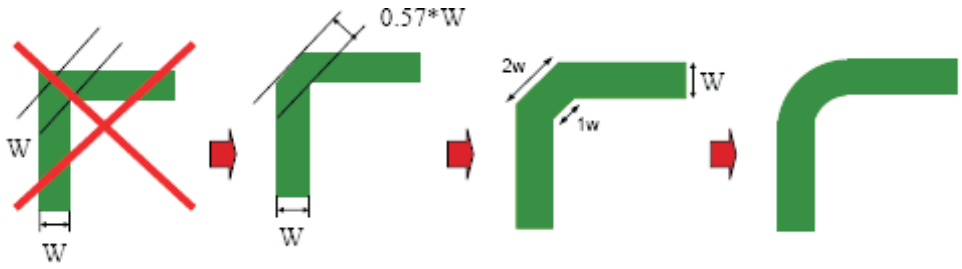

Figure 13. Poor and Good Right Angle Bends

The use of vias is essential in most routings, but the designer has to be careful when using them. They add additional inductance and capacitance, and reflections occur due to the change in the characteristic impedance. Vias also increase the trace length.

- Avoid vias in differential traces. If it is impossible to avoid them, use vias in both traces or compensate the delay also in the other trace.

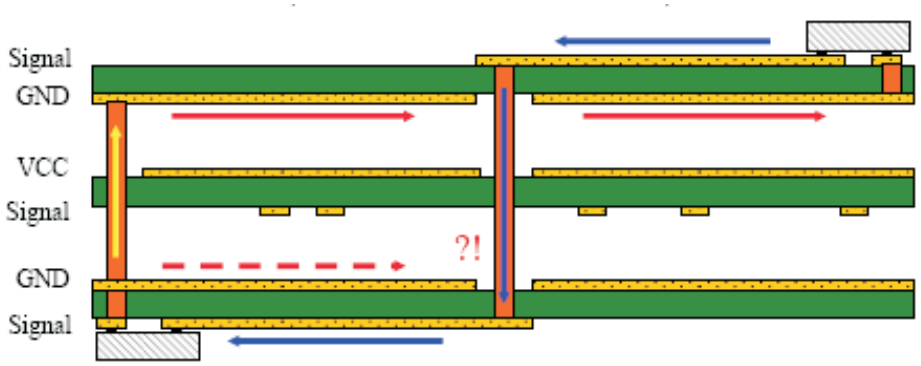

Figure 14. Loop Areas Caused by Poor Via Placement

Figure 14 illustrates another problem with vias – loop areas. The designer has to make sure that the return current can flow ideally underneath (beside) the signal trace. A good way to realize this is to add some ground vias around the signal via. This is a similar structure to a coaxial line. Take care if the new layer has another distance to the reference plane; this can cause reflections due to an impedance change.

Figure 15 shows how good via placement avoids loop areas if there is need for multiple vias.

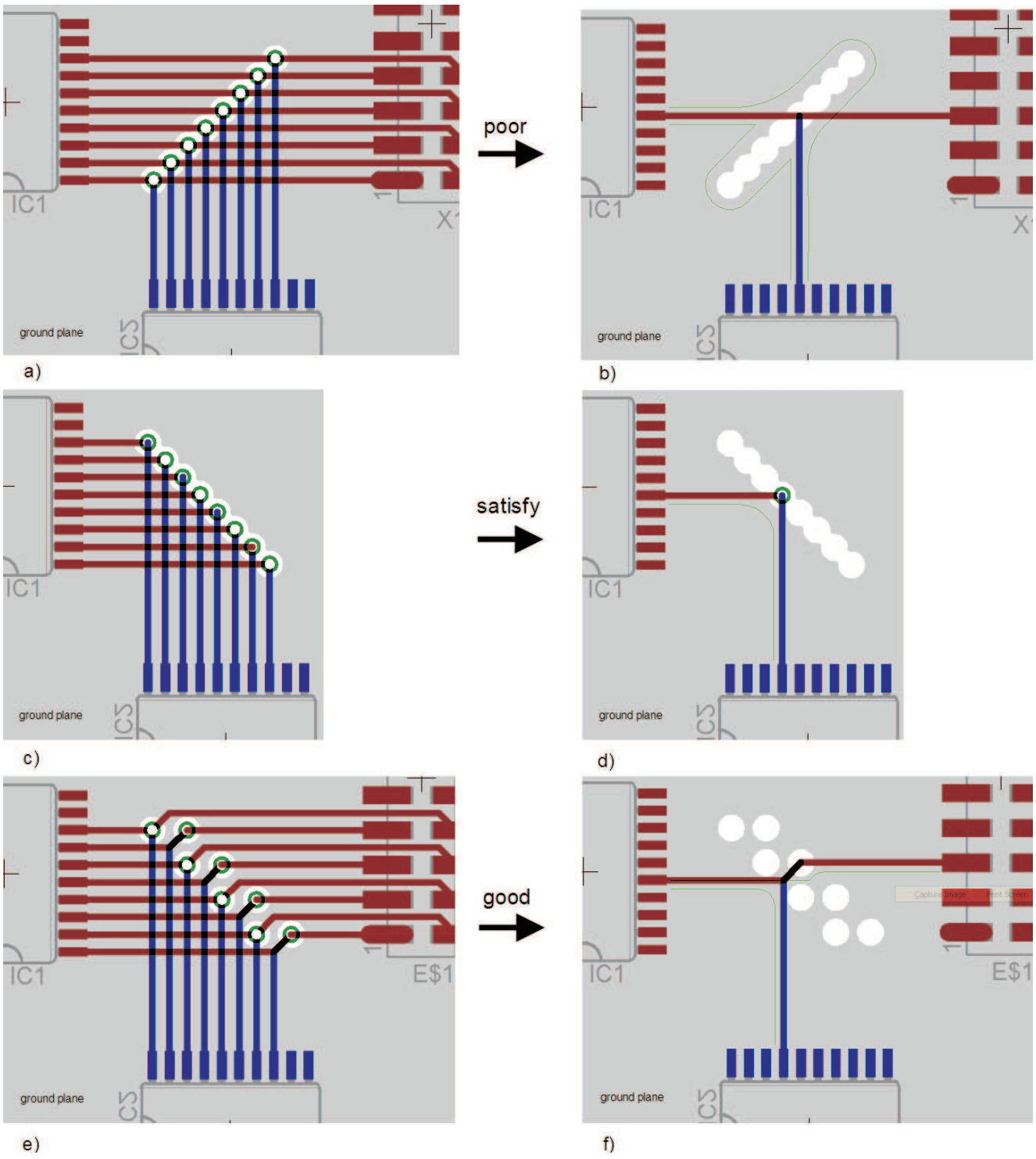

Figure 15. Poor and Good Via Placement

Figure 15: Because of wrong via placement, especially with bus signals, slots in the ground plane can arise. Further, the return current can create a loop area when placing the vias in the wrong direction. Three different routings are shown on the left. On the right, some traces are masked out to see how the return current (green trace) will flow.

In Figure 16, a four-layer stackup can be seen. The signal changes from layer 1 to layer 2. The via passes through all four layers. Thus, we get the structure of an open-end transmission line with no termination and thereby a 100% reflection. Due to the length of the stub, a delay also occurs. The worst case is now that the two signals (original one → red and reflected one → gray) on layer 2 have a phase shift of 180°, and so they cancel each other. The phase shift is due to the delay which arises from the stub length. The time delay is twice the stub length divided by the signal speed. To avoid this problem, use blind vias or buried vias.

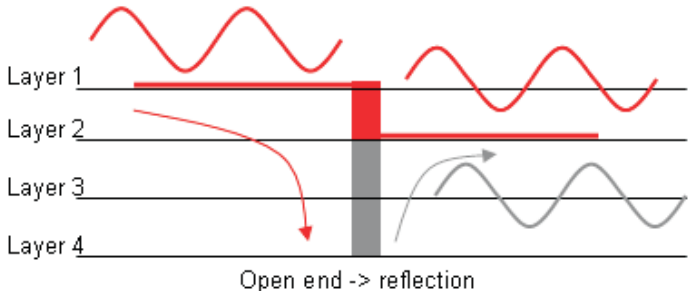

Figure 16. Reflection Caused by Stubs in a Via

Tips for routing traces and the use of vias:

- Do not use right-angle bends on traces with controlled impedance and fast rise time, respectively.
- Route the traces orthogonally to each other on adjacent layers to avoid coupling.
- To minimize crosstalk, the distance between two traces should be approximately 2 to 3 times the width of the trace.
- Differential traces should be routed as close as possible to get a high coupling factor. As a result of this, influenced noise is then a common-mode noise and is not a problem for a differential input stage.
- Do not use vias on traces with sensitive signals, if unnecessary.
- Be careful with the return current when changing the layers. Use ground vias around the signal via to make sure that the return current can flow as close as possible to the signal (see Figure 14).
- Do not create slots, for example in the ground plane, by using closely placed vias (see Figure 15).
- Consider stubs created by vias. If necessary, use blind vias or buried vias (see Figure 16).

Micro strip implementation for traces can have high crosstalk and are not recommended for high-speed digital systems. Stripline traces inherently have zero crosstalk and minimize the EMI/EMC (see *An EMC/EMI system-design and testing methodology for FPD-Link III SerDes* (SLYT719) for more information). Striplines require vias because traces have to buried inside the PCB. Vias do offer some parasitic inductance in the path, however, good news is that the impedance of a properly designed via can be controlled to avoid any reflections on the line. Before concluding that vias are good, consider another scenario in which a PCB via is passing through completely through the printed-circuit board. If the trace connections are made at one end of the via that leaves a *stub* on the other side. This stub would look like a capacitor on the TDR plot and can create resonance phenomena. At the quarter wave frequency, the open-ended stub looks like a short and produces nulls of transmission. Thus, the designer must *back drill* such vias after the PCB is fabricated. The dangling via stub can be trimmed by drilling from the back side.

2.6 Clock Distribution

Figure 17 shows four possible clock distribution circuits. The problems in Figure 17a are the enormous reflections at the branches and the different trace length to the devices. Because of the delay, it is possible that the system cannot function properly. To avoid the reflection at the branches, do not use them (see Figure 17b). Route the signal in a chain from one device to the other and realize a proper termination. Be careful with the delay. In a high-speed environment, it is possible that the data, sent from device A to device B, is out of date when the clock signal arrives at device B. A star connection as shown

in Figure 17c is a good solution to minimize the delay. A clock driver is used to distribute the clock signals to the different devices. To minimize the skew, the same trace length for every clock signal should be used. Figure 17d illustrates a solution for a complex system. A main clock feeds several clock drivers. Again, to reach low skew, implement delay-time compensation and use a proper termination to avoid reflections.

- Be careful with trace length in a clock distribution layout. Consider the delay for each trace. The best solution is to route these signals with the same length.
- Avoid branches to reduce reflections. Use a clock driver to distribute the signal to every device and consider a proper termination.

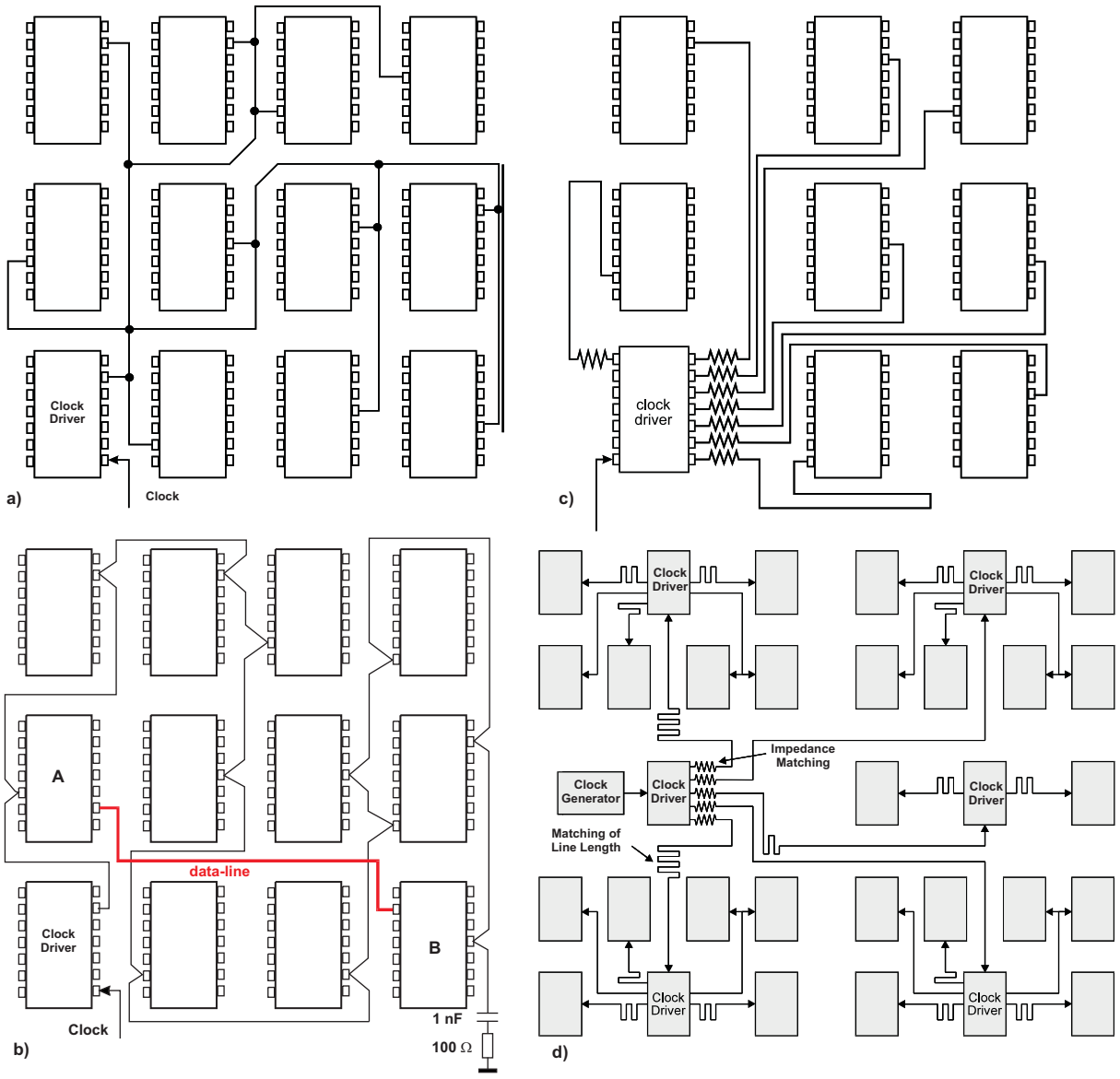

Figure 17. Poor and Good Clock Distribution on a PCB

3 Summary

This document presents an introduction to designing a PCB, a complex topic. However, the rules presented in this introduction can assist the designer in creating proper PCB designs. The higher the signal frequency with which the designer must contend, the more complicated will be the PCB design. Complicated PCB designs require a deep knowledge, experience, and simulation tools. However, it is not always necessary to route traces as short as possible, differential signals as close as possible, or to avoid crosstalk as much as possible. Rather, it depends on the signal on the trace. Basically, the designer must know which are the sensitive parts in the circuit or where problems due to reflections can occur. With this knowledge, a good placement of the devices can be made. Because placement is such an important step in high-speed design, the designer will do well to always keep it and the return current in mind.

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Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (November 2006) to A Revision	Page
• Added content to *Crosstalk* section	8
• Added content to *Decoupling Capacitors* section	13

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