Chapter 5
Backplane design considerations and Bus LVDS

Many high-speed applications require more than just the ability to run point-to-point or from one driver to multiple receivers. Multiple driver(s) and/or receiver(s) on one interconnect is an efficient and common bus application. This requires a double termination of the interconnect to properly terminate the signal at both ends of the bus. Multipoint configurations offer an efficient balance between interconnect density and throughput. LVDS drivers are not intended for double termination loads, thus an enhanced family of devices was invented by National to bring the advantages of LVDS to bus applications.

For multidrop (with the driver located in the middle) and multipoint applications, the bus normally requires termination at both ends of the media. If the bus were terminated with 100Ω at both ends, a driver in the middle would see an equivalent load of 50Ω. Depending upon the load spacing, the effective impedance of the bus may drop further, and for signal quality reasons, the terminations may be as low as 60Ω. Again, a driver would see both resistors in parallel, thus a 30Ω load.

Standard (644) LVDS drivers have only 3.5 mA of loop current. If these were used to drive the doubly terminated bus with a termination load of 30Ω, they would only generate a 105 mV differential voltage on the bus. This small differential voltage is not sufficient when noise margins, reflections, over-drive and signal quality are taken into account. In fact, even doubling the drive is not enough for a heavily loaded backplane application.

Bus LVDS addresses the issue of driving a low impedance interconnect by boosting its driver current to about 10 mA. This means that into a load as low as 30Ω, a 300 mV differential signal is maintained. Thus, LVDS-like signaling with all of its benefits is obtained in doubly terminated bus applications.

5.1 Configurations

Backplanes present special challenges to data transmission systems. This is due to the variety of interconnections (multidrop, multipoint, and switch fabrics) and also the close spacing of the loads. For these very reasons, National invented the Bus LVDS family of interface devices to extend the benefits of LVDS into backplane applications, which commonly require two terminations.

There are a number of ways of implementing high-speed backplanes. Each of these ways of implementing a backplane has advantages and disadvantages.

5.1.1 Multidrop (single termination)

A multidrop bus consists of one transmitter and multiple receivers (broadcast bus). Note that the driver is restricted to be located at one end of the bus and the other end is terminated. This configuration is useful for data distribution applications and may employ standard LVDS or Bus LVDS devices depending upon loading.

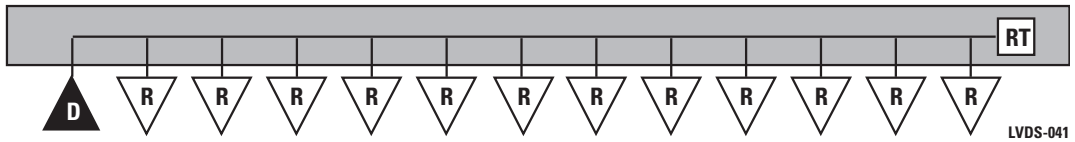

Figure 5.1. Multidrop application with a single termination

This architecture lends itself to serialization of the bus but without the need for a central switch card/chip. Serialization results in less interconnect (fewer connector pins and backplane traces) which in many cases reduces the stack-up of the backplane to fewer layers.

A disadvantage of this configuration is the restricted location of the driver, and (if required) complexity of a back channel (communication path from the loads back to the source).

5.1.2 Multidrop (double termination)

A multidrop bus consists of one transmitter and multiple receivers (broadcast bus). Note that with Bus LVDS, the driver can be placed anywhere in the multidrop bus and the bus is terminated at both ends.

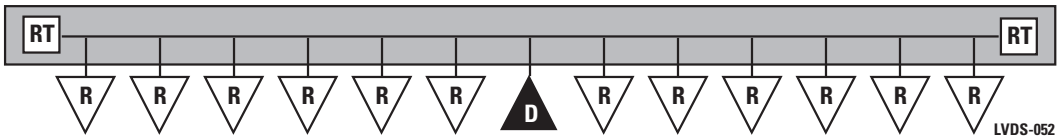

Figure 5.2. Multidrop application with double termination

Again, this architecture lends itself to serialization of the bus but without the need for a central switch card/chip. Serialization results in less interconnect (fewer connector pins and backplane traces). The advantages and disadvantages are the same as those discussed in Section 5.1.1.

5.1.3 Data distribution with point-to-point links

A distribution amplifier can also be used to buffer the signal into multiple copies which then drive independent interconnects to their loads. This offers optimized signal quality, the capability to drive long leads (long stub) to the loads, at the expense of interconnect density.

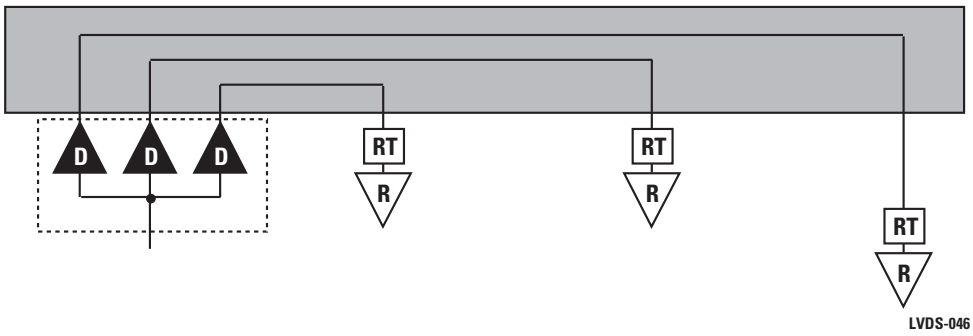

Figure 5.3. Data distribution application

5.1.4 Multipoint

The multipoint bus requires the least amount of interconnect (routing channels and connector pins), while providing bi-directional, half-duplex communication.

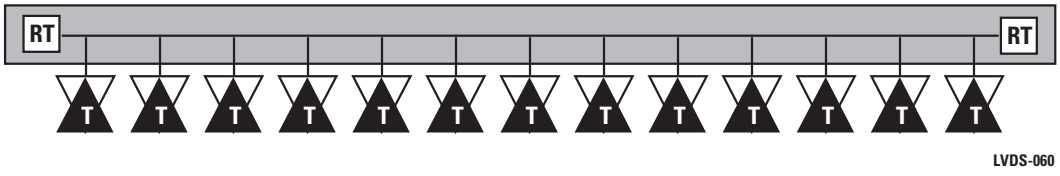

Figure 5.4. Multipoint application

However, on this type of bus, there can only be one transaction at a time. Thus, a priority and arbitration scheme are typically required. These may be protocol or hardware solutions, depending upon the application.

5.1.5 Switch matrix

Switch busses are growing in popularity for systems that require the very highest throughput possible. It is possible to have simultaneous transactions occurring on the switch bus at the same time and it has the cleanest electrical signal path of all the bus options (multidrop and multipoint, due to the no-stub effect).

The disadvantage of this type of scheme is that interconnect density increases with the number of loads, and also the complexity of the central switching card.

The switch application, due to its inherent optimized signal quality, is commonly used for links running hundreds of megabits per second into the gigabit per second range. The top speed tends to be limited by the bandwidth of the interconnect.

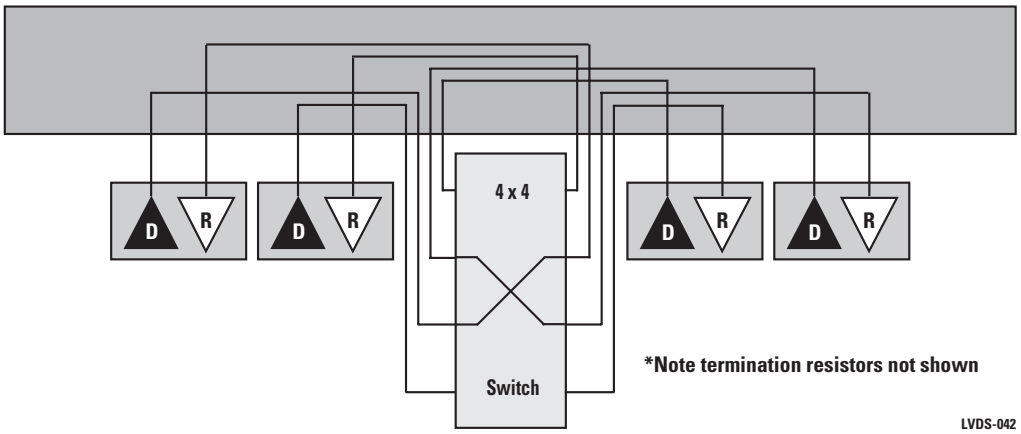

Figure 5.5. Switch application

5.2 Bus LVDS

5.2.1 System benefits of Bus LVDS

There are numerous system benefits to using Bus LVDS over other technologies that have historically been used for bus interconnect. Many of these advantages are discussed next, but can be summed up again with "Gigabits @ milliwatts!".

5.2.2 High-speed capability

Bus LVDS is capable of driving a multidrop or multipoint bus at high-speeds – for example:

- at 155 Mbps across a 20 slot multipoint FR4 backplane
- at 400 Mbps across a 10 slot multidrop FR4 backplane
- at 66 MHz with ultra-low skew clock buffers
- at 800 Mbps for point-to-point links

Previously, this has only really been achievable with the more costly high-speed ECL products. These present a translation challenge between common TTL devices and ECL drivers, and also power supply/termination problems. Other single-ended technologies were limited to sub 100 MHz applications and presented tough termination and power dissipation problems. For a detailed comparison of backplane technologies, please refer to National Application Note 1123 – Sorting out Backplane Driver Alphabet Soup.

5.2.3 Low power

Bus LVDS switches an interconnect with only 10 mA of loop current. This is much less than other high performance bus technologies that use large amounts of current (as much as 80 mA in the case of BTL and 40+ mA for GTL) to switch a bus with an incident wave. Typically, the load power for Bus LVDS is only 2.5 mW. The current-mode drivers tend to offer low power dissipation, even at high data signaling rates. Lastly, with the low swings required, the supply rails may be less than 5V, 3.3V, or even 2.5V. These three reasons make LVDS and Bus LVDS components extremely low power.

5.2.4 Low swing/low noise/low EMI

Bus LVDS uses a low swing differential signal. This small balanced signal transition generates small EMI, and the current-mode driver limits spiking into the supply rails. These reasons make the Bus LVDS driver capable of running at better than 10x the frequency of TTL at lower EMI levels.

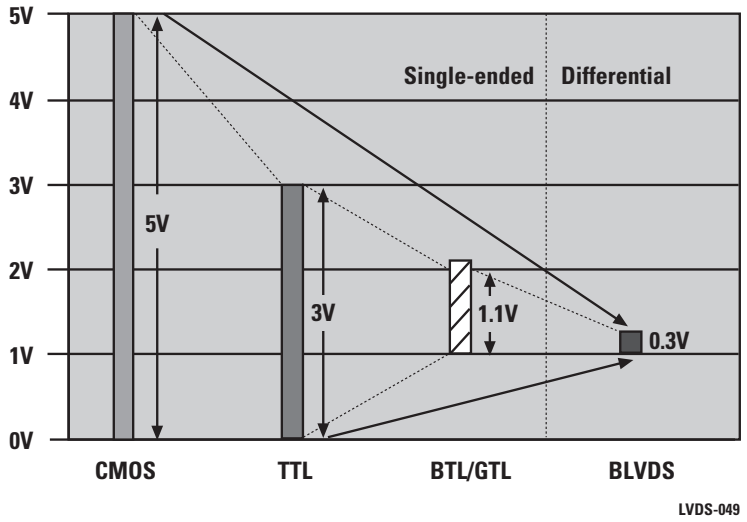

Figure 5.6. Comparison of voltage swings for various backplane technologies

CMOS and TTL technologies use a large swing and often large currents in order to switch a bus. This switching can cause ringing and undershoot which can be a large contributor to system EMI.

BTL addressed this noise issue by reducing its output swing to just 1V. However, it still uses large amounts of current to switch the bus with an incident wave (80 mA typical) and still uses the single-ended approach with limited noise margins and a complex termination scheme.

As we have seen, Bus LVDS uses only 10 mA to switch the bus with an incident wave, is low swing (300 mV typical) and is differential. We saw in Section 3.3 how differential signaling can help substantially reduce system EMI. The small swing also provides the high-speed capability while consuming minimal power.

5.2.5 Low system cost

All of National's Bus LVDS products are implemented in a core CMOS technology, which allows for low manufacturing cost and the ability to integrate more functionality onto one piece of silicon. By putting the coding, clock recovery, and other PHY/LINK layer digital functions into the interface device, ASIC complexity and risk is greatly reduced. Immense system savings can be obtained through the use of the serializer and deserializer chipsets. Connectors, cable size, and cost may be reduced. In most cases, these savings more than compensate for the interface silicon cost!

5.2.6 System benefits

Besides the cost effectiveness of using Bus LVDS, there are also other system savings in using Bus LVDS:

- Low power
  - Its CMOS design helps reduce the cost of system power supplies and cooling, enabling fan-free applications!
- Simple passive terminations
  - A bus can be implemented using only discrete components for termination. Other high-speed bus technologies such at GTL, BTL and ECL require active termination devices and/or oddball supply rails, (+1.5V, +2.1V for example) which add to system cost and power distribution complexity.
- Serialization
  - National's Bus LVDS portfolio consists of bus-able serializers and deserializers which reduce system interconnect and connector size.
- Low noise
  - The low noise characteristic of Bus LVDS help with the limitation of EMI within a system which can help with system cycle times and system cost reductions.

5.3 Backplane design considerations

Prior to the start of any system design, the following methodology should be used.

1. System design starts with a solid power and ground distribution system. When this is left to the last step, it tends to be the source of noise and EMI problems.
2. Next, consider the transmission line configuration and layout. Optimize paths to provide the best signal quality. Locating certain devices close to the connector location and other devices (potential noise sources) far away is one way to do this. Give priority to the layout of the transmission line traces to avoid unnecessary via and imbalances.
3. Complete the remaining digital design.
4. Always review the completed layout.

5.3.1 Loading effects

Figure 5.7 shows a differential bus with one card plugged in. The card adds a load to the bus, which is mainly composed of a bulk capacitance load resulting from the connector (2 pF to 3 pF), the PCB trace (2 pF to 3 pF), and the device (4 pF to 5 pF), for a total load of about 10 pF. Limit the number of vias on the card's stub to minimize capacitance loading. Also keep stub lengths as short as possible. These two tips will help maintain a high "loaded" bus impedance that will increase noise margins.

The flexibility of programmable devices comes at the cost of capacitance. National's Bus LVDS products have an I/O capacitance of 5 pF. The I/O capacitance of a programmable device is approximately double, or 10 pF. This increase in capacitance will lower the loaded bus impedance, thereby reducing the available noise margin and lowering the maximum frequency of operation in the design.

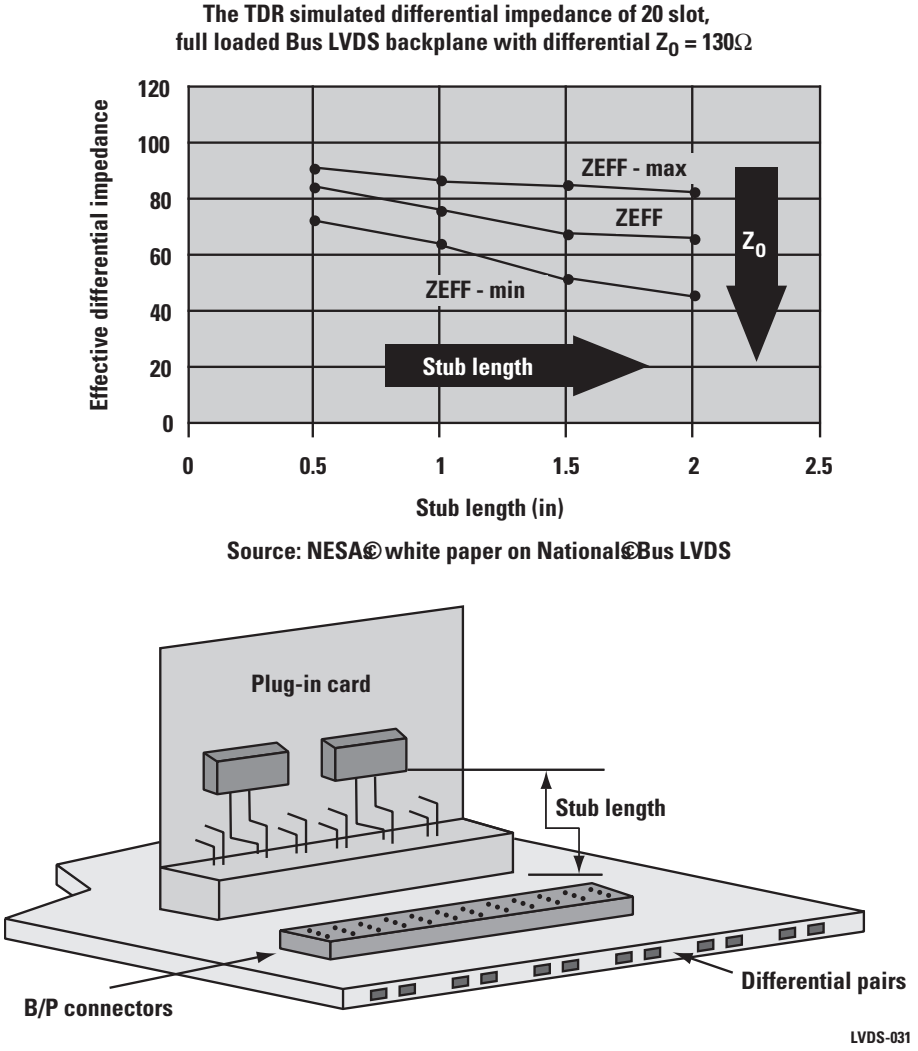

Figure 5.7. Diagram of backplane demonstrating stub length

Bus LVDS is capable of operating in wild card configurations! Depending upon system noise margin goals, full card loading is NOT required. Termination selection is a bit tricky, but should be matched to a fully loaded case (or slightly higher). Signal integrity is good even for half loaded or section loaded busses! Single-ended technologies cannot support this feature due to noise margin violations.

Figure 5.8 provides a TDR simulation of backplane impedance vs. loading.

- Case A shows the raw traces only (no via)
- Case B inserts the backplane connectors
- Case C adds all the cards into the bus, note that the cards do not include the device
- Case D adds the device to the card, thus it is a fully loaded system

Notice that about 50% of the loading is due only to the backplane connectors and their vias. Also notice how the velocity of the signal is slowed by the loading. The final loaded impedance of the bus requires two 56Ω termination resistors placed at each end of the bus.

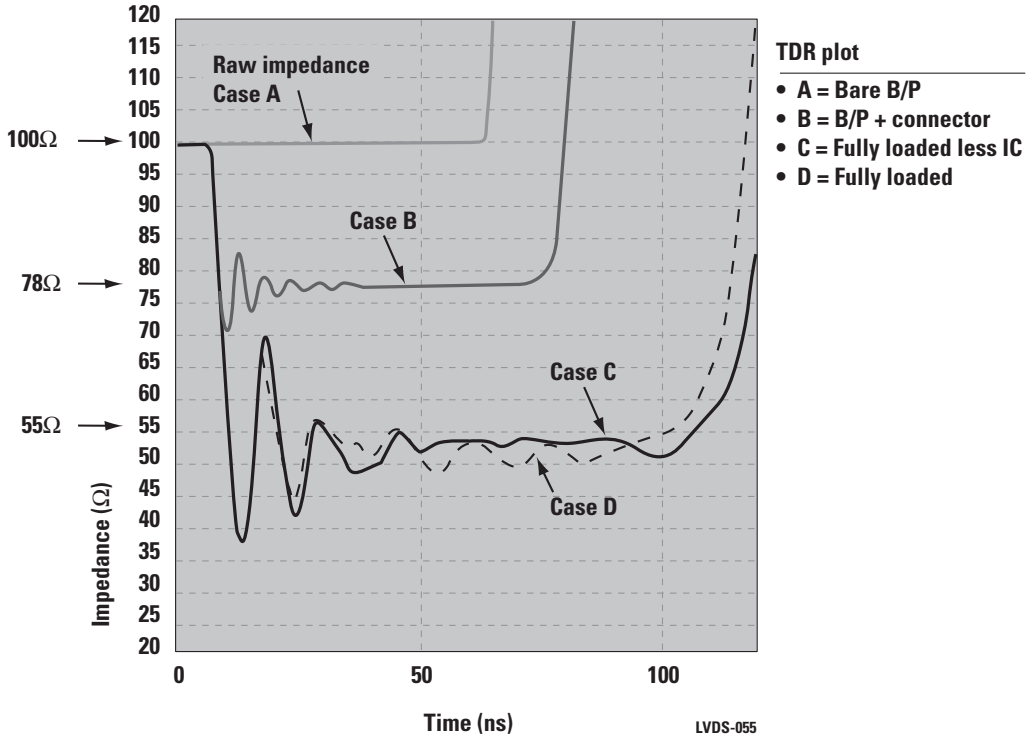

Figure 5.8. TDR plots

5.3.2 Bus termination

Termination is required for two reasons:

1. Current-mode drivers require the resistor to complete the current loop.
2. Bus LVDS edge rates are fast and the interconnect will act as a transmission line; therefore terminations are needed to limit reflections.

Bus LVDS only requires a simple termination of a single surface mount resistor across the line at each end of the bus for multipoint applications. There is no need for a special VT rail or active termination devices, as with single-ended technologies (TTL/BTL/GTL). The resistor should be equal to or slightly greater than the loaded differential impedance of the line. Typically, it is located at both ends of the backplane depending upon the configuration/application. (See also Section 4.6 on Failsafe Biasing).

5.3.3 Stub length

A long stub adds to the capacitive load, lowers the loaded impedance even more and tends to impact signal quality. For this reason, stub interconnect should be a microstrip and the number of vias (0 to 1 is best) should be limited. Figure 5.9 is from the NESA (North East System Associates, Inc.) white paper on Bus LVDS* (available from LVDS.national.com) and illustrates how increasing stub length lowers the loaded impedance. That same paper studies the relationship between maximum stub-length and data-rate. There is a strong correlation between the edge rate of a signal, and the maximum stub length that can be supported. LVDS drivers generate rising and falling edges in the region of 0.2 ns to 0.5 ns. Figure 5.9 is a TDR trace, where the launched signal has an edge rate of 0.3 ns and is therefore a good simulation of a real LVDS signal. The paper concludes that stub lengths should typically be 1 to 1.5 in. or less. As frequency increases, edge rates also typically increase.

There is one golden rule for stubs: **The shorter the better!**

**Signal Integrity and Validation of National's Bus LVDS (BLVDS) Technology in Heavily Loaded Backplanes*. Dr. Jinhua Chen et al. North East Systems Associates, Inc.

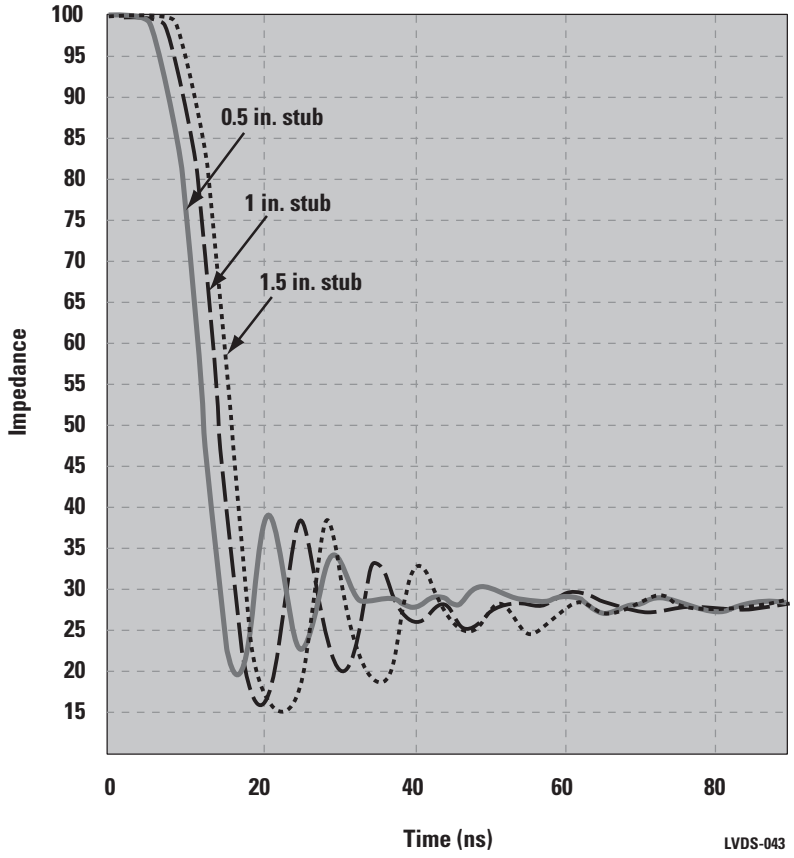

Figure 5.9. TDR plot with 300 ps input signal vs. 0.5 in., 1.0 in., and 1.5 in. stub

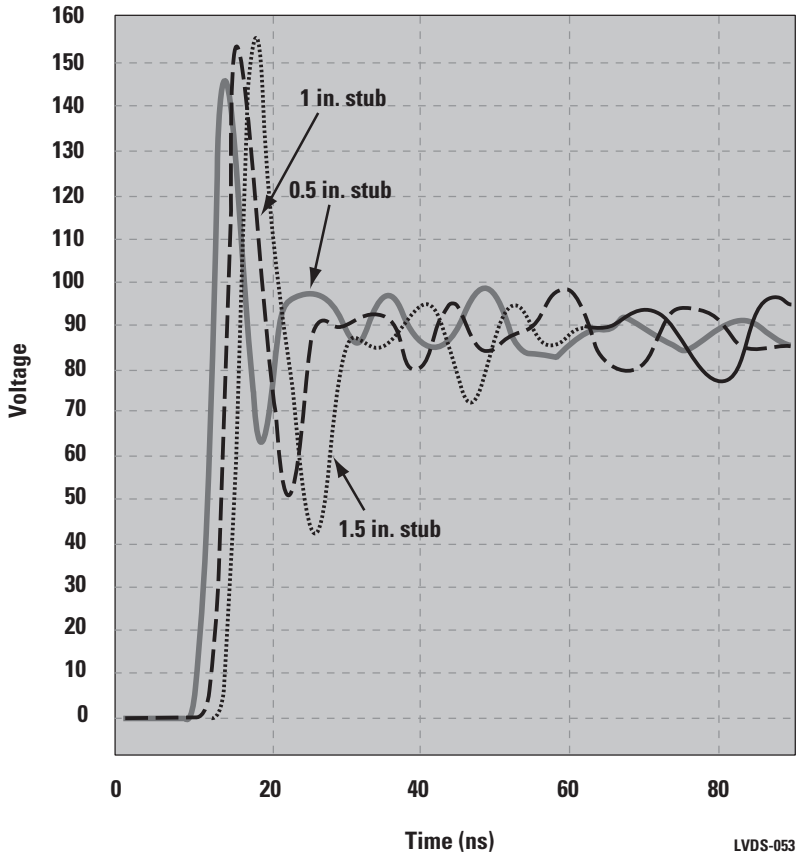

Figure 5.10. 300 ps input signal vs. 0.5", 1.0" and 1.5" stub

5.3.4 Connectors

Connectors are a complex topic and are the subject of many heated debates at standard committee meetings. There are two basic types: standard matrix based connectors (3 rows of 32 pins) and special connectors. The special connectors may be optimized for differential signals or may use elaborate techniques to clamp to the PCB. The elaborate connectors tend to avoid via structures and thus offer the highest bandwidth. However, they are also very application specific and tend to be rather expensive.

More common is the use of standard connectors for a mix of differential, power, ground and single-ended connections (see Figure 5.11). The graphic shows a variety of pinout recommendations for single-ended and differential options.

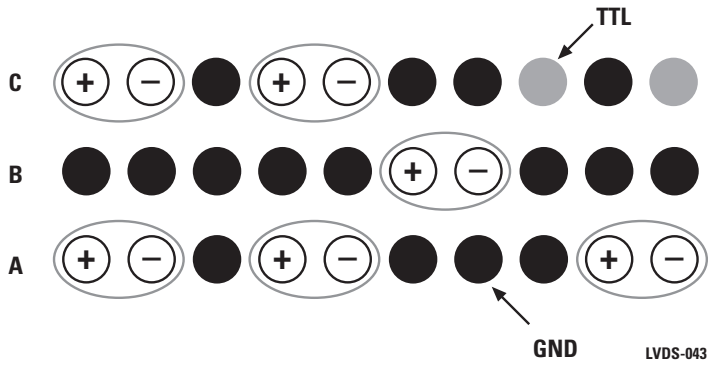

Figure 5.11. Typical connector pinouts

For differential lines in a matrix (single-ended) connector, adjacent pins in a row tend to be better as electrical lengths are the same. In addition, the row with the shorter path provides a better path over a longer row.

Ground signal assignment can be used to isolate large swing (TTL) signals from the small-swing lines (LVDS) as shown in Figure 5.11.

Connector example: Teradyne VHDM high-speed differential connector

This is a differentially optimized high-density connector for applications into the Gigabit per second range. It is offered in both 8-row (which provides 3 differential pairs) and 5-row (which provides 2 differential pairs) configurations. The 8-row connector can coexist with the basic 8-row VHDM single-ended connector and also power/ground contacts. Shielding is provided between wafers providing excellent isolation of signal contacts. The backplane layout is also improved over earlier generations and the new footprint now supports wider traces (10 mils) to be routed through the pin field easing backplane design. The backplane side of the connector accepts either the single-ended or differential versions of VHDM. Skew has been minimized within the pair and pairs are also routed together (see next drawing). This is an example of a high-throughput differential optimized connector that provides excellent signal quality. For details, please visit the Teradyne website at: www.teradyne.com/prods/bps/vhdm/hsd.html.

Check our LVDS website (LVDS.national.com) for the results of this testing. The white paper containing the test details was presented at DesignCon 2001 and titled, “Gigabit Backplane Design, Simulation and Measurement - the unabridged story.”

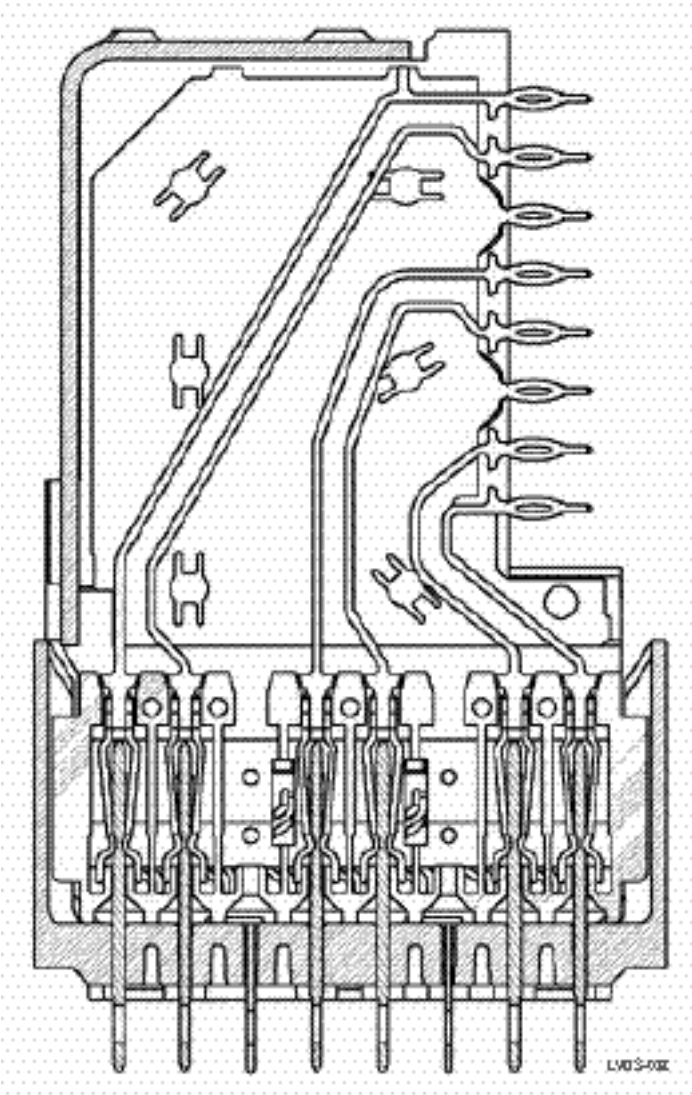

Figure 5.12. Cross section of VHDM HSD (graphic courtesy of Teradyne)

5.3.5 Failsafe biasing

Failsafe biasing may be required if a known state is required on the bus when any of the following conditions occur:

- All drivers are in TRI-STATE – common in multipoint applications.
- All drivers are removed or powered-off

If this is the case, additional biasing (beyond the internal failsafe biasing of the receivers) may be provided with a failsafe biasing (power) termination as shown in Figure 5.13.

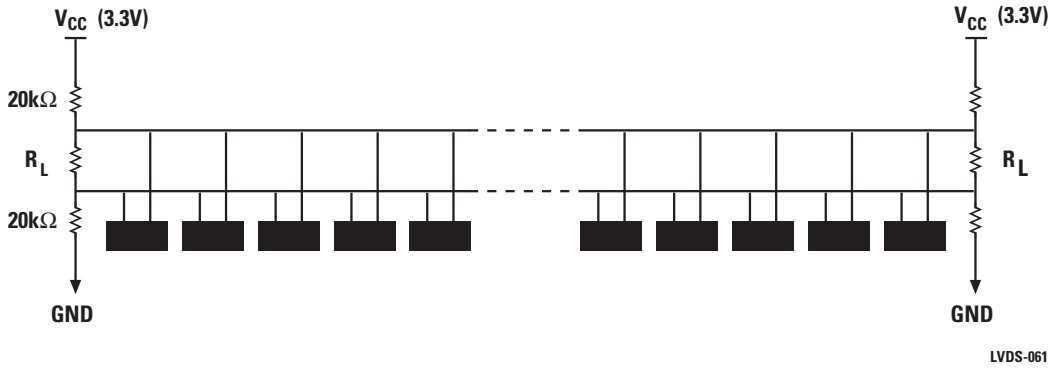

Figure 5.13. Multipoint bus with failsafe bias

In selecting failsafe resistor values note the following:

- The magnitude of the resistors should be one to two orders higher than the termination resistor, to prevent excessive loading to the driver and waveform distortion
- The mid-point of the failsafe bias should be close to the offset voltage of the driver (+1.25V) to prevent a large common-mode shift from occurring between active and TRI-STATE (passive) bus conditions
- The pull-up and pull-down resistors should be used at both ends of the bus for the quickest response
- Note that signal quality is reduced as compared to active driving (on/on)
- See Section 4.6 for equations for selecting failsafe biasing resistors

5.3.6 Hot plugging/live insertion

Live insertion, or hot swapping, is of particular importance to the telecommunications marketplace. In these applications, it is critical that maintenance, upgrading and repair can be performed without shutting down the entire system or causing disruption to the traffic on the backplane. Bus LVDS's wide common-mode range of ±1V plays a key role in supporting this function. Upon insertion of a card into a live backplane, the occurrence of abnormalities on the signals are common on both signals, thus data is not impacted. This allows for safe hot swapping of cards, making the systems robust and reliable.

Lab testing done in National's LVDS interface lab has shown zero-bit errors while plugging in or removing cards from an active bus (BERT test). During the test, up to four cards were inserted at once without an error! This is due to the fact that the differential lines equally load the active line on contact and any glitch seen is a common-mode modulation that is ignored by the receivers.

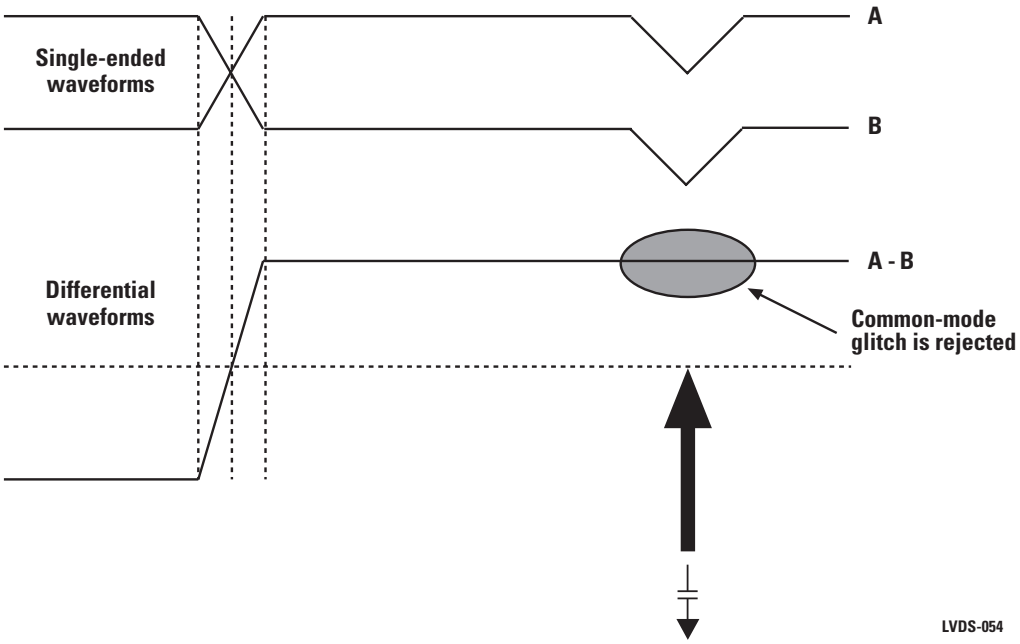

Figure 5.14. Live insertion waveforms

However, standard power sequencing is still recommended to ensure proper biasing of the devices (substrate). For insertion, the following sequence should be guaranteed by hardware design:

1. Ground
2. Power
3. I/O pins

For removal, the reverse order is recommended (3-2-1). This sequence can be supported a number of ways. Staggered power pin connectors may be employed (available from multiple sources and even compatible with many matrix connector styles). Multiple connectors are also commonly used. A DIN connector for the I/O, and "Jack" like connectors for power and ground is one approach. Yet another option uses card edge contact on the rails to establish a GND bias when the card is first inserted into the card rail.

5.4 Additional information

Detailed backplane design information is available from National's website in the form of white papers and application notes. National has also teamed up with NESA and jointly published a number of white papers and conference papers. Recent papers are available from both websites:

- LVDS.national.com
- http://www.nesa.com