Chapter 3
High-speed design

3.1 PCB layout tips

As a technology, LVDS is relevant in systems where the data rates range from around 100 MHz to 2 GHz. At these frequencies a PCB can no longer be treated as a simple collection of interconnects. Traces carrying these high-speed signals need to be treated like transmission lines. These transmission lines should be designed with appropriate impedance and they need to be correctly terminated.

The topics covered in this chapter range from impedance calculations and signal integrity to proper power-supply design. They are relevant for any high-speed design, whether it employs ECL, CML, or LVDS.

Generalized design recommendations are provided next.

The fast edge rate of an LVDS driver means that impedance matching is very important – even for short runs. Matching the differential impedance is important. Discontinuities in differential impedance will create reflections, which will degrade the signal and also show up as common-mode noise. Common-mode noise on the line will not benefit from the canceling magnetic field effect of differential lines and will be radiated as EMI.

Controlled differential impedance traces should be used as soon as possible after the signal leaves the IC. Try to keep stubs and uncontrolled impedance runs to <12 mm or 0.5 in. Also, avoid 90° turns since this causes impedance discontinuities; use 45° turns, radius or bevel PCB traces.

Minimize skew between conductors within a differential pair. Having one signal of the pair arrive before the other creates a phase difference between voltages along the signal pairs that appear and radiate as common-mode noise.

Use bypass capacitors at each package and make sure each power or ground trace is wide and short (do not use 50Ω dimensions) with multiple vias to minimize inductance to the power planes.

A detailed list of suggestions for designing with LVDS is shown next. The suggestions are cost-efficient and easy to implement. By using these suggestions as guidelines, your LVDS-based systems should provide maximum performance and be quick and easy to develop.

3.1.1 PCB design

1. Use at least 4 PCB board layers (top to bottom): LVDS signals, ground, power, TTL signals. Dedicating planes for V_{CC} and ground are typically required for high-speed design. The solid ground plane is required to establish a controlled (known) impedance for the transmission line interconnects. A narrow spacing between power and ground will also create an excellent high frequency bypass capacitance.
2. Isolate fast edge rate CMOS/TTL signals from LVDS signals, otherwise the noisy single-ended CMOS/TTL signals may couple crosstalk onto the LVDS lines. It is best to put TTL and LVDS signals on a different layer(s), which should be isolated by the power and ground planes.
3. Keep drivers and receivers as close to the (LVDS port side) connectors as possible. This helps to ensure that noise from the board is not picked up onto the differential lines and will not escape the board as EMI, from the cable interconnect. This recommendation also helps to minimize skew between the lines. Skew tends to be proportional to length; therefore, by limiting length, we also limit skew. Please see Chapter 5 for more information on routing high-speed signals through connectors.
4. Bypass each LVDS device and also use distributed bulk capacitance. Surface mount capacitors placed close to power and ground pins work best.

Power supply: A 4.7 µF or 10 µF, 35V tantalum capacitor works well between supply and ground. Choosing a capacitor value which best filters the largest power/ground frequency components (usually 100 MHz to 300 MHz) is best. This can be determined by checking the noise spectrum of V_{CC} across bypass capacitors. The voltage rating of tantalum capacitors is critical and must not be less than 5 x V_{CC}. Some electrolytic capacitors also work well.

V_{CC} pins: One or two multi-layer ceramic (MLC) surface mount capacitors (0.1 µF and 0.01 µF) in parallel should be used between each V_{CC} pin and ground if possible. For best results, the capacitors should be placed as close as possible to the V_{CC} pins to minimize parasitic effects that defeat the frequency response of the capacitance. Wide (>4 bits) and PLL-equipped (e.g., channel link and FPD-link) LVDS devices should have at least two capacitors per power type, while other LVDS devices are usually fine with a 0.1 µF capacitor. The bottom line is to use good bypassing practices.

EMI problems often start with power and ground distribution problems. EMI can be greatly reduced by keeping power and ground planes quiet. As a general rule of thumb, a target of <100 mV of noise on the power lines should be the target for power supply bypassing; however, some devices have more stringent requirements. Consult your device's datasheet for exact requirements.

1. Power and ground should use wide (low impedance) traces — their job is to be a low impedance point. Do not use 50Ω design rules on power and ground traces.
2. Keep ground PCB return paths short and wide. Provide a return path that creates the smallest loop for the image currents to return.
3. Cables should employ a ground return wire connecting the grounds of the two systems. This provides for common-mode currents to return on a short known path and is especially important in box-to-box applications where ground return paths will help limit shifts in ground potential. See Section 6.3.
4. Use two vias to connect to power and ground from bypass capacitor pads to minimize inductance effects. Surface mount capacitors are good as they are compact and can be located close to device pins.

3.1.2 Traces

1. Edge-coupled microstrip, edge-coupled stripline, or broad-side striplines all work well for differential lines.
2. Traces for LVDS signals should be closely coupled and designed for 100Ω differential impedance. See Section 3.1.3.
3. Edge-coupled microstrip lines offer the advantage that a higher differential Z_O is possible (100Ω to 150Ω). Also, it may be possible to route from a connector pad to the device pad without any via. This provides a "cleaner" interconnect. A limitation of microstrip lines is that these can only be routed on the two outside layers of the PCB, thus routing channel density is limited.
4. Stripline may be either edge-coupled or broad-side coupled lines. Since they are embedded in the board stack and typically sandwiched between ground planes, they provide additional shielding. This limits radiation and also limits coupling of noise onto the lines. However, they do require the use of vias to connect to them.

3.1.3 Differential traces

1. Use controlled impedance PCB traces that match the differential impedance of your transmission medium (e.g., cable) and termination resistor. Route the differential pair traces as close together as possible and as soon as they leave the IC. This helps to eliminate reflections and ensures that noise is coupled as common-mode. Signals that are 1 mm apart radiate far less noise than traces 3 mm apart, as magnetic field cancellation is much better with the closer traces. In addition, noise induced on the differential lines is much more likely to appear as common-mode which is rejected by the receiver.

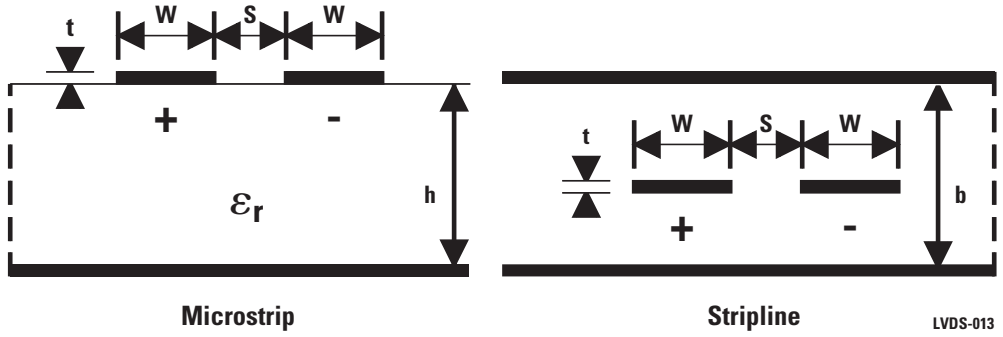


Figure 3.1. Microstrip and stripline differential traces

When designing for a specific differential Z_O (Z_{DIFF}) for edge-coupled lines, it is best to adjust trace width "W" to alter Z_{DIFF}. It is not recommended to adjust "S" which should be the minimum spacing specified by your PCB vendor for line-to-line spacing. You can obtain National's Transmission Line RAPIDESIGNER by visiting our website (search for Rapidesigner) or contact the National support center for your area. (Lit# 633200-001 metric or Lit# 633201-001 English units) and application note AN-905, (Lit# 100905-002) to calculate Z_O and Z_{DIFF}, or use the equations below for edge-coupled differential lines:

Microstrip

$$Z_{DIFF} \approx 2 \times Z_0 \left(1 - 0.48 e^{-0.96 \frac{S}{h}}\right) \Omega$$

Stripline

$$Z_{DIFF} \approx 2 \times Z_0 \left(1 - 0.374 e^{-0.29 \frac{S}{h}}\right) \Omega$$

Microstrip

$$Z_0 = \frac{60}{\sqrt{0.457 \varepsilon_r + 0.67}} \ell n \left(\frac{4h}{0.67\left(0.8W + t\right)}\right) \Omega$$

Stripline

$$Z_0 = \frac{60}{\sqrt{\varepsilon_r}} \ell n \left(\frac{4b}{0.67\pi\left(0.8W + t\right)}\right) \Omega$$

Note: For edge-coupled striplines, the term "0.374" may be replaced with "0.748" for lines which are closely coupled (S < 12 mils).

Broadside coupled line structures can also be used. The dimensions for this type of line are shown in Figure 3.2. Broadside coupled striplines can be useful in backplane design as these use only one routing channel and may be easier to route through the connector pin field.

There is no closed-form equation for calculating the impedance of broadside-coupled stripline. Instead, a field solver should be used.

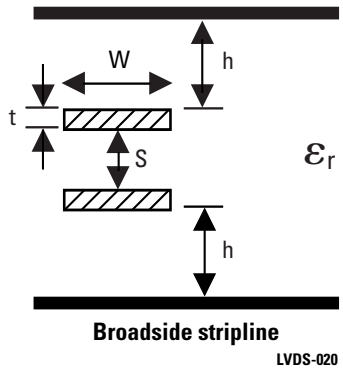


Figure 3.2. Broadside couple stripline

Always use consistent dimensions (e.g., all dimensions in mils, cm or mm) for S, h, W, and t when making calculations.

Cautionary note: The expressions for Z_{DIFF} were derived from empirical data and results may vary. Please refer to AN-905 for accuracy information and ranges supported.

Common values of dielectric constant (εr) for various printed circuit board (PCB) materials are given in Table 3.1. Consult your PCB manufacturer for actual numbers for the specific material that you plan to use. Note that in most LVDS applications, the widely used FR-4 PCB material is acceptable. GETEK is about 1.5x as expensive as FR-4, but can be considered for 1000+ MHz designs. Also note that ε_r will vary within a single board. It is not uncommon for FR-4 PCBs to vary by 10% across one board, affecting skew. This is another good reason to keep differential lines close together.

Table 3.1. Properties of PCB materials

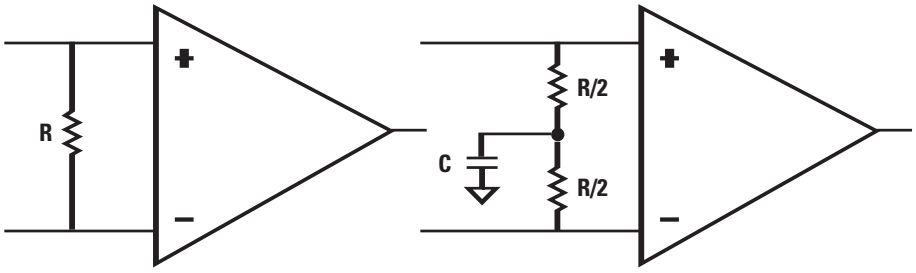
PCB material	Dielectric constant (′r)	Loss tangent
Air	1.0	0
PTFE (Teflon)	2.1 to 2.5	0.0002 to 0.002
BT resin	2.9 to 3.9	0.003 to 0.012
Polyimide	2.8 to 3.5	0.004 to 0.02
Silica (quartz)	3.8 to 4.2	0.0006 to 0.005
Polyimide/glass	3.8 to 4.5	0.003 to 0.01
Epoxy/glass (FR-4)	4.1 to 5.3	0.002 to 0.02
GETEK	3.8 to 3.9	0.010 to 0.015 (1 MHz)
ROGERS4350 core	3.48 ± 0.05	0.004 @ 10G, 23°C
ROGERS4403 prepreg	3.17 ± 0.05	0.005 @ 10G, 23°C

2. Match electrical lengths between traces of a pair to minimize skew. Skew between the signals of a pair will result in a phase difference between the signals. That phase difference will destroy the magnetic field cancellation benefits of differential signals and EMI will result! (Note that the velocity of propagation, v = c/εr where c (the speed of light) = 0.2997 mm/ps or 0.0118 in./ps). A general rule is to match lengths of the pair to within 100 mils.

3. Do not rely solely on the auto-route function for differential traces. Carefully review dimensions to match trace length and to ensure isolation between pairs of differential lines.
4. Minimize the number of vias and other discontinuities on the line.
5. Avoid 90° turns (these cause impedance discontinuities). Use arcs or 45° bevels instead.
6. Within a pair of traces, the distance between the two traces should be minimized to maintain common-mode rejection of the receivers. On the printed circuit board, this distance should remain constant to avoid discontinuities in differential impedance. Minor violations at connection points are allowable. The key to "imbalances" is to make as few as possible and as small as possible. Differential transmission works best on a balanced interconnect. For the best results, both lines of the pair should be as identical as possible.

3.1.4 Termination

1. Use a termination resistor that best matches the differential impedance of your transmission line. It should be between 90Ω and 130Ω for point-to-point cable applications. Remember that the current-mode outputs need the termination resistor to generate the proper differential voltage. LVDS is not intended to work without a termination resistor.
2. Typically, a single, passive resistor across the pair at the receiver end suffices.
3. Surface mount resistors are best. PCB stubs, component leads, and the distance from the termination to the receiver inputs should be minimized. The distance between the termination resistor and the receiver should be <7 mm (12 mm max.).
4. Resistor tolerance of 1% or 2% is recommended. Note that from a reflection point of view, a 10% mismatch in impedance causes a 5% reflection. The closer the match, the better. Match to the nominal differential impedance of the interconnect. For multidrop/multipoint applications, match the differential impedance to the fully loaded case.
5. Center tap capacitance termination may also be used in conjunction with two 50Ω resistors to filter common-mode noise at the expense of extra components if desired. This termination is not commonly used or required.



Where R = Z_{DIFF} (between 100Ω and 120Ω), C ≈ 50 pF

Components should be surface-mount components, placed close to the receiver.

Use 1-2% resistors.

LVDS-015

Figure 3.3. Common differential termination schemes

3.1.5 The "S" Rule

Using the edge-to-edge "S" distance between the traces of a pair, other separations can be defined:

- The distance between two pairs should be >2S.
- The distance between a pair and a TTL/CMOS signal should be >3S at a minimum. Even better, locate the TTL/CMOS signals on a different plane isolated by a ground plane.
- If a guard ground trace or ground fill is used, it should be >2S away.

3.2 Lowering Electromagnetic Interference (EMI)

3.2.1 Electromagnetic radiation of differential signals

Today's increasing data rates and tough electromagnetic compatibility (EMC) standards are making electromagnetic radiation an increasing concern. System designers are usually most concerned with far field electromagnetic radiation, propagated through transverse electromagnetic (TEM) waves, which can escape through shielding and cause a system to fail EMC tests.

Fields around a conductor are proportional to voltage or current, which are small in the case of LVDS. The fields are distorted by and interact with their environment, which is why EMI is so hard to predict. The fields can be distorted to advantage, however, and such is the case with tightly coupled differential lines ("+" and "–" signals in close proximity with one another).

In single-ended lines like CMOS/TTL lines shown in Figure 3.4, almost all the electric field lines are free to radiate away from the conductor. Certain structures can intercept these fields. But some of these fields can travel as TEM waves which may escape the system and cause EMI problems.

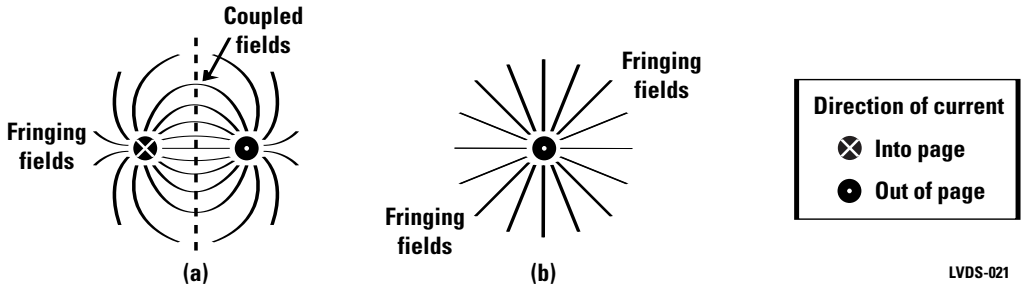


Figure 3.4. Electromagnetic field cancellation in differential signals (a) through coupling vs. a single-ended signal (b)

Balanced differential lines, however, have equal but opposite ("odd" mode) signals. This means that the concentric magnetic field lines tend to cancel and the electric fields (shown in Figure 3.4b) tend to couple. These coupled electric fields are "tied up" and cannot escape to propagate as TEM waves beyond the immediate vicinity of the conductors. Only the stray fringing fields are allowed to escape to the far field. Therefore, for coupled differential signals, much less field energy is available to propagate as TEM waves vs. single-ended lines. The closer the "+" and "–" signals, the tighter or better the coupling.

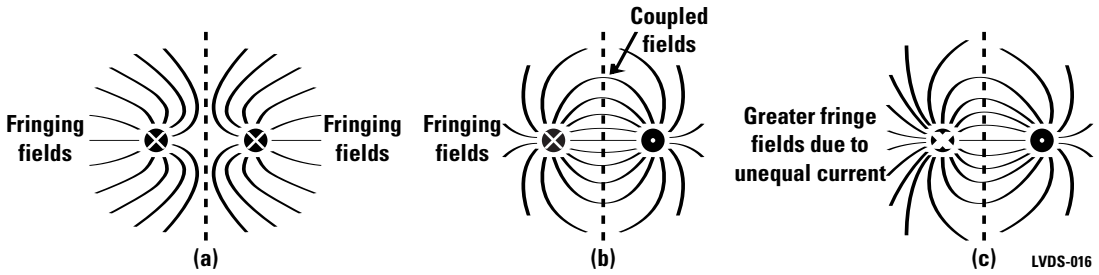


Figure 3.5. Even or common-mode signals (a), ideal equal and opposite odd mode signals (b), and unbalanced signals (c) on differential lines

Clearly, the voltages and currents of the two ("+" and "–") conductors are not always equal and opposite. For LVDS, the DC currents should never flow in the same direction as in Figure 3.5a, but factors can cause an imbalance in currents (c) vs. the ideal case in (b). When this imbalance happens, an excess of field fringing occurs since the field strength of the two conductors is unequal. The extra fringe fields can escape as TEM waves and lead to more EMI.

Similar effects can be seen in microstrip and stripline PCB traces shown in Figure 3.6. The ideal cases for microstrip and stripline are represented by (a) and (b). Here we see that the microstrip ground plane helps couple additional field lines from below, tying up more field lines and reducing EMI. Stripline almost completely shields the conductors and therefore can significantly decrease EMI, but has the penalty of slower propagation velocity (about 40% slower than microstrip), more PCB layers, additional vias, and difficulty in achieving 100Ω Z_O (Z_{DIFF}).

The use of shield traces with microstrip, as in Figure 3.6d, will result in more shielding without significantly impacting propagation velocity. Be careful to add the shield trace (preferably ground) on both sides of the pair (d). Running the shield trace – or any trace – on one side (c) creates an imbalance that can increase EMI. Ground trace shields should have frequent vias to the underlying ground plane at regular (<¼ wavelength) intervals, and should be placed at least 2S from the pair.

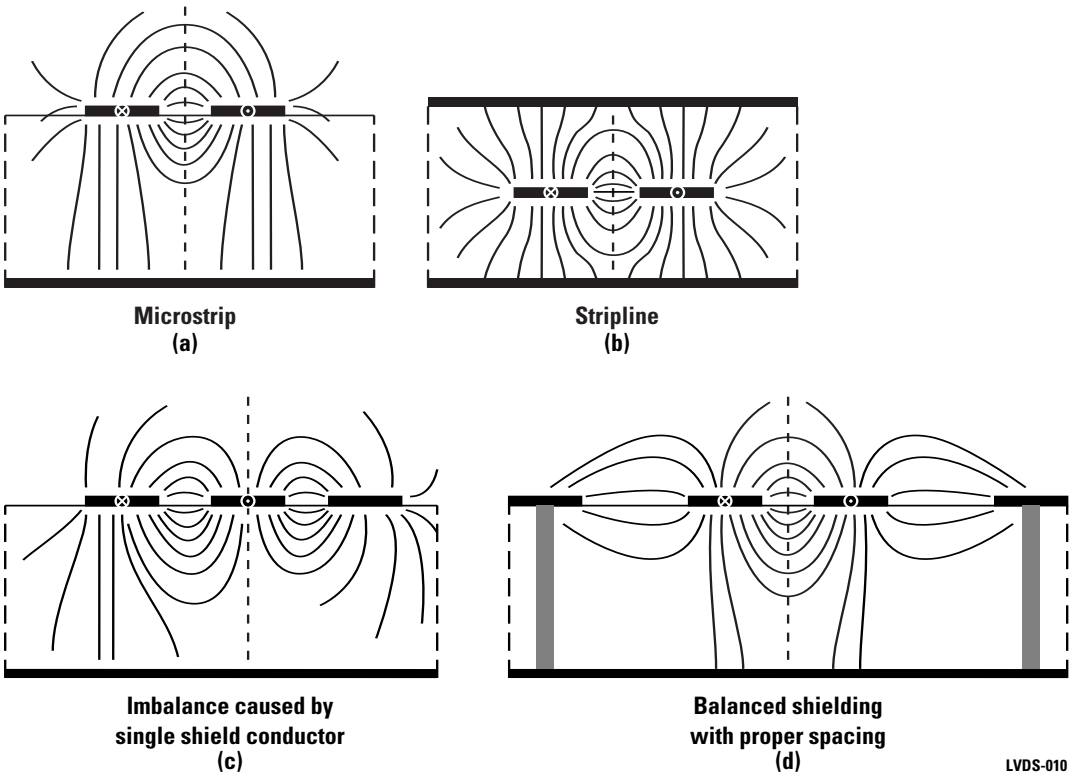


Figure 3.6. Ideal differential signals on microstrip (a) and stripline (b), negative effects of unbalanced shielding (c), and positive effects of balanced shielding (d)

3.2.2 Design practices for low EMI

As discussed in the preceding paragraphs, the two most important factors to consider when designing differential signals for low EMI are 1) close coupling between the conductors of each pair and 2) minimizing the imbalances between the conductors of each pair. Let us discuss close coupling first.

In order for sufficient coupling to occur, the space between the conductors of a pair should be kept to a minimum as shown in Figure 3.7. (Note that matched transmission impedance must also be maintained). Stripline power and ground planes/traces should not be closer than the distance between conductors. This practice will lead to closer coupling between the conductors, as compared with the coupling between each conductor and the power/ground planes. A good rule is to keep S < W, S < h, and x greater or equal to the larger of 2S or 2W. The best practice is to use the closest spacing, "S," allowed by your PCB vendor and then adjust trace widths, "W," to control differential impedance.

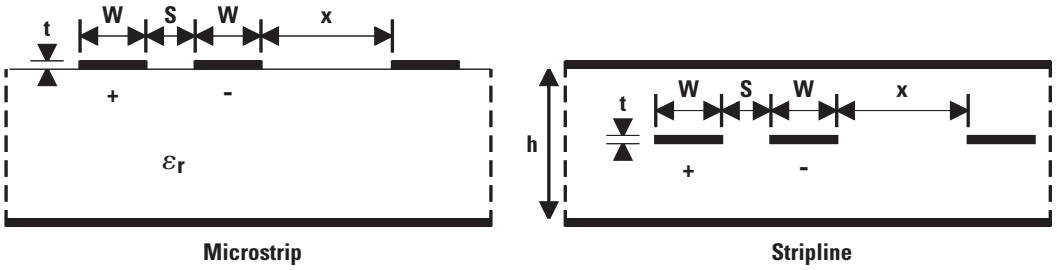


Figure 3.7. Coupling of differential traces

Minimize the distance between the "+" and the "-" signal to create sufficient coupling (canceling) of electromagnetic fields. As previously mentioned, close coupling between conductors of a pair reduces electromagnetic emissions. It also increases the immunity of the circuit to received electromagnetic noise. Noise coupled onto the conductors will do so as common-mode noise, which will then be rejected by the receiver. Since the differential pair is a current loop, minimizing conductor spacing also reduces the antenna loop.

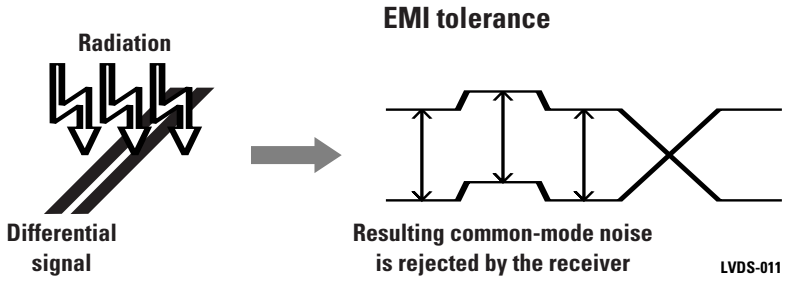


Figure 3.8. Close coupling not only reduces EM emissions, but improves EM immunity too

It is also important to minimize imbalances in order to reduce EMI. Complex interaction between objects of a system generate fields and are they are difficult to predict (especially in the dynamic case), but certain generalizations can be made. The impedance of your signal traces should be well controlled. If the impedances of two trace within a pair are different, it will lead to an imbalance. The voltage and fields of one signal will be different from its partner. This will tend to create more fringing fields and therefore more EMI as we have seen.

There is a basic rule to follow. Any unavoidable discontinuity introduced in proximity to differential lines should be introduced equally, to both members of the pair. Examples of discontinuities include: components, vias, power and ground planes, and PCB traces. Remember that the key word is balance.

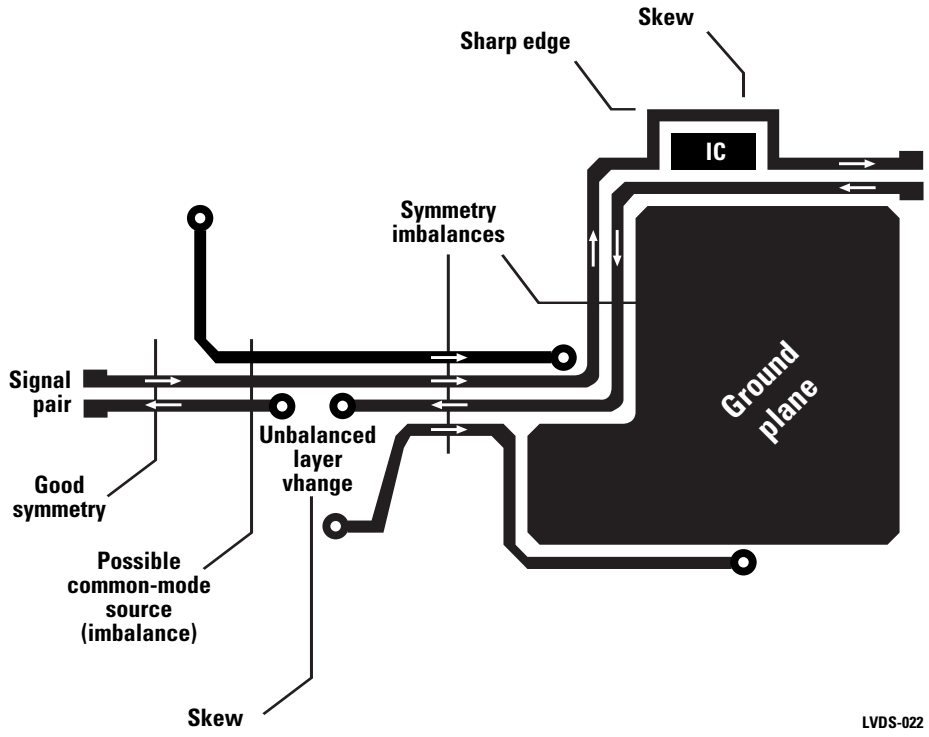


Figure 3.9. This PCB layout contains many sources of differential signal imbalance that will tend to increase electromagnetic radiation

Unfortunately unless you have an elaborate EMI lab, fields resulting from imbalances cannot easily be measured. Waveforms, however, are easy to measure. Fields are proportional to voltage/current amplitude at any given point in time. Any factors affecting the time (i.e., delay, velocity) and/or amplitude (i.e., attenuation) properties of the signals can increase EMI and can be seen on a scope. Figure 3.10 illustrates how waveforms – easily seen on a scope – can help predict far field EMI. First, the beneficial field canceling effects of ideal differential signals (b) vs. single-ended signals (a) are compared.

A real differential signal, however, is non-ideal and contains skew, unbalanced pulse widths and edge rates, common-mode noise, and unbalanced attenuation. These affect the relative amplitudes of the fields at any given moment, reducing the canceling effects of the differential signals, and potentially increasing EMI. Thus, the waveforms of one conductor of a pair should balance or mirror the other to minimize EMI.

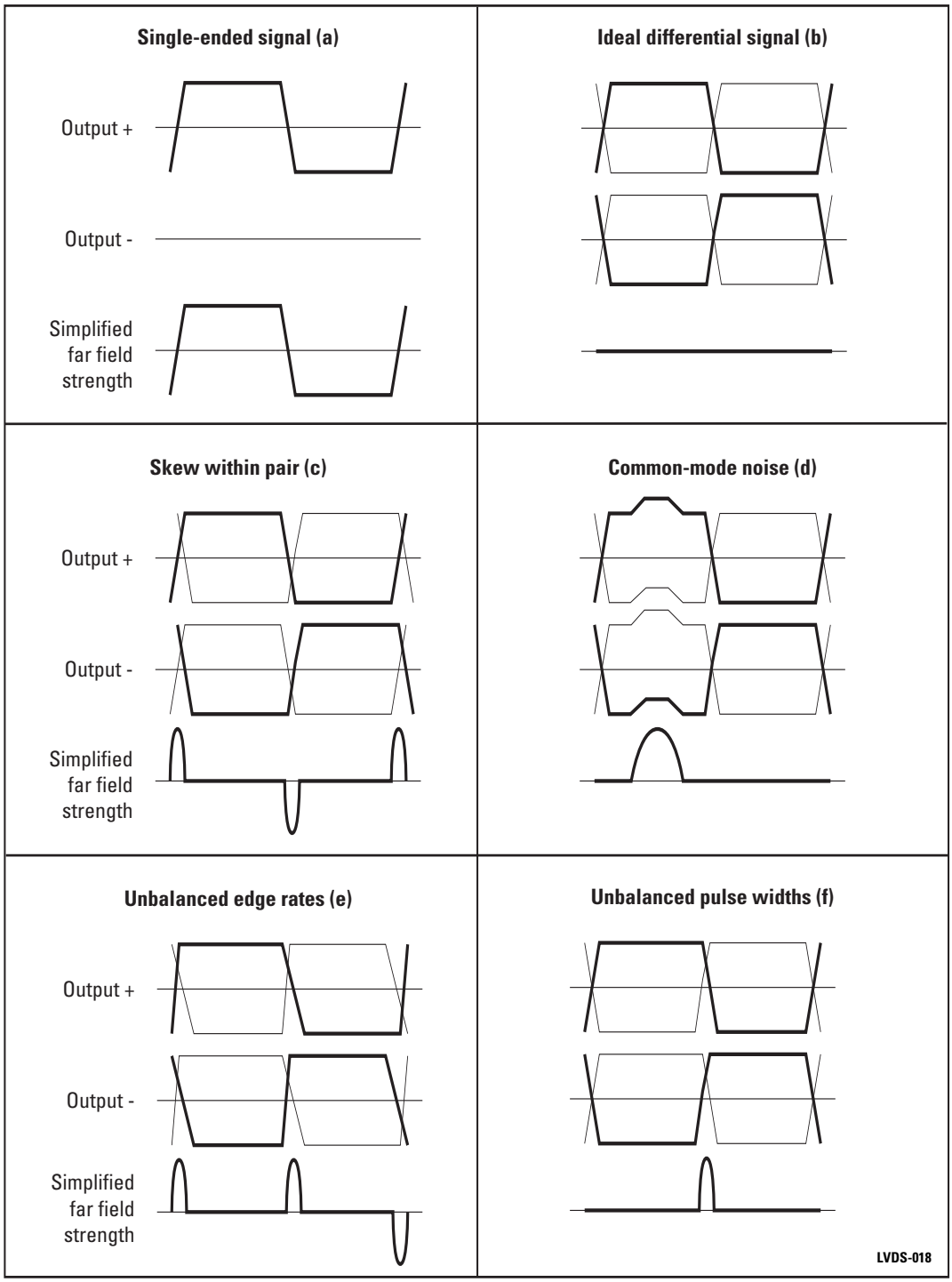


Figure 3.10. Diagram showing simplified far field radiation under various situations

3.2.3 EMI test results

The PCB setup shown below was used to examine the effects on EMI of closely coupled differential signals vs. uncoupled signals. The setup compares two sets of LVDS signals. One set contains pairs whose spacing is less than the trace width (S < W). The other set consists of pairs that are not closely coupled (S >> W). Note that the differential impedance of the widely spaced pair is still 100Ω.

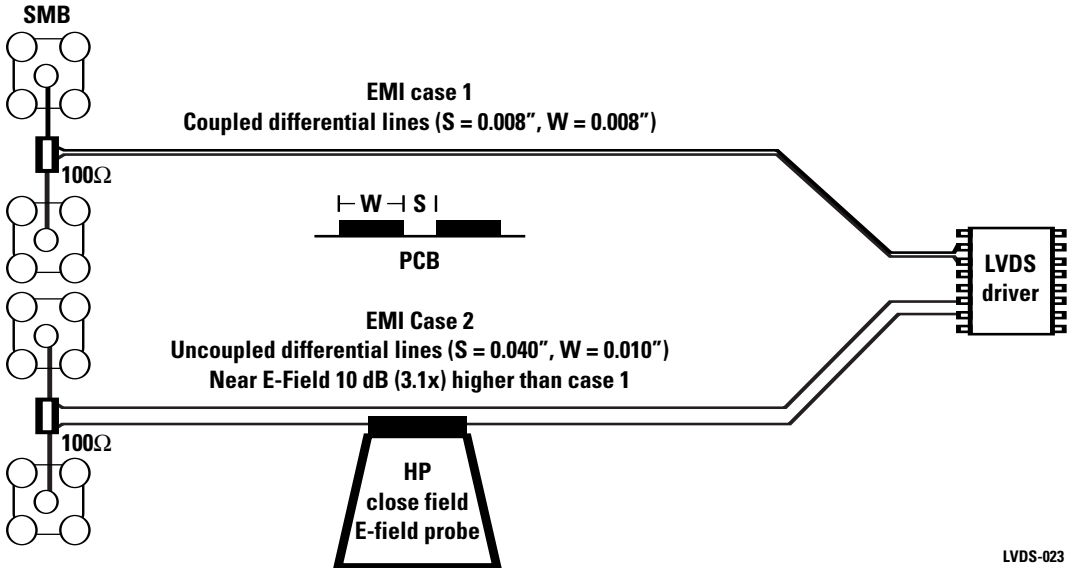


Figure 3.11. EMI test setup

Near (close) field electric field measurements were made for both cases while using a 32.5 MHz 50% duty cycle clock as the source. The plots in Figure 3.12 show the E-field strength results for case 2, the uncoupled case. The first plot shows the E-field strength over 200 MHz to 1 GHz. The second plot looks more closely at the frequencies between 30 MHz and 300 MHz. The electric field noise shows up as "spikes" which occur at harmonics of the input frequency.

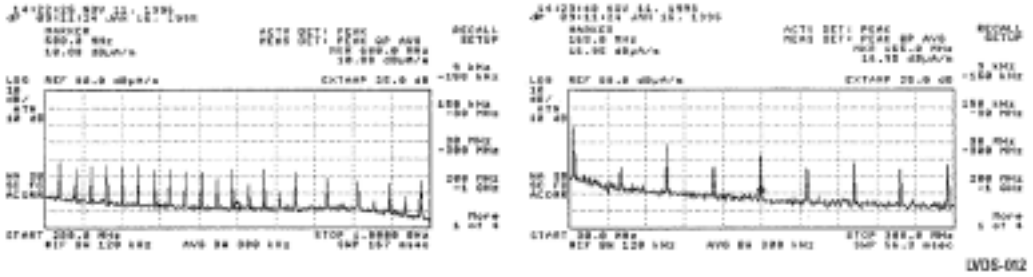


Figure 3.12. Near E-field strength for uncoupled signals
(Case 2): 200 MHz – 1 GHz (Case 2): 30 MHz – 300 MHz

The two plots in Figure 3.13 show the E-field strength for case 1 in which the differential pair is closely coupled. Notice that the harmonics are significantly reduced.

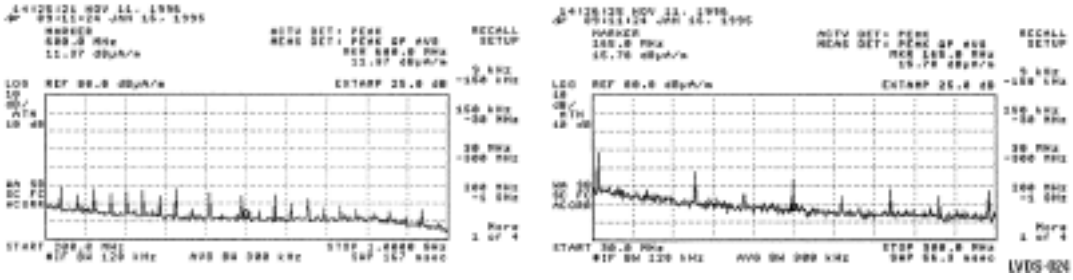


Figure 3.13 Near E-field strength for closely coupled signals
(Case 1): 200 MHz – 1 GHz (Case 1): 30 MHz – 300 MHz

In the far field, the EMI of the closely coupled pair should radiate much less due to the coupling of the electric fields. Even in the near field, however, the closely coupled pair generated much weaker electric fields. The electric field generated by the closely coupled pair was about 10 dB (>3x) lower than the field generated by the uncoupled pair.

This test illustrates two things:

1. Use of differential signals vs. single-ended signals can be used effectively to reduce emissions.
2. The EMI advantages of differential signs will be lost or greatly diminished unless the signals are closely coupled.

This test used uncoupled LVDS signals to represent single-ended signals. Most single-ended signals such as TTL or GTL, have a much greater swing and involve much greater currents, so their EMI is expected to be even greater than what is shown here.

3.2.4 Ground return paths

A conductor that carries current requires an opposite mirror current to return through some part of the system. This return current path will be the path of least resistance. For high-speed signals, the return current path will be the path of least inductance.

Since LVDS is differential, the signal current that flows in one conductor of a pair will flow back through the other conductor, completing the current-loop. This is ideal, because the current return antenna loop area is minimized since the traces of a pair are closely spaced. Real signals, however, will have some common-mode noise current, which must return also. This common-mode current will be capacitively coupled to ground and return to the driver through the path of least inductance. Therefore, a short ground current return path is needed between the driver and receiver in differential systems.

On PCBs, the best current return path is a uniform, unbroken ground plane beneath the LVDS signals. The ground plane will allow the common-mode (even mode) current to return directly under the LVDS signals. This closely coupled path is the path of least inductance and means that the current loop area is minimized.

Similarly, in cables, a ground return wire or wires should be used between driver and receiver. This allows the return path to be in close proximity to the signal pairs reducing the current loop area. (See Chapter 6 on Cables).

3.2.5 Cable shielding

Shielding is an effective way to reduce EMI. Shielding should be connected directly to both driver enclosure and receiver enclosure when possible. Shields are not designed to handle significant ground return currents, so it may be necessary to construct a filter network which isolates the shield from ground at one end (See Chapter 6).

3.2.6 EMC conclusion

To take advantage of the inherent low EMI properties of LVDS, designers should ensure the conductors of each pair are (1) closely coupled and (2), well-balanced. Impedance, both single-ended and differential, should be controlled and matched.

3.3 AC-coupling

Why would you want to AC-couple a signal?

1. To change the DC bias voltage when interfacing logic families with different input thresholds (such as optical systems where LVDS and PECL are used), or
2. To protect drivers from possibly getting shorted when used in a removable interface (such as on cards used in network switches and routers), or
3. To prevent DC currents flowing between systems with different ground potentials

If your application meets one of these requirements and you are using encoded data, use AC-coupling.

AC-coupling works best with encoded data that provides an equal number of ones and zeros (a DC-balanced signal). Just to name a few, 50% duty-cycle clocks, 8b/10b coding, and Manchester-coded data are all examples of DC-balanced signals. DC-balanced data should be used when AC-coupled.

For signals with good DC-balancing, the useful spectral content of the data usually has a low frequency cutoff, and it is possible to pass the information with minimal degradation in content. However, for any signal passed through an AC-coupling circuit, you should expect a small portion of the signal to be filtered out.

When AC-coupling is used, the DC common-mode bias voltage used in LVDS and many other logic families is lost. Although many devices have a wide common-mode operating voltage range, this should be verified in the device's datasheet. For devices limited in common-mode operating range, a simple bias circuit can be used to properly bias the signal.

The most common method of AC-coupling is to use a DC-blocking capacitor. For high-speed designs, the smallest available package should be used. This will help minimize degradation of the signal due to package parasitics.

LVDS-091

Figure 3.14. AC-coupling

To find the appropriate capacitor value to use, you can use the following equation as a rough approximation:

$$C = \frac{\left(7.8 \times N \times Tb\right)}{R}$$

Tb = bit period
R = impedance
N = the maximum number of consecutive identical bits

Every AC-coupled signal will have some droop in amplitude when passed through a capacitor. The equation listed above takes into account a 0.25 dB droop.

The most commonly used capacitor values found in high-speed applications are 0.1 µF and 0.01 µF capacitors. These capacitors are easy to find and have sufficient bandwidth to support most high-speed data rates.

For applications where edge rates are very fast, placing the AC-coupling capacitors closer to the receiver inputs may provide better results since edge rates will be slower.

In general, for logic interconnects within the same PCB, a simple DC-coupled interface is best. If AC-coupling must be used, then make sure that DC-balanced data is used.