Chapter 2
Using LVDS

2.1 Why low-swing differential?

The differential data transmission method used in LVDS is less susceptible to common-mode noise than single-ended schemes. Differential transmission uses two wires with opposite current/voltage swings instead of the one wire used in single-ended methods to convey data information. The advantage of the differential approach is that if noise is coupled onto the two wires as common-mode (the noise appears on both lines equally) and is thus rejected by the receivers, which looks at only the difference between the two signals. The differential signals also tend to radiate less noise than single-ended signals due to the canceling of magnetic fields. In addition, the current-mode driver is not prone to ringing and switching spikes, further reducing noise.

Because differential technologies such as LVDS reduce concerns about noise, they can use lower signal voltage swings. This advantage is crucial, because it is impossible to raise data rates and lower power consumption without using low voltage swings. The low swing nature of the driver means data can be switched very quickly. Since the driver is also current-mode, very low – almost flat – power consumption across frequency is obtained. Switching spikes in the driver are very small, so that ICC does not increase exponentially as switching frequency is increased. Also, the power consumed by the load (3.5 mA x 350 mV = 1.2 mW) is very small in magnitude.

2.1.1 A quick comparison between differential signaling technologies

Table 2.1. Comparison of LVDS with RS-422 and PECL

Parameter	RS-422	PECL	LVDS
Differential driver output voltage	±2 to ±5V	±600 to 1000 mV	±250-450 mV
Receiver input threshold	±200 mV	±200 to 300 mV	±100 mV
Data rate	<30 Mbps	>400 Mbps	>400 Mbps

Parameter	RS-422	PECL	LVDS*
Supply current quad driver (no load, static)	60 mA (max)	32 to 65 mA (max)	8.0 mA
Supply current quad receiver (no load, static)	23 mA (max)	40 mA (max)	15 mA (max)
Propagation delay of driver	11 ns (max)	4.5 ns (max)	1.7 ns (max)
Propagation delay of receiver	30 ns (max)	7.0 ns (max)	2.7 ns (max)
Pulse skew (driver or receiver)	N/A	500 ps (max)	400 ps (max)

*LVDS devices noted are DS90LV047A/048A

Table 2.1 compares basic LVDS signaling levels with those of PECL and shows that LVDS has half the voltage swing of PECL. LVDS swings are one-tenth of RS-422 and also traditional TTL/CMOS levels.

Another voltage characteristic of LVDS is that the drivers and receivers do not depend on a specific power supply, such as 5V. Therefore, LVDS has an easy migration path to lower supply voltages such as 3.3V or even 2.5V, while still maintaining the same signaling levels and performance. In contrast, technologies such as ECL or PECL have a greater dependence on the supply voltage, which make it difficult to migrate systems utilizing these technologies to lower supply voltages.

2.1.3 Easy termination

The transmission medium must be terminated to its characteristic differential impedance to complete the current loop and terminate the high-speed (edge rates) signals. That requirement is the same, whether the LVDS transmission medium consists of a cable or of controlled impedance traces on a printed circuit board. If the medium is not properly terminated, signals reflect from the end of the cable or trace and may interfere with succeeding signals. Proper termination also reduces unwanted electromagnetic emissions and provides the optimum signal quality.

To prevent reflections, LVDS requires a terminating resistor that is matched to the actual cable or PCB trace's differential impedance. Commonly, 100Ω media and terminations are employed. This resistor completes the current loop and properly terminates the signal. This resistor is placed across the differential signal lines as close as possible to the receiver input.

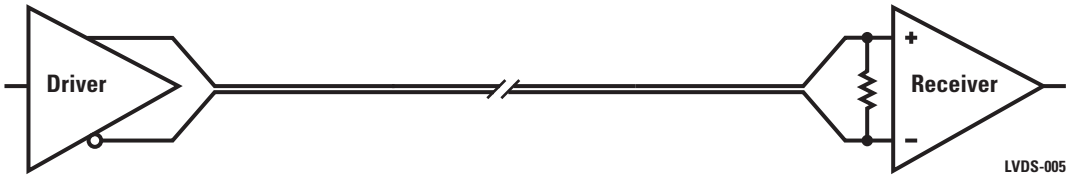

Figure 2.1. LVDS termination

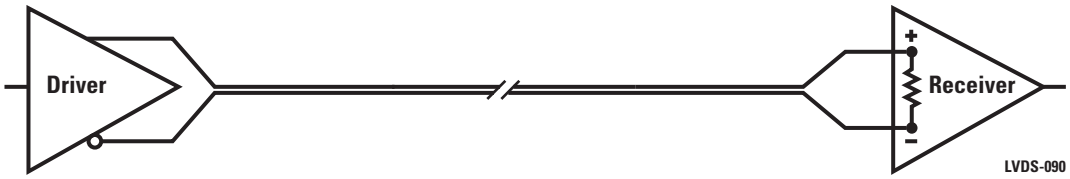

Figure 2.1a. Internal termination

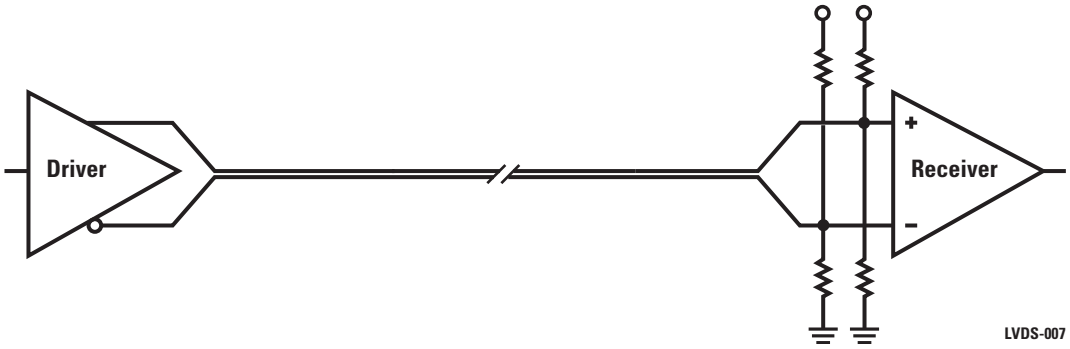

Figure 2.2. PECL termination

The simplicity of the LVDS termination scheme makes it easy to implement in **most** applications. ECL and PECL require a more complex termination than the one-resistor solution for LVDS. PECL connections must meet several requirements at the same time. The receivers must be biased to around 1V below V_{EE}. The transmission lines must be terminated and there must be a resistive path for DC current to flow from the driver. The example in the Figure 2.2 shows an implementation with a Thévenin network.

2.1.4 Maximum switching speed

Maximum switching speed of an LVDS Interface is a complex question, and its answer depends upon several factors. These factors are the performance of the line driver (edge rate) and receiver, the bandwidth of the media, and the required signal quality for the application.

Since the driver outputs are very fast, the limitation on speed is commonly restricted by:

1. How fast TTL data can be delivered to the driver – in the case of simple PHY devices that translate a TTL/CMOS signal to LVDS (i.e. DS90LV047A)
2. Bandwidth performance of the selected media (cable) – type and length dependent

For example, the factor that limits the speed of the DS90LV047A LVDS driver is the rate that TTL data can be delivered.

National's Channel Link devices (SerDes) capitalize on the speed mismatch between TTL and LVDS by serializing the TTL data into a narrower LVDS data stream (more about this later.)

2.1.5 Saving power

LVDS technology saves power in several important ways. The power dissipated by the load (the 100Ω termination resistor) is a mere 1.2 mW. In comparison, an RS-422 driver typically delivers 3V across a 100Ω termination. It dissipates 90 mW of power — 75x more than LVDS.

LVDS devices are implemented in CMOS processes, which provide low static power consumption. The circuit design of the drivers and receiver require roughly one-tenth the power supply current of PECL/ECL devices.

Aside from the power dissipated in the load and static I_{DD} current, LVDS also lowers system power through its current-mode driver design. This design greatly reduces the frequency component of I_{DD}. The I_{DD} vs. frequency plot for LVDS is virtually flat between 10 MHz and 100 MHz. The quad device, DS90C031/2 uses less than 50 mA total, for driver and receiver at 100 MHz. Compare this to TTL/CMOS transceivers whose dynamic power consumption increases exponentially with frequency.

2.1.6 LVDS configurations

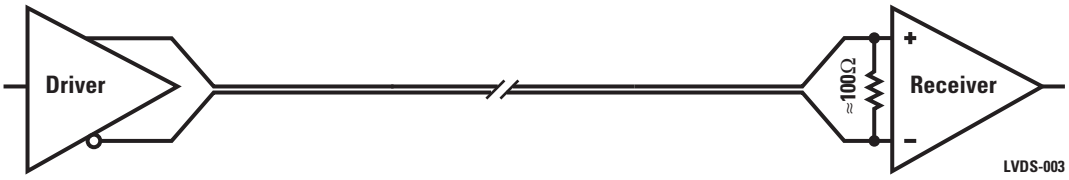

Figure 2.3. Point-to-point configuration

LVDS drivers and receivers are commonly used in a point-to-point configuration, as shown in Figure 2.3. Dedicated point-to-point links provide the best signal quality due to the clear path they provide. In this configuration, LVDS is capable of transmitting high-speed signals over substantial lengths of cable while using remarkably little power and generating very little noise. However, other topologies/configurations are also possible.

When the system architect is more interested in minimizing the number of interconnects than in raw performance, LVDS is a great technology to consider. LVDS is well suited to bi-directional signaling and bus applications.

The configuration shown in Figure 2.4 allows bi-directional communication over a single twisted pair. Data can flow in only one direction at a time. The requirement for two terminating resistors reduces the signal (and thus the differential noise margin), so this configuration should be considered only where noise is low and transmission distance is short (<10m). Chapter 5 contains an overview of Bus LVDS devices, which are designed for double termination loads and provide full LVDS compatible levels.

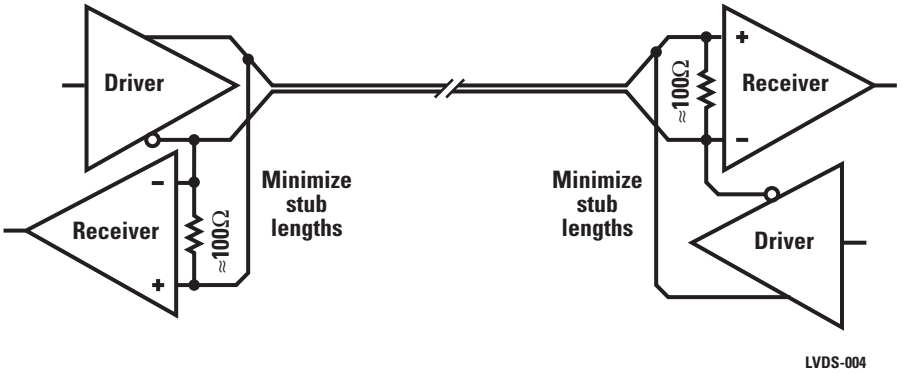

Figure 2.4. Bi-directional half-duplex configuration

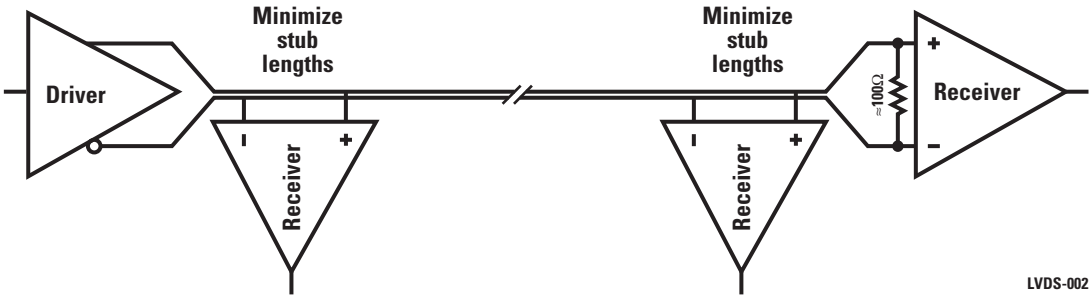

Figure 2.5. Multidrop configuration

A multidrop configuration connects multiple receivers to a driver. These are useful in data distribution applications. They can also be used if the stub lengths are as short as possible (less than 20 mm – application dependent). Section 5.2 also covers multidrop applications.

2.2 An economical interface

LVDS is a cost-effective solution:

1. National's LVDS CMOS implementations provide better price/performance ratios as compared to custom solutions on elaborate processes.
2. High performance can be achieved using common, off-the-shelf CAT3 cable and connectors, and/or FR4 material.
3. LVDS consumes very little power, thereby reducing or eliminating power supplies, fans, and other peripherals.
4. LVDS is a low-noise and noise-tolerant technology, minimizing problems.

5. LVDS transceivers are cost-efficient products that can also be integrated around digital cores providing a higher level of integration.
6. LVDS moves data much faster than TTL, so multiple TTL signals can be serialized or multiplexed into a single LVDS channel, reducing board, connectors, and cabling costs.

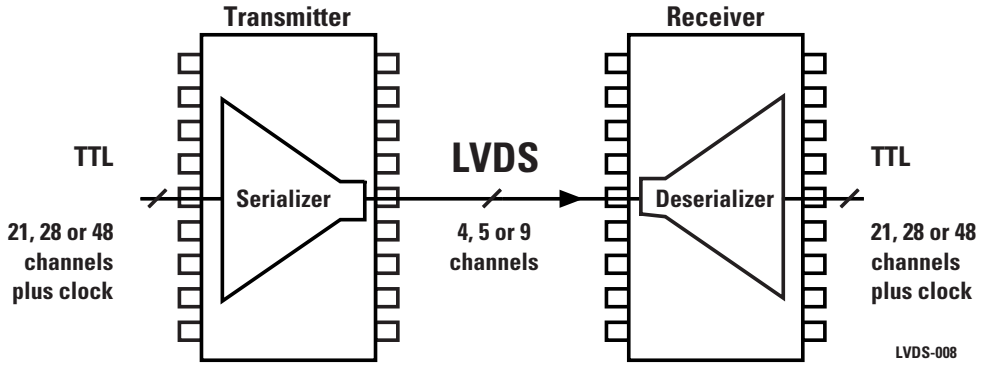

Figure 2.6. National's Channel Link chipsets convert a TTL bus into a compact LVDS data stream and back to TTL

In fact, in some applications, the Printed Circuit Board (PCB), cable, and connector cost savings greatly overshadow any additional silicon costs. Smaller PCBs, cables, and connectors also result in a much more ergonomic, user-friendly system.

2.3 Embedded LVDS I/O in FPGAs and ASICs

The latest Field Programmable Gate Arrays (FPGAs) and Application-Specific Integrated Circuits (ASICs) are moving into the Bus LVDS application space. These new product offerings have enhanced LVDS drive characteristics designed to be more compatible with a typical multidrop topology. There are advantages and disadvantages to these FPGA platforms over discrete solutions. For example, fewer ICs on a PCB generally lead to simpler designs with fewer interconnects, and integrated solutions are sometimes necessary when board size is a concern.

System designers should weigh these advantages against the compromises they will be making in signal integrity. They should also be aware that discrete solutions are typically more cost effective than integrated FPGA platforms.

Several major design challenges still need to be addressed in order to successfully design a robust backplane interface.

1. Stub length: This is the trace length from the backplane trace, through the backplane connector to the Bus LVDS receiver. Long stubs in multidrop and multipoint buses lead to poor signal integrity.
2. ESD protection: Resistance to electrostatic discharge (ESD) improves the reliability of system boards during insertion and removal events.
3. Capacitive loading: This is the capacitance seen at the I/O of an active device. High capacitance leads to low impedance and low noise margin.

2.3.1 Stub length

Reductions in stub length are one of the best ways to improve the signal integrity of a multidrop or multipoint bus.

As a rule of thumb, stub lengths should be no longer than 2.5 cm or 1 in., (see Section 5.3.3) It is possible to design with longer stub trace lengths, but bus noise from signal reflections limit system performance.

A board designer does not always have a great deal of flexibility with respect to the placement of the FPGA or ASIC on his board. If an LVDS receiver is integrated into a larger IC, its placement depends on a number of factors. These factors tend to conflict with the signal integrity related needs of the receiver being near the backplane connector. The designer's ability to control trace lengths between the connector and the ICs inputs are further diminished when an FPGA contains a large number of high-speed I/Os.

A discrete solution enables the placement of LVDS I/Os for optimum signal integrity. This is one less factor that the board designer needs to worry about as the balances the compromises over the placement of the larger ICs.

2.3.2 ESD protection

Anytime a board or cable is handled or plugged into a system, the opportunity exists for ESD events to occur. Integrated circuits mounted to the external interfaces on the board are most likely to be in the ESD event path. Selecting devices with high ESD tolerances will increase the reliability of the board. It is desirable to isolate and protect sensitive programmable devices from the stresses associated with ESD events with interface devices from National.

Example HBM ESD protection levels

DS90LV047	>10 kV
DS90LV048	>10 kV
DS90CP22	>5.0 kV
DS92LV090	>4.5 kV
DS92LV040	>4.0 kV

Many of the FPGAs and PLDs pass HBM ESD tests in the range of 1000V to 2000V. For these designs requiring more protection, a lower-cost, stand-alone LVDS IC provides this protection on behalf of the high-end ICs.

2.3.3 Capacitive loading

Plug-in cards present capacitive loads on backplane traces. As the loading on the backplane bus traces increases, their impedance drops. The drop in impedance reduces the available noise margin and the reliability of operation in the design.

The three factors on a plug-in card that contribute to the capacitive loading on a bus are the:

- Bulk capacitance load resulting from the connector
- PCB trace
- I/O structure of the device

In a good design the connector contributes 2 pF to 3 pF, the trace contributes 2 pF to 3 pF, and the device contributes 4 pF to 5 pF. The total load in such a design is around 10 pF.

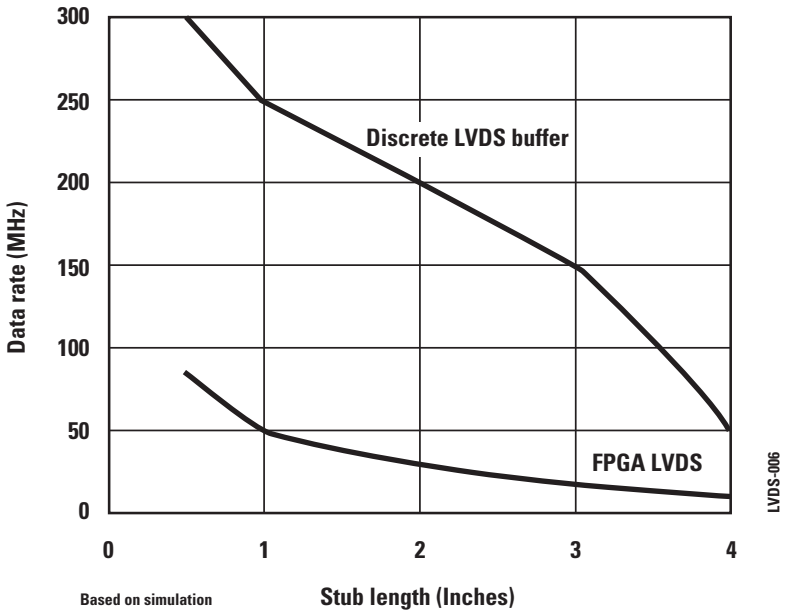

Figure 2.7. Comparison of backplane performance between integrated and discrete solutions

The flexibility of programmable devices comes at the cost of capacitance. National Bus LVDS products have an I/O capacitance of 5 pF. The I/O capacitance of a programmable device is approximately double or 10 pF. This increase in capacitance will lower the loaded bus impedance, thereby reducing the available noise margin and lowering the reliability of operation in the design.

Figure 2.7 is the result of a simulation comparing the performance of a discrete solution with the performance of an FPGA with embedded LVDS I/Os. The data rates that can be supported by the discrete solution are several times higher, which is mostly a result of lower capacitance in the I/Os.

2.3.4 Cable drive capability

Today's system requirements often define high-speed serial intra- and inter-chassis connections. This makes the ability to drive cables an important aspect of I/O performance. Comparing LVDS outputs typical of advanced FPGAs available today with the new generation of LVDS devices shows a substantial difference in capabilities.

Figure 2.8 shows the results of an experiment, comparing the abilities of different circuits to drive cables. Data taken on the FPGA was done with minimal internal logic. The only structures used in this optimized setup for the FPGA were the input stage, internal buffering and the output stage. If more internal logic is switching inside the FPGA, then there is more noise on the LVDS I/O signals. The National device was fully operational with all outputs switching at the input frequency.

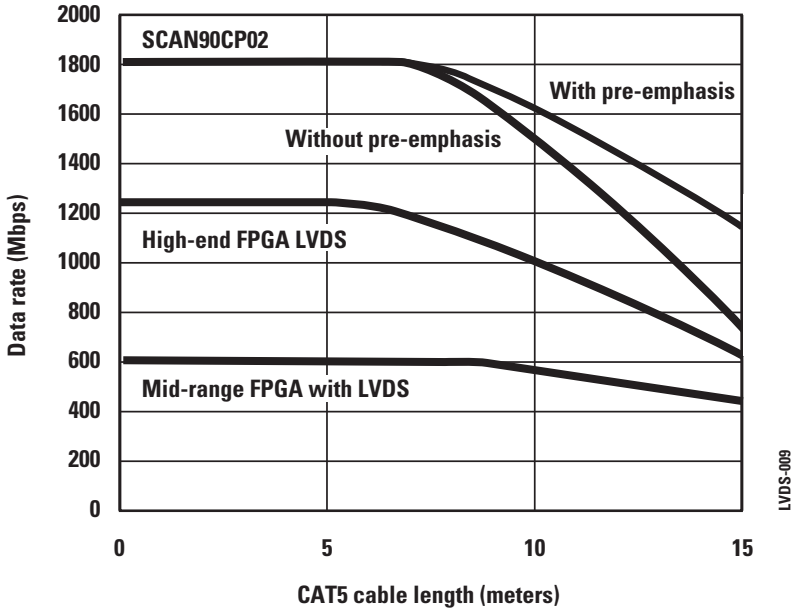

Figure 2.8. Comparison of cable-drive performance between integrated and discrete solutions

The discrete LVDS devices have I/Os that have been optimized for driving cables. Figure 2.8 clearly demonstrates that their performance is superior to the general-purpose I/Os of the FPGA.

2.3.5 Flexibility

FPGAs with high-speed LVDS I/Os tend to be more expensive than similar devices with lower speed I/Os. The designer might realize value from the more expensive FPGA when all or most of the high-speed I/Os are being used. It is often the case, however, that the number of I/Os does not closely match the requirements of the design. When that happens, much of the high-value performance that the designer is paying for goes to waste.

There are many discrete LVDS products on the market, with a wide range of interface configurations and bus widths. It is much more likely that a designer will find a suitable LVDS interface on a discrete component, than he will on an FPGA. A solution more closely suited to a design's minimum requirements will certainly be more cost effective.

2.4 National's wide range of LVDS solutions

National offers LVDS technology in several forms. For example, National's 5V DS90C031/ DS90C032 and 3V DS90LV047A/DS90LV048A quad line driver/receiver devices implement LVDS technology in discrete packages for general-purpose use. This family of basic line drivers and receivers also contains single, dual and quad footprints.

For the specialized task of connecting laptop and notebook computers to their high-resolution LCD screens, National offers the Flat Panel Display Link (FPD-Link) and LVDS Display Interface (LDI) devices. These parts provide a high bandwidth, low power, small size, interface enabling XGA/SXGA/UXGA and beyond displays for notebook and monitor applications.

Another more generalized use of LVDS is in the National channel link family, which can convert 21, 28, or 48 bits of parallel data to 3, 4, or 8 channels of LVDS serial data, plus LVDS clock. These devices provide fast data pipes (up to 6.4 Gbps throughput) and are well suited for high-speed network hubs, router applications, or anywhere a low-cost, high-speed link is needed. Their serializing nature provides a greater price/performance ratio as cables and connector physical size are greatly reduced.

Bus LVDS is an extension of the LVDS line drivers and receivers family. They are specifically designed for multidrop and multipoint applications where the bus is terminated at both ends. They may also be used in heavily loaded backplanes where the effective impedance is lower than 100Ω. In this case, the drivers may see a load in the 30Ω to 50Ω range. Bus LVDS drivers provide about 10 mA of output current so that they provide LVDS swings with heavier termination loads. Transceivers and repeaters are currently available in this product family.

The 18-, 16-, and 10-bit serializer and deserializer families of devices are available that embed and recover clock and data from a single serial stream. These chipsets also provide a high level of integration with on-chip clock recovery circuitry. All deserializers provide a random data lock capability, an industry first. The deserializer can be hot-plugged in to a live data bus and does not require sending special characters for PLL training.

Special functions are also being developed using LVDS technology. This family provides additional functionality over the simple PHY devices. Currently a special low-skew clock transceiver with 6 CMOS outputs is available (DS92CK16) along with a line of crosspoint switches.

2.5 Conclusion

LVDS technology solutions eliminate the trade-offs in speed, power, noise, and cost for high-performance data transmission applications. In doing so, LVDS not only achieves great benefits in existing applications, but opens the door to many new ones.