Chapter 1
Introduction to LVDS

Low-Voltage Differential Signaling (LVDS) is a new technology addressing the needs of today's high performance data transmission applications. The LVDS standard is becoming the most popular differential data transmission standard in the industry. This is driven by two simple features: "Gigabits @ milliwatts!"

LVDS delivers high data rates while consuming significantly less power than competing technologies. In addition, it brings many other benefits, which include:

- Low-voltage power supply compatibility
- Low noise generation
- High noise rejection
- Robust transmission signals
- Ability to be integrated into system level ICs

LVDS technology allows products to address high data rates ranging from 100's of Mbps to greater than 2 Gbps. For all of the above reasons, it has been deployed across many market segments wherever the need for speed and low power exists.

1.1 The trend to LVDS

Consumers are demanding more realistic visual information in the office and in the home. This drives the need to move video, 3D graphics and photo-realistic image data from cameras to PCs and printers through LAN, phone, and satellite systems to home set-top boxes and digital VCRs. Solutions exist today to move this high-speed digital data both very short and very long distances, on printed circuit boards (PCB) and across fiber or satellite networks. Moving this data from board-to-board or box-to-box however, requires an extremely high-performance solution that consumes a minimum of power, generates little noise, (must meet increasingly stringent FCC/CISPR EMI requirements) is relatively immune to noise, and is cost-effective.

National Semiconductor first introduced LVDS as a standard in 1994. National recognized that the demand for bandwidth was increasing at an exponential rate while users also desired low power dissipation. This exceeded the speed capabilities of RS-422 and RS-485 differential transmission standards. While Emitter Coupled Logic (ECL or PECL) was available at the time, it is incompatible with standard logic levels, uses negative power rails, and leads to high chip-power dissipation. These factors limited its wide spread acceptance.

LVDS is differential, using two signal lines to convey information. While sounding like a penalty, this is actually a benefit. The cost is two traces (or conductors) to convey a signal, but the gain is noise tolerance in the form of common-mode rejection.

Signal swing can be dropped to only a few hundred millivolts because the signal-to-noise rejection has been improved. The small swing enables faster data rates since the rise time is now so much shorter.

1.2 Getting speed with low noise and low power

LVDS is a low swing, differential signaling technology, which allows single channel data transmission at hundreds or even thousands of Megabits per second (Mbps). Its low swing and current-mode driver outputs create low noise and provide very low power consumption across a wide range of frequencies.

1.2.1 How LVDS works

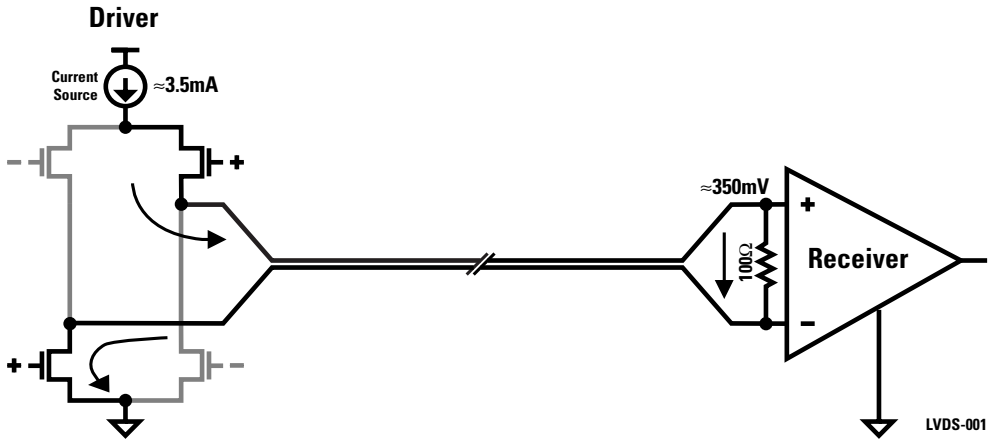

Figure 1.1. Simplified diagram of LVDS Driver and receiver connected via 100Ω differential impedance media

LVDS outputs consist of a current source (nominal 3.5 mA) that drives the differential pair lines. The basic receiver has a high DC input impedance, so the majority of driver current flows across the 100Ω termination resistor generating about 350 mV across the receiver inputs. When the driver switches, it changes the direction of current flow across the resistor, thereby creating a valid "one" or "zero" logic state.

1.2.2 The LVDS Standard

LVDS is currently standardized by the TIA/EIA (Telecommunications Industry Association/Electronic Industries Association) ANSI/TIA/EIA-644-A (LVDS) Standard

The generic (multi-application) LVDS standard, ANSI/TIA/EIA-644-A, began in the TIA Data Transmission Interface committee TR30.2 in 1995. It was revised and published as ANSI/TIA/EIA-644-A in 2001. The ANSI/TIA/EIA standard defines driver output and receiver input characteristics, thus it is an electrical-only standard. It does not include functional specifications, protocols or even complete cable characteristics since these are application dependent. ANSI/TIA/EIA-644-A is intended to be reference by other standards that specify the complete interface (i.e., connectors, protocol). This allows it to be easily adopted into many applications.

ANSI/TIA/EIA-644-A (LVDS) standard

Table 1.1. ANSI/TIA/EIA-644 (LVDS) standards

Parameter	Description	Min	Max	Units
V_{OD}	Differential output voltage	247	454	mV
V_{OS}	Offset voltage	1.125	1.375	V
V_{OD}	|Change to V_{OD}|		50	|mV|
V_{OS}	|Change to V_{OS}|		50	|mV|
I_{SA}, I_{SB}	Short circuit current		24	|mA|
tr/tf	Output rise/fall times (200 Mbps)	0.26	1.5	ns
	Output rise/fall times (<200 Mbps)	0.26	30% of tui†	ns
I_{IN}	Input current		20	|µA|
V_{TH}	Receive threshold voltage		+100	mV
V_{IN}	Input voltage range	0	2.4	V

† tui is unit interval (i.e. bit width).
Note: Actual datasheet specifications may be significantly better.

(See Appendix A for a detailed explanation of these parameters.)

The ANSI/TIA/EIA standard recommends a maximum data rate of 655 Mbps (based on a limiting set of assumptions) and it also provides a theoretical maximum of 1.923 Gbps based on a loss-less medium. This allows the referencing standard to specify the maximum data rate required depending upon required signal quality and media length/type.

The standard also covers minimum media specifications, failsafe operation of the receiver under fault conditions, and other configuration issues such as multiple receiver operation.

The ANSI/TIA/EIA-644 standard was approved in November 1995. National held the editor position for this standard. The 644 spec has been revised to include additional information about multiple receiver operation. The revised spec was published in February 2001 with the title TIA-644-A.

There was another LVDS standard from an IEEE project. This standard came out of an effort to develop a standard for purposes such as linking processors in a multiprocessing system or grouping workstations into a cluster. This Scalable Coherent Interface (SCI) program originally specified a differential ECL interface that provided the high data rates required but did not address power concerns or integration.

The low-power SCI-LVDS standard was later defined as a subset of SCI and is specified in the IEEE 1596.3 standard. The SCI-LVDS standard also specifies signaling levels (electrical specifications) similar to the ANSI/TIA/EIA-644-A standard for the high-speed/low-power SCI physical layer interface. The standard also defines the encoding for packet switching used in SCI data transfers. The IEEE 1596.3 standard was approved in March 1996, but expired 5 years later and was not renewed. National chaired this standardization committee.

In the interest of promoting a wider standard, no specific process technology, medium, or power supply voltages are defined by either standard. This means that LVDS can be implemented in CMOS, GaAs or other applicable technologies, migrate from 5V to 3.3V to sub-3V supplies, and transmit over PCB traces or cable, thereby serving a broad range of applications in many industry segments.

1.3 LVDS ICs

A wide variety of LVDS Interface devices is available from a range of suppliers. LVDS is most commonly found in the following types of ICs.

Line drivers/receivers

These devices are typically used to convert single-ended signals, such as LVCMOS into a format more suitable for transmission over a backplane or a cable. They are available in single-channel as well as multi-channel configurations.

SerDes

Serializer/deserializer pairs are used to multiplex a number of low-speed CMOS lines and to transmit them as a single channel running at a higher data rate. SerDes ICs are typically used to reduce the number of connector pins or lines within cables and backplanes. SerDes functions are being embedded into large and complex ICs in order to reduce the number of I/Os on the IC package.

Switches

Switching architectures are favored over bus architectures when data-rates are high. As a consequence, switches tend to operate at high data rates. LVDS is a common choice for the I/Os on these IC's. Switches can be used for clock distribution. LVDS is one of the most suitable signaling standards for clocks of any frequency because of reliable signal integrity.

1.4 Bus LVDS (BLVDS)

Bus LVDS, sometimes called BLVDS, is a new family of bus interface circuits based on LVDS technology, specifically addressing multipoint cable or backplane applications. it differs from standard LVDS in providing increased drive current to handle double terminations that are required in multipoint applications.

Bus LVDS addresses many of the challenges faced in a high-speed bus design.

- Bus LVDS eliminates the need for a special termination pull-up rail
- It eliminates the need for active termination devices
- Utilizes common power supply rails (3.3V or 5V)
- Employs a simple termination scheme
- Minimizes power dissipation in the interface devices
- Generates little noise
- Supports live insertion of cards
- Drives heavily loaded multi-point busses at 100's of Mbps

The Bus LVDS products provide designers with new alternatives for solving high-speed, multi-point bus interface problems. Bus LVDS has a wide application space ranging from telecom infrastructure and datacom applications where card density demands high-performance backplanes to industrial applications where long cable length and noise immunity are useful.

Refer to Chapter 5 for more details on Bus LVDS.

1.5 LVDS applications

The high-speed and low power/noise/cost benefits of LVDS make it a compelling technology, that fits into a broad range of applications. Some examples are listed in Table 1.2.

Table 1.2. Sample applications

PC/computing	Telecom/datacom	Consumer/commercial
Flat-panel displays	Switches	Home/commercial video links
Monitor link	Add/drop multiplexers	Set top boxes
SCI processor interconnect	Hubs	In-flight entertainment
Printer engine links	Routers	Game displays/control
Digital Copiers	Access systems	
System clustering	Broadband concentrators	
Multimedia peripheral links	Base stations	