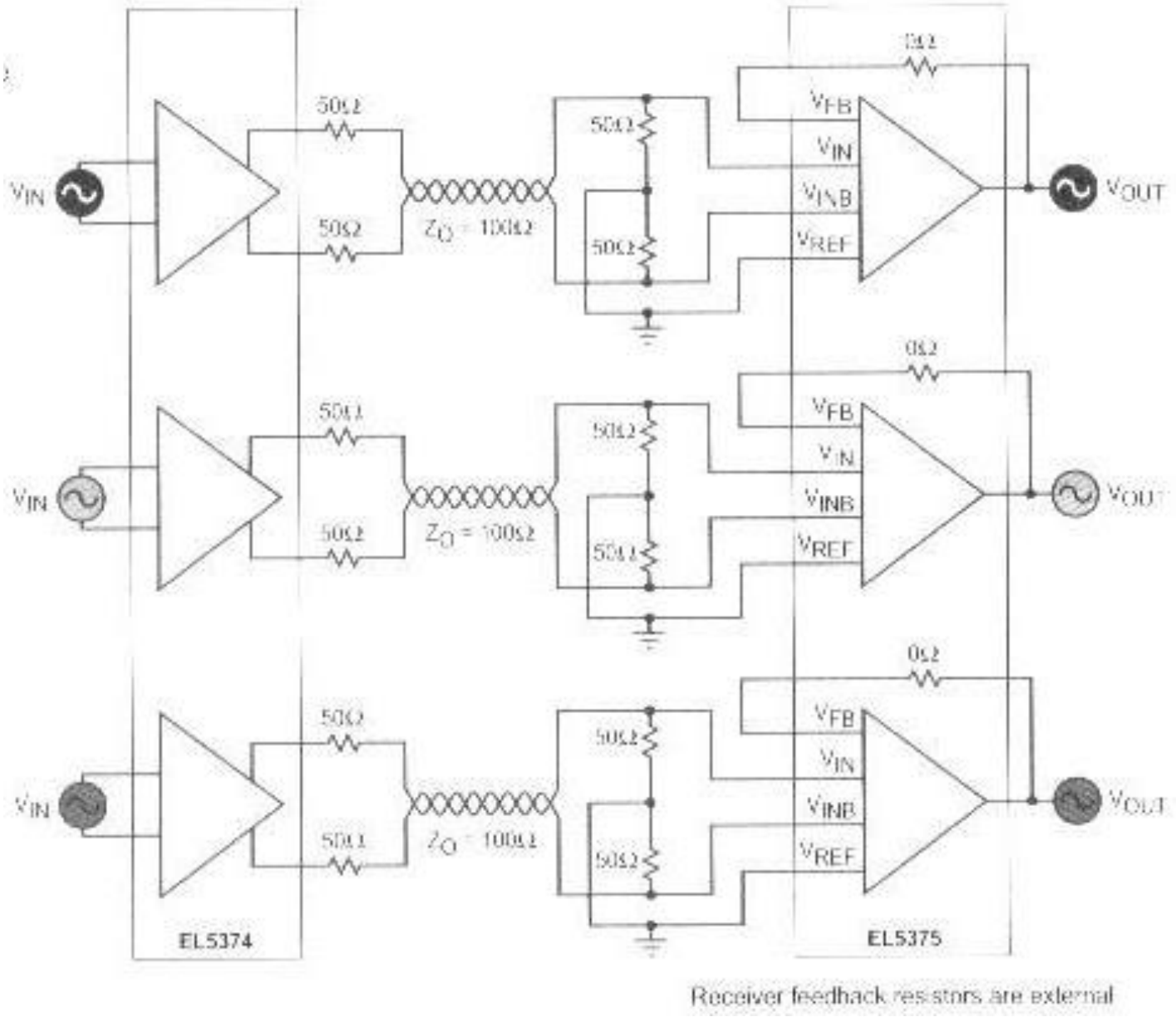
Differential lines: examples

[mipi]

Intersil
EL5374, 5375

(these are not
LVDS signals:
e.g. V_{offset}=0



Receiver feedback resistors are external

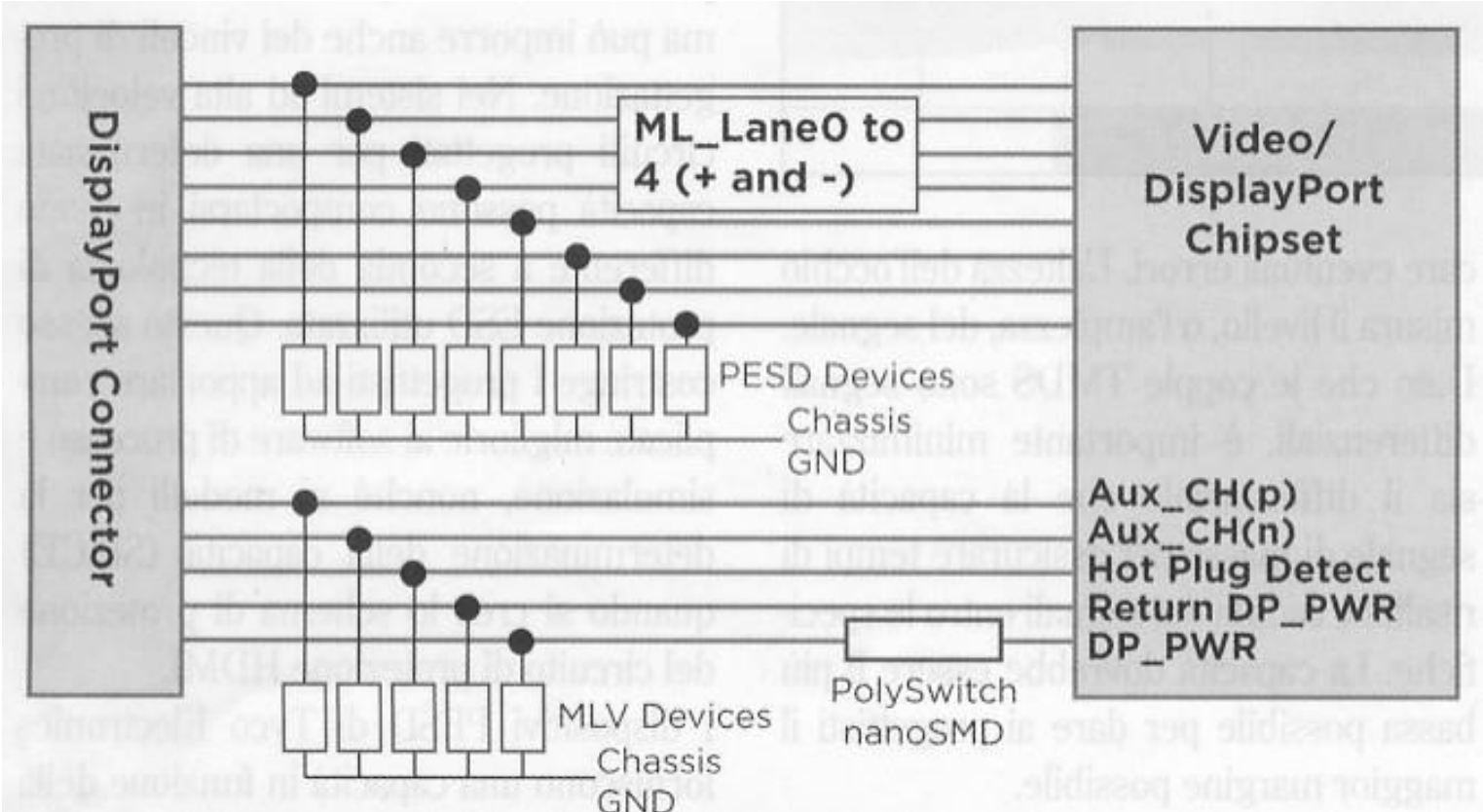
Some standards

Technology	Speed (Gbps)	Signal architecture	Signal speed (GHz)
HDMI 1.3 and 1.4 *	up to 10.2	4 diff. pairs (1 for the clock)	up to 3.4
Display port	up to 10.8	up to 4 diff. pairs	up to 2.7
E-SATA **	up to 3	2 diff. pairs	up to 1.5
USB 2.0	up to 0.48	1 diff. pair	up to 0.48
USB 3.0	up to 5	2 diff. pairs 1 Tx and 1 Rx	up to 5

* the physical layer is CML (similar to LVDS)
** normally used for external HDs for PCs

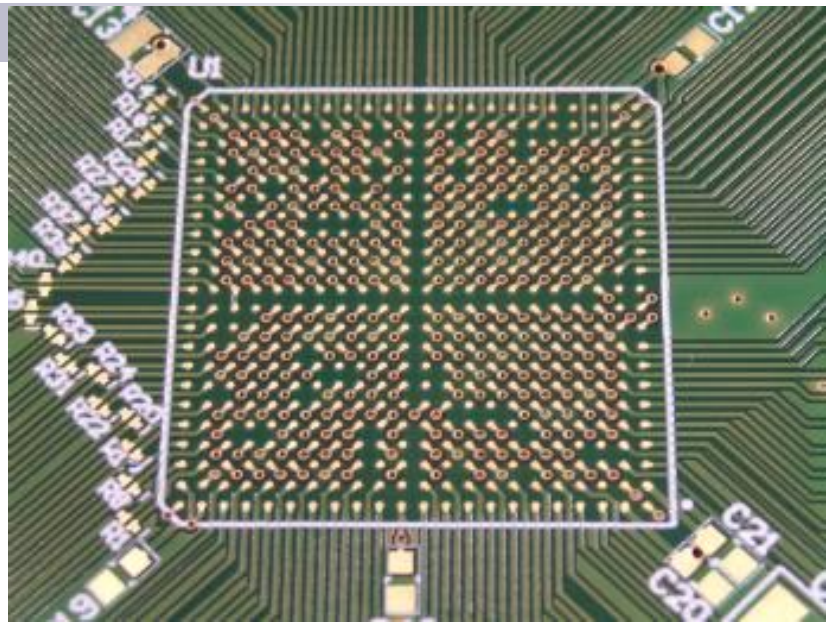
ESD and overcurrent protection

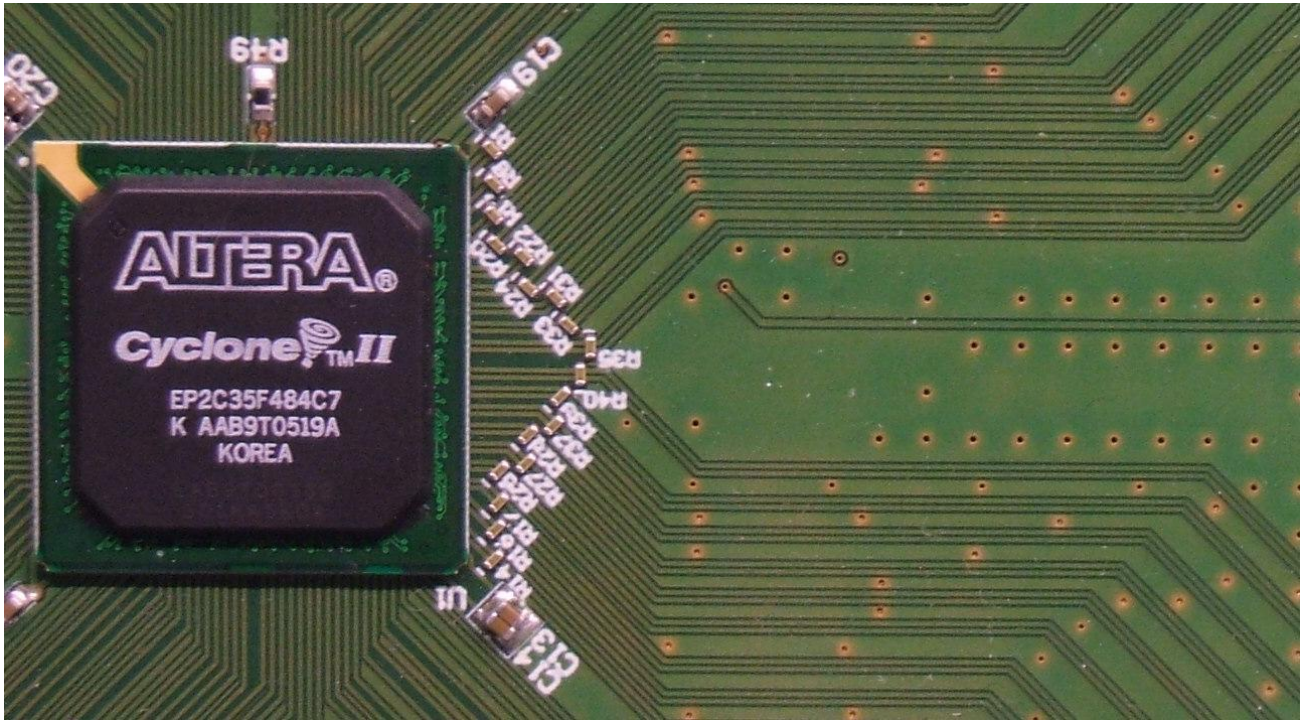
- Circuits have to be protected against ESD, and must often have overcurrent limiters
- In high speed applications, ESD protection devices must have very low parasitic capacitances
- An example for the DisplayPort standard:



Example with an Altera FPGA

with
- CMOS lines
- LVDS lines (terminated)





MIPI D-PHY

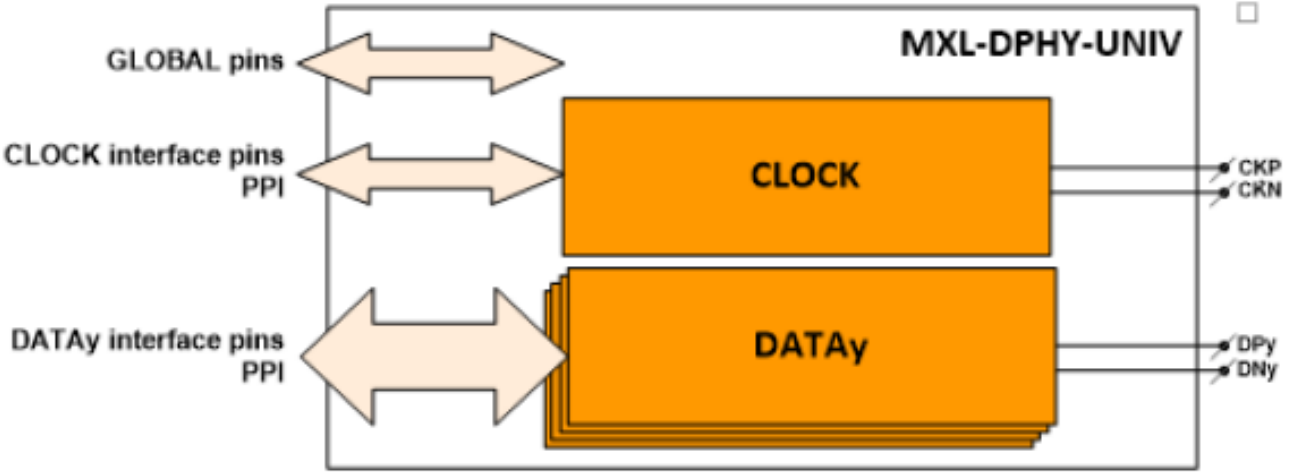


Figure 1: Four data lane D-PHY block diagram

Simple synchronous physical layer with one clock lane and several (e.g. 4) data lanes

Max. 1.5 or 2.5 Gbps per lane

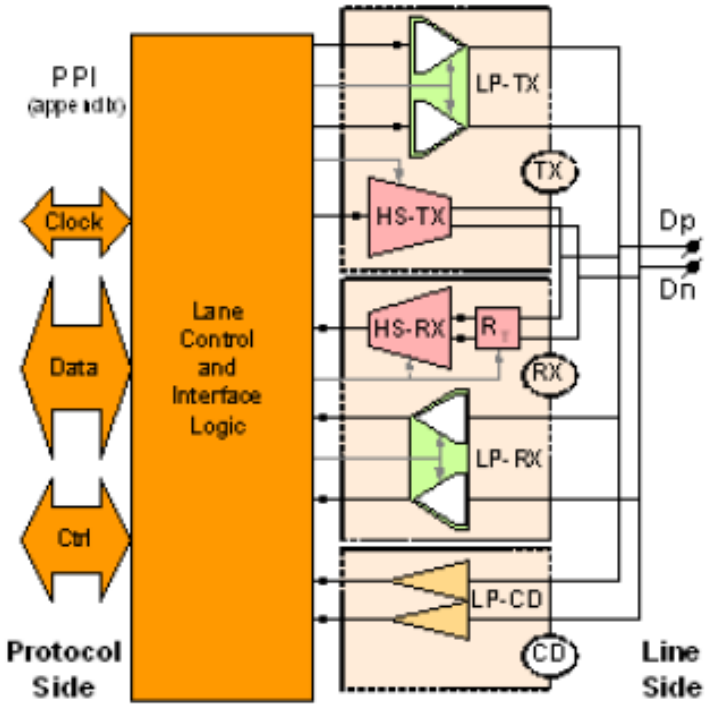
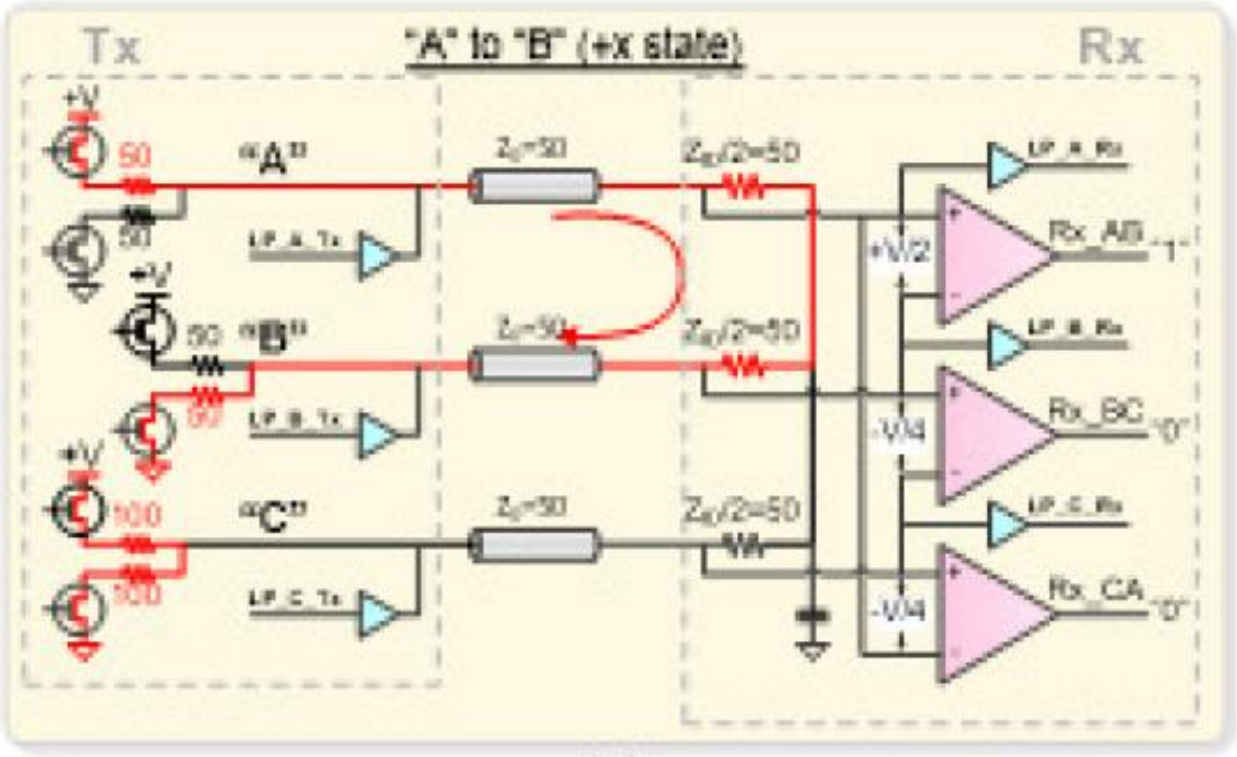


Figure 2: Block Diagram of a D-PHY data lane

MIPI C-PHY

It operates on 3 signals, a trio, and clock is embedded into the data

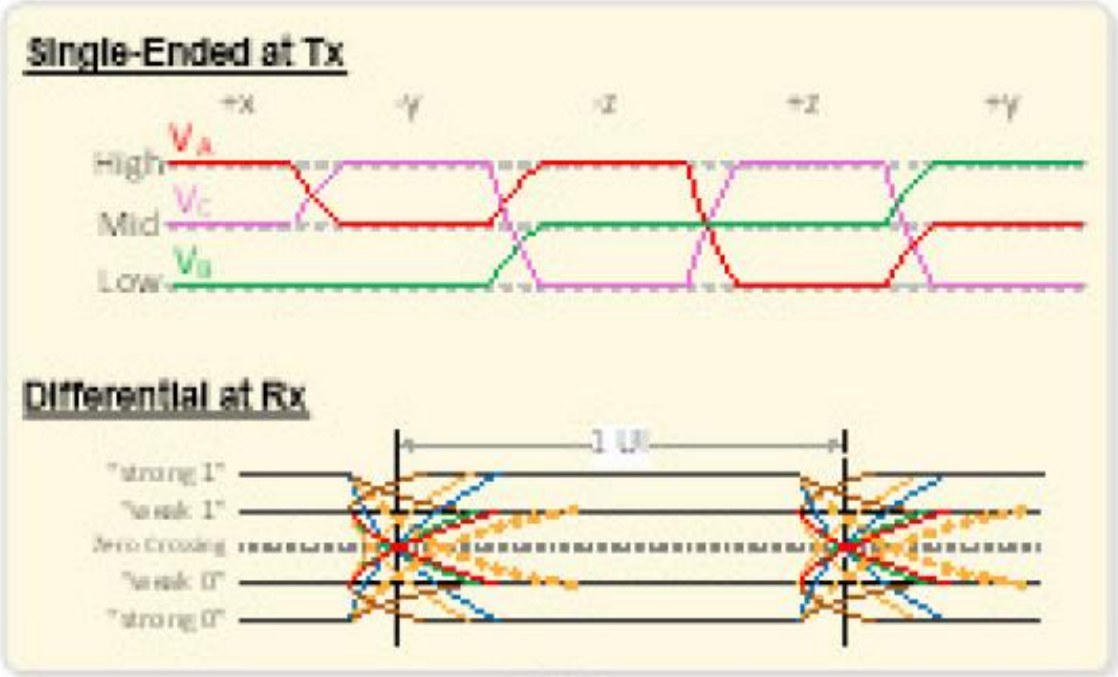


C-PHY

Each line is driven high, mid, or low, with some rules
- one transition per symbol
- all 3 differential RX inputs non-zero
- constant common mode

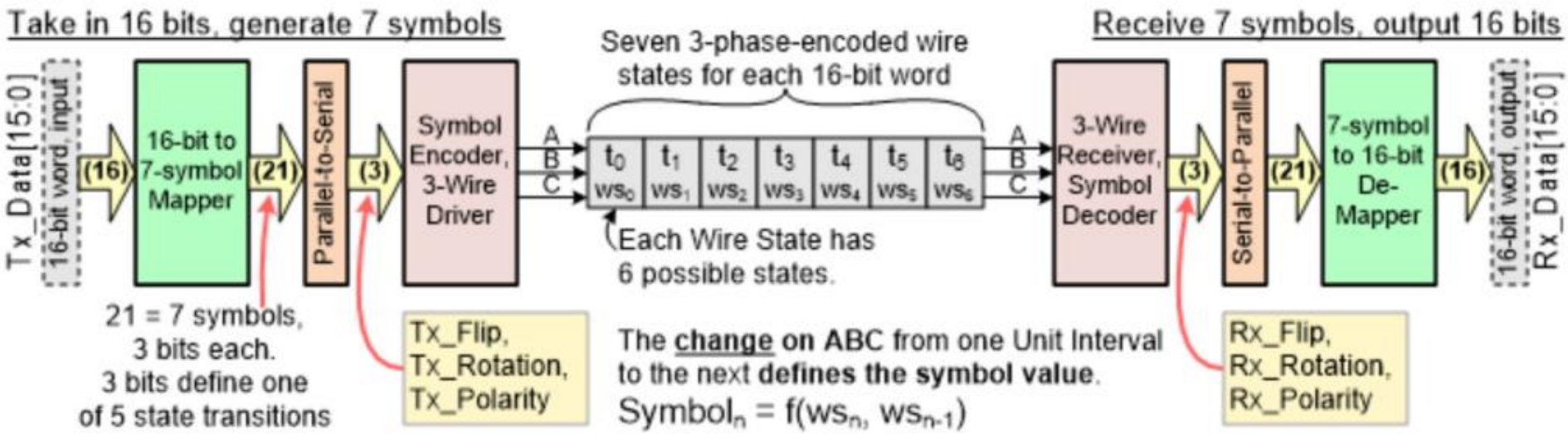
=> 5 possible states => it is a quinary system

Theoretical max. number of bits/symbol: $\log_2(5)=2.3219$



C-PHY

A mapper maps 16 bits into 7 symbols: 16/7≈2.28



C-PHY vs D_PHY (an example)