National Semiconductor

Application Note AN

Current Feedback Amplifiers

November 1992

The use of clever circuit architectures and the development of high-speed complementary BJT processes make it possible to achieve monolithic speeds and bandwidths hitherto available only in hybrid form.

—Sergio Franco, San Francisco State University
1600 Holloway Avenue, San Francisco, CA 94132

In their effort to approximate the ideal op amp, manufacturers must not only maximize the open-loop gain and minimize input-referred errors such as offset voltage, bias current, and noise, but must also ensure adequate bandwidth and settling-time characteristics. Amplifier dynamics are particuularly important in applications like high-speed DAC buffers, subranging ADCs, S/H circuits, ATE pin drivers, and video and IF drivers.[1]

Being basically voltage-processing devices, op amps are subject to the speed limitations inherent to voltage-mode operation, stemming primarily from the stray capacitances of nodes and the cutoff frequencies of transistors. Particularly severe is the effect of the stray capacitances between the input and output nodes of high-gain inverting stages because of the Miller effect which multiplies the stray capacitance by the voltage gain of the stage.

On the other hand, it has long been recognized that current manipulation is inherently faster than voltage manipulation. The effect of stray inductances in a circuit is usually less severe than that of its stray capacitances, and BJTs can switch currents much more rapidly than voltages. These technological reasons form the basis of emitter-coupled logic, bipolar DACs, current conveyors, and the high-speed amplifier topology known as *current-feedback*.[2]

For true current-mode operation, all nodes in the circuit should ideally be kept at fixed voltages to avoid the slow-down effect by their stray capacitances. However, since the output of the amplifier must be a voltage, some form of high-speed voltage-mode operation must also be provided at some point. This is achieved by employing gain configurations that are inherently immune from the Miller effect, such as the common-collector and the cascode configurations, and by driving the nodes with push-pull stages to rapidly charge/discharge their stray capacitances.

To ensure symmetric rise and fall times, the npn and pnp transistors must have comparable characteristics in terms of cutoff frequency f_t. Traditionally, monolithic pnp's have been plagued by much poorer performance characteristics than their npn counterparts. However, the recent development of truly complementary high-speed processes makes it possible to achieve monolithic speeds that were hitherto available only in hybrid form.

The advantages of the current-feedback topology are best appreciated by comparing it against that of the conventional op amp.[3,4]

The Conventional Op Amp

The conventional op amp consists of a high input-impedance differential stage followed by additional gain stages, the last of which is a low output-impedance stage. As shown in the circuit model of Fig. 1a, the op amp transfer characteristic is

$$V_o = a(jf)V_d \qquad (1)$$

where V_o is the output voltage; $V_d = V_p - V_n$ is the differential input voltage; and $a(jf)$, a complex function of frequency f, is the open-loop gain.

Connecting an external network as in Fig. 1b creates a feedback path along which a signal in the form of a *voltage* is derived from the output and applied to the noninverting input. By inspection.

$$V_d = V_i - \frac{R_1}{R_1 + R_2} V_o \qquad (2)$$

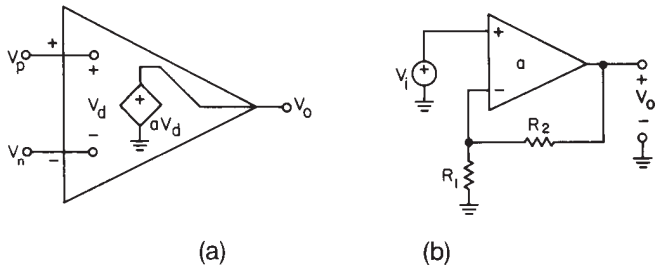

Fig. 1: Circuit model of the conventional op amp, and connection as a noninverting amplifier.

Substituting into Eq. (1), collecting, and solving for the ratio V_o/V_i yields the familiar noninverting amplifier transfer characteristic

$$A(jf) \triangleq \frac{V_o}{V_i} = \left(1 + \frac{R_2}{R_1}\right) \frac{1}{1 + 1/T(jf)} \qquad (3)$$

where $A(jf)$ represents the closed-loop gain, and

$$T(jf) = \frac{a(jf)}{1 + R_2/R_1} \qquad (4)$$

represents the loop gain.

The designation *loop gain* stems from the fact that if we break the loop as in Fig. 2a and inject a test signal V_x with V_i suppressed, the circuit will first attenuate V_x to produce $V_n = V_x/(1 + R_2/R_1)$, and then amplify V_n to produce $V_o = -aV_n$. Hence, the gain experienced by a signal in going around the loop is $V_o/V_x = -a/(1 + R_2/R_1)$. The *negative* of this ratio represents the loop gain, $T \triangleq -(V_o/V_x)$. Hence, Eq. (4).

The loop gain gives a measure of how close A is to the ideal value $1 + R_2/R_1$, also called the *noise gain* of the circuit. By Eq. (3), the larger *T*, the better. To ensure substantial loop gain over a wide range of closed-loop gains, op amp manufacturers strive to make *a* as large as possible. Consequently, V_d will assume extremely small values since $V_d = V_o/a$. In the limit $a \to \infty$ we obtain $V_d \to 0$, that is, $V_n \to V_p$. This forms the basis of the familiar op amp rule: when operated with negative feedback, an op amp will provide whatever output voltage and current are needed to ideally force V_n to follow V_p.

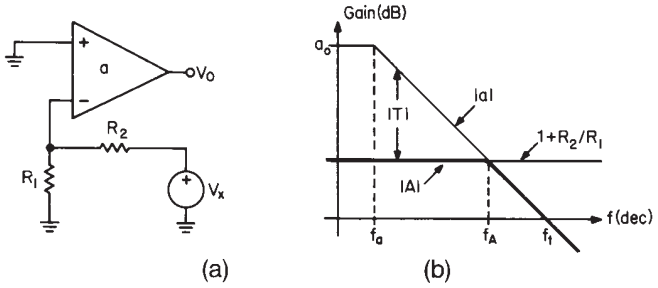

Fig. 2: Test circuit to find the loop gain, and graphical method to determine the closed-loop bandwidth f_A.

Gain-Bandwidth Tradeoff

Large open-loop gains can physically be realized only over a limited frequency range. Past this range, gain rolls off with frequency. Most op amps are designed for a constant rolloff of −20dB/dec, so that the open-loop response can be expressed as

$$a(jf) = \frac{a_o}{1 + j(f/f_a)} \qquad (5)$$

where a_o represents the *dc gain,* and f_a is the −3dB *frequency* of the open-loop response. Both parameters can be found from the data sheets. For example, the 741 op amp has $a_o \simeq 2 \times 10^5$ and $f_a \simeq 5$Hz.

Substituting Eq. (5) into Eq. (4) and then into Eq. (3), and exploiting the fact that $(1 + R_2/R_1)\, a_o \ll 1$, we obtain

$$A(jf) = \frac{1 + R_2/R_1}{1 + j(f/f_A)} \qquad (6)$$

where

$$f_A = \frac{f_t}{1 + R_2/R_1} \qquad (7)$$

represents the *closed-loop bandwidth,* and $f_t = a_o f_a$ represents the open-loop unity-gain frequency, that is the frequency at which $|a| = 1$. For instance, the 741 op amp has $f_t = 2 \times 10^5 \times 5 = 1$ MHz.

Equation (7) reveals a gain-bandwidth tradeoff. As we raise the R_2/R_1 ratio to increase the closed-loop gain, we also decrease its bandwidth in the process. Moreover, by Eq. (4), the loop-gain is also decreased, thus leading to a greater closed-loop gain error.

The above concepts can also be visualized graphically. Since Eq. (4) implies $|T|_{dB} \triangleq 20 \log |T| = 20 \log |a| - 20 \log (1 + R_2/R_1) \triangleq |a|_{dB} - (1 + R_2/R_1)_{dB}$, it follows that the loop gain can be found graphically as the *difference* between the open-loop gain and the noise gain. This is shown in Fig. 2b. The frequency at which the two curves meet is called the *crossover frequency.* At this frequency we have $T = 1\angle -90° = -j$, that is, $|A| = (1 + R_2/R_1)/\sqrt{2}$. Thus, the crossover frequency represents the −3dB frequency of the closed-loop response, that is, the closed-loop bandwidth f_A.

We now see that increasing the closed-loop gain shifts the noise-gain curve upward, thus reducing the loop gain, and causes the crosspoint to move up the $|a|$ curve, thus decreasing the closed-loop bandwidth. Clearly, the circuit with the widest bandwidth and the highest loop gain is also the one with the lowest closed-loop gain. This is the voltage follower, for which $R_2/R_1 = 0$, so that $A = 1$ and $f_A = f_t$.

Slew-Rate Limiting

To fully characterize the dynamic behavior of an op amp, we also need to know its *transient response.* If an op amp with the response of Eq. (5) is operated as a unity-gain voltage follower and is subjected to a suitably small voltage step, its dynamic behavior will be similar to that of an *RC* network. Applying an input step ΔV_i will cause the output to undergo an exponential transition with magnitude $\Delta V_o = \Delta V_i$, and with a time-constant $\tau = 1/(2\pi f_t)$. For the 741 op amp we have $\tau = 1/(2\pi \times 10^6) \simeq 170$ ns.

The rate at which the output changes with time is highest at the beginning of the exponential transition, when its value is $\Delta V_o/\tau$. Increasing the step magnitude increases this initial rate of change, until the latter will saturate at a value called the slew-rate (SR). This effect stems from the limited ability of the internal circuitry to charge/discharge capacitive loads, especially the compensation capacitor responsible for open-loop bandwidth f_a.

To illustrate, refer to the circuit model of Fig. 3, which is typical of many op amps.[4] The input stage is a transconductance block consisting of differential pair Q_1–Q_2 and current mirror Q_3–Q_4. The remaining stages are lumped together as an integrator block consisting of an inverting amplifier and the compensation capacitor *C*. Slew-rate limiting occurs when the transconductance stage is driven into saturation, so that all the current available to charge/discharge *C* is the bias current *I* of this stage. For example, the 741 op amp has $I = 20\ \mu$A and $C = 30$ pF, so that $SR = I/C = 0.67\ V/\mu s$. The step magnitude corresponding to the onset of slew-rate limiting is such that $\Delta V_i/\tau = SR$, that is, $\Delta V_i = SR \times \tau = (0.67\ V/\mu s) \times (170\ ns) = 116$ mV. As long as the step is less than 116 mV, a 741 voltage follower will respond with an exponential transition governed by $\tau \simeq 170$ ns, whereas for a greater input step the output will slew at a constant rate of $0.67\ V/\mu s$.

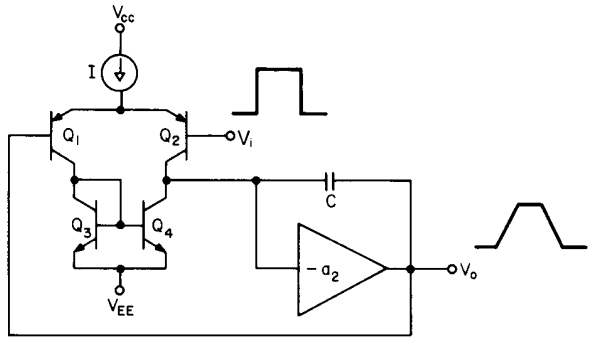

Fig. 3: Simplified slew-rate model of a conventional op amp.

In many applications the dynamic parameter of greatest concern is the *settling time*, that is, the time it takes for the output to settle and remain within a specified band around its final value, usually for a full-scale output transition. Clearly, slew-rate limiting plays an important role in the settling-time characteristic of the device.

The Current-Feedback Amplifier

As shown in the circuit model of Fig. 4, the architecture of the current-feedback amplifier (CF amp) differs from the conventional op amp in two respects:[2]

1. The input stage is a *unity-gain voltage buffer* connected across the inputs of the op amp. Its function is to force V_n to follow V_p, very much like a conventional op amp does via negative feedback. However, because of the low output impedance of this buffer, current can easily flow in or out of the inverting input, though we shall see that in normal operation this current is extremely small.

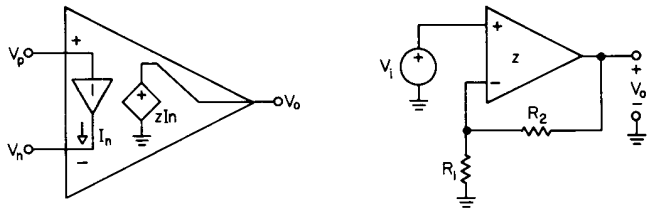

Fig. 4: Circuit model of the current-feedback amplifier, and connection as a noninverting amplifier.

2. Amplification is provided by a *transimpedance amplifier* which senses the current delivered by the buffer to the external feedback network, and produces an output voltage V_o such that

$$V_o = z(jf)\,I_n \qquad (8)$$

where $z(jf)$ represents the *transimpedance gain* of the amplifier, in V/A or Ω, and I_n is the current out of the inverting input.

To fully appreciate the inner workings of the CF amp, it is instructive to examine the simplified circuit diagram of Fig. 5a. The input buffer consists of transistors Q_1 through Q_4. While Q_1 and Q_2 form a low output-impedance push-pull stage, Q_3 and Q_4 provide V_{BE} compensation for the push-pull pair, as well as a Darlington function to raise the input impedance.

Summing currents at the inverting node yields $I_1 - I_2 = I_n$, where I_1 and I_2 are the push-pull transistor currents. Two Wilson current mirrors, consisting of transistors Q_9–Q_{10}–Q_{11} and Q_{13}–Q_{14}–Q_{15}, reflect these currents and recombine them at a common node, whose equivalent capacitance to ground has been designated as *C*. By mirror action, the current through this capacitance is $I_C = I_1 - I_2$, that is

$$I_C = I_n \qquad (9)$$

The voltage developed by *C* in response to this current is then conveyed to the output via a second buffer, consisting of Q_5 through Q_8. The salient features of the CF amp are summarized in block diagram form in Fig. 5b.

When the amplifier loop is closed as in Fig. 4b, and whenever an external signal tries to imbalance the two inputs, the input buffer will begin sourcing (or sinking) an imbalance current I_n to the external resistances. This imbalance is then conveyed by the Wilson mirrors to capacitor *C*, causing V_o to swing in the positive (or negative) direction until the original imbalance I_n is neutralized via the negative feedback loop. Thus, I_n plays the role of error signal in the system.

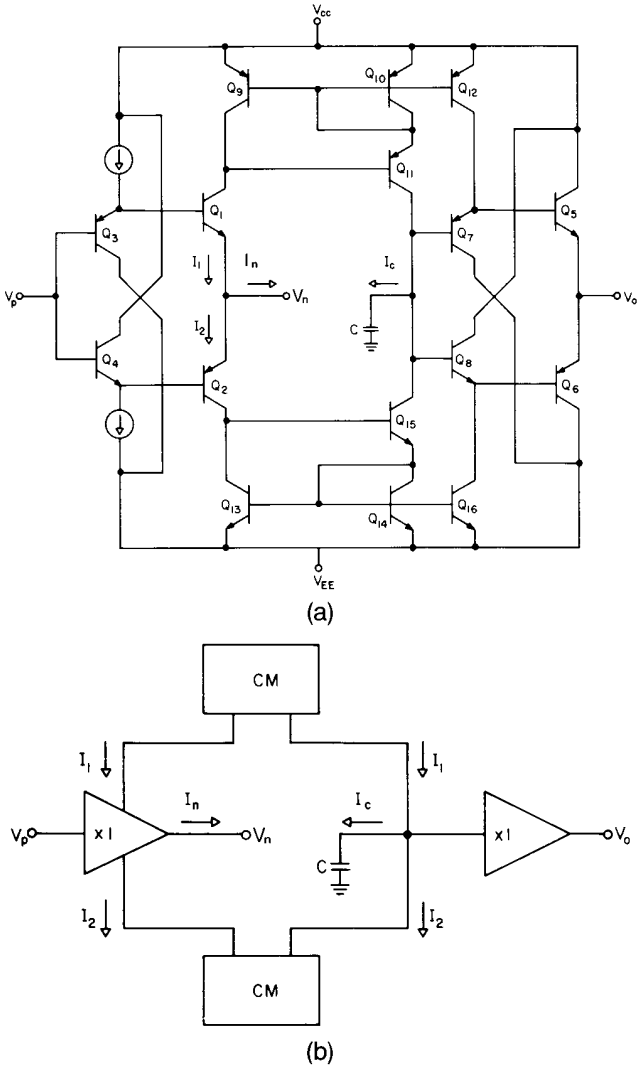

Fig. 5: Simplified circuit diagram and block diagram of a current-feedback amplifier.

To obtain the closed-loop transfer characteristic, refer again to Fig. 4b. Summing currents at the inverting node yields

$$I_n = \frac{V_n}{R_1} - \frac{V_o - V_n}{R_2} \qquad (10)$$

since the buffer ensures $V_n = V_p = V_i$ we can rewrite as

$$I_n = \frac{V_i}{R_1 \,||\, R_2} - \frac{V_o}{R_2} \qquad (11)$$

confirming that the feedback signal V_o/R_2 is now in the form of a *current*. Substituting into Eq. (8), collecting, and solving for the ratio V_o/V_i yields

$$A(jf) \triangleq \frac{V_o}{V_i} = \left(1 + \frac{R_2}{R_1}\right) \frac{1}{1 + 1/T(jf)} \qquad (12)$$

where $A(jf)$ represents the *closed-loop gain* of the circuit, and

$$T(jf) = \frac{z(jf)}{R_2} \qquad (13)$$

represents the *loop gain*. This designation stems again from the fact that if we break the loop as in Fig. 6a, and inject a test voltage V_x with the input V_i suppressed, the circuit will first convert V_x to the current $I_n = -V_x/R_2$, and then convert I_n to the voltage $V_o = zI_n$, so that $T \triangleq -(V_o/V_x) = z/R_2$, as expected.

In an effort to ensure substantial loop gain to reduce the closed-loop gain error, manufacturers strive to make z as large as possible relative to the expected values of R_2. Consequently, since $I_n = V_o/z$, the inverting-input current will be very small, though this input is a low-impedance node because of the buffer. In the limit $z \to \infty$ we obtain $I_n \to 0$, indicating that a CF amp will provide whatever output voltage and current are needed to ideally drive I_n to zero. Thus, the conventional op amp conditions $V_n = V_p$ and $I_n = I_p = 0$ hold for CF amps as well.

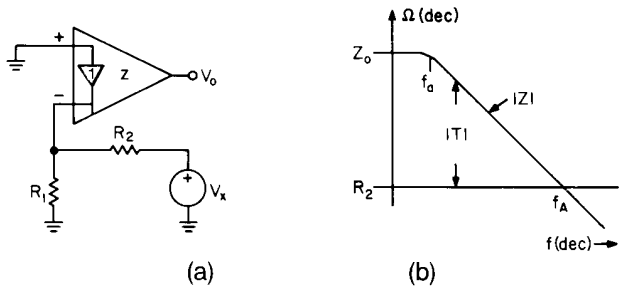

Fig. 6: Test circuit to find the loop gain, and graphical method to determine the closed-loop bandwidth f_A.

No Gain-Bandwidth Tradeoff

The transimpedance gain of a practical CF amp rolls off with frequency according to

$$z(jf) = \frac{z_o}{1 + j(f/f_a)} \qquad (14)$$

where z_o is the *dc value* of the transimpedance gain, and f_a is the frequency at which rolloff begins. For instance, from the data sheets of the CLC401 CF amp (Comlinear Co.) we find $z_o = 710\ k\Omega$, and $f_a = 350\ kHz$.

Substituting Eq. (14) into Eq. (13) and then into Eq. (12), and exploiting the fact that $R_2/z_o \ll 1$, we obtain

$$A(jf) = \frac{1 + R_2/R_1}{1 + j(f/f_A)} \qquad (15)$$

where

$$f_A = \frac{z_o f_a}{R_2} \qquad (16)$$

represents the *closed-loop bandwidth*. for R_2 in the kΩ range, f_A is typically in the 100 MHz. Retracing previous reasoning, we see that the noise-gain curve is now R_2, and that f_A can be found graphically as the frequency at which this curve meets the $|z|$ curve, see Fig. 6b.

Comparing with Eqs. (6) and (7), we note that the closed-loop gain expressions are formally identical. However, the bandwidth now depends only on R_2 rather than on the closed-loop gain $1 + R_2/R_1$. Consequently, we can use R_2 to select the bandwidth, and R_1 to select the gain. The ability to control gain independently of bandwidth constitutes a major advantage of CF amps over conventional op amps, especially in automatic gain control applications. This important difference is highlighted in Fig. 7.

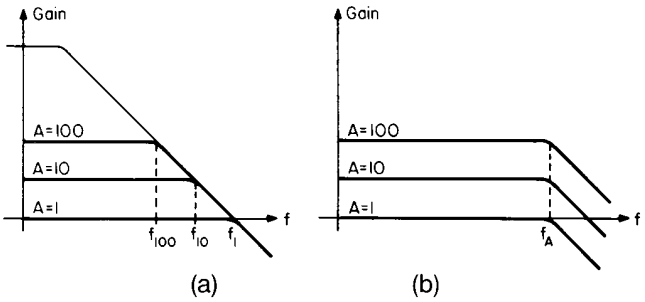

Fig. 7: Comparing the gain-bandwidth relationship of conventional op amps and current-feedback amplifiers.

Absence of Slew-Rate Limiting

The other major advantage of CF amps is the inherent absence of slew-rate limiting. This stems from the fact that the current available to charge the internal capacitance at the onset of a step is proportional to the step regardless of its size. Indeed, applying a step ΔV_i induces, by Eq. (11), an initial current imbalance $I_n = \Delta V_i/(R_1 \,||\, R_2)$, which the Wilson mirrors then convey to the capacitor. The initial rate of charge is, therefore, $I_c/C = I_n/C = \Delta V_i/[(R_1 \,||\, R_2)C] = [\Delta V_i(1 + R_2/R_1)]/(R_2C) = \Delta V_o/(R_2C)$, indicating an exponential output transition with time-constant $\tau = R_2C$. Like the frequency response, the transient response is governed by R_2 alone, regardless of the closed-loop gain. With R_2 in the kΩ range and C in the pF range, τ comes out in the ns range.

The *rise time* is defined as the amount of time t_r it takes for the output to swing from 10% to 90% of the step size. For an exponential transition, $t_r = \tau \times \ln(0.9/0.1) = 2.2\tau$.

For example, the CLC401 has $t_r = 2.5$ ns for a 2V output step, indicating an effective τ of 1.14 ns. The time it takes for the output to settle within 0.1% of the final value is $t_s = \tau \ln 1000 \simeq 7\tau$. For the CLC401, this yields $t_s \simeq 8$ ns, in reasonable agreement with the data sheet value of 10 ns.

The absence of slew-rate limiting not only allows for faster settling times, but also eliminates slew-rate related nonlinearities such as intermodulation distortion. This makes CF amps attractive in high-quality audio amplifier applications.

Second-Order Effects

The above analysis indicates that once R_2 has been set, the dynamics of the amplifier are unaffected by the closed-loop gain setting. In practice it is found that bandwidth and rise time do vary with gain somewhat, though not as drastically as with conventional op amps. The main cause is the non-zero output impedance of the input buffer, whose effect is to alter the loop gain and, hence, the closed-loop dynamics.

Referring to Fig. 8a and denoting this impedance as R_o, we note that the circuit first converts V_x to a current $I_{R2} = V_x/(R_2 + R_1 \| R_0)$, then it divides I_{R2} to produce $I_n = I_{R2}R_1/(R_1 + R_0)$, and finally it converts I_n to the voltage $V_o = zI_n$. Eliminating I_{R2} and I_n and letting $T = -V_o/V_x$ yields $T = z/Z_2$, where

$$Z_2 = R_2\left(1 + \frac{R_0}{R_1 \| R_2}\right) \qquad (17)$$

Thus, the effect of R_0 is to increase the noise gain from R_2 to $R_2[1 + R_0/(R_1 \| R_2)]$, see Fig. 8b, curve 1. Consequently, both bandwidth and rise time will be reduced by a proportional amount.

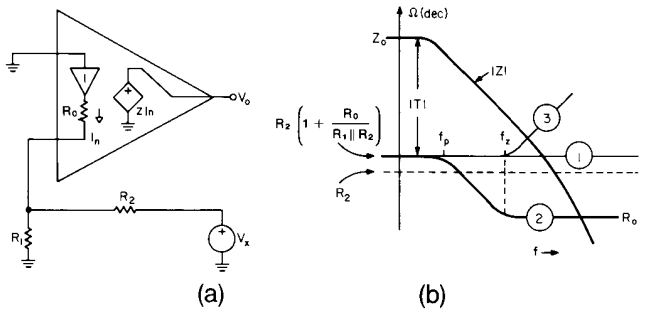

Fig. 8: Test circuit to investigate the effect of R_0, and noise-gain curves for the case of: (1) purely resistive feedback, (2) a capacitance in parallel with R_2, and (3) the same capacitance in parallel with R_1.

Replacing R_2 with Z_2 in Eq. (16) yields, after simple manipulation,

$$f_A = \frac{f_t}{1 + \frac{R_0}{R_2}\left(1 + \frac{R_2}{R_1}\right)} \qquad (18)$$

where $f_t = z_0 f_a/R_2$ represents the extrapolated value of f_A in the limit $R_0 \to 0$. This equation indicates that bandwidth reduction due to R_0 will be more pronounced at high closed-loop gains. As an example, suppose a CF amp has $R_0 = 50\Omega$, $R_2 = 1.5$ kΩ, and $f_t = 100$ MHz, so that $f_A = 10^8/[1 + (50/1500)A_0] = 10^8/(1 + A_0/30)$, where $A_0 = 1 + R_2/R_1$. Then, the bandwidths corresponding to $A_0 = 1$, 10, and 100 are, respectively, $f_1 = 96.8$ MHz, $f_{10} = 75.0$ MHz, and $f_{100} = 23.1$ MHz. Note that these values still compare favorably with a conventional op amp, whose bandwidth would be reduced, respectively, by 1, 10, and 100.

If so desired, the external resistance values can be predistorted to compensate for the bandwidth reduction at high gains. Turning Eq. (18) around yields the required value of R_2 for a given bandwidth f_A and gain A_0.

$$R_2 = \frac{z_0 f_a}{f_A} - R_0 A_0 \qquad (19)$$

while the required value of R_1 for the given gain A_0 is

$$R_1 = \frac{R_2}{A_0 - 1} \qquad (20)$$

As an example, suppose we want the above amplifier to retain its 100 MHz bandwidth at a closed-loop gain of 10. Since with $R_2 = 1.5$ kΩ this device has $z_0 f_a/R_2 = 100$ MHz, it follows that $z_0 f_a = 10^8 \times 1500 = 1.5 \times 10^{11}\ \Omega \times$ Hz. Then, the above equations yield $R_2 = 1.5 \times 10^{11}/10^8 - 50 \times 10 = 1$ kΩ, and $R_1 = 1000/(10 - 1) = 111\ \Omega$.

Besides the dominant pole at f_a, the open-loop response of a practical amplifier presents additional poles above the crossover frequency. As shown in Fig. 8b, the effect of these poles is to cause a steeper gain rolloff at this frequency, further reducing the closed-loop bandwidth. Moreover, the additional phase-shift due to these poles decreases the phase margin somewhat, thus causing a small amount of peaking in the frequency response, and ringing in the transient response.

Finally, it must be said that the rise time of a practical CF amp does increase with the step size somewhat, due primarily to transistor current gain degradation at high current levels. For instance, the rise time of the CLC401 changes from 2.5 ns to 5 ns as the step size is changed from 2V to 5V. In spite of second-order limitations, CF amps still provide superior dynamics.

CF Applications Considerations

Although the above treatment has focused on the non-inverting configuration, the CF amp will work as well in most other resistive feedback configurations, such as the inverting amplifier, the summing and differencing amplifier, I–V and V–I converters, and KRC active filters.[4] In fact, the derivation of the transfer characteristic of any of these circuits proceeds along the same lines as conventional op amps. Special consideration, however, require the cases in which the feedback network includes reactive elements, either intentional or parasitic.

Consider first the effect of a *feedback capacitance* C_2 in parallel with R_2 in the basic circuit of Fig. 8a. Letting $Z = R_2 \| (1/sC_2)$, the noise gain becomes $Z_2 = Z[1 + R_0/(R_1 \| Z)]$. After expanding, it is readily seen that the noise-gain curve has a pole at $f_p = 1/(2\pi R_2 C_2)$ and a zero at $f_z = 1/[2\pi(R_0 \| R_1 \| R_2)C_2]$, as shown in Fig. 8b, curve 2. Consequently, the crossover frequency will be pushed into the region of substantial

phase shift due to the higher-order poles of z. If the overall shift reaches −180° at this frequency, then $T = 1\angle -180° = -1$ there, indicating that *A* will become infinite by Eq. (12), and the circuit will oscillate. Even if the phase shift fails to reach −180°, the closed-loop response may still exhibit intolerable peaking and ringing. Hence, capacitive feedback must be avoided with CF amps. To minimize the effect of stray feedback capacitances, manufacturers often provide R_2 internally.

CF Integrators

To synthesize the integrator function in CF form, which provides the basis for dual-integrator-loop filters and oscillators as well as other popular circuits, we must use configurations that avoid a direct capacitance between the output and the inverting input. One possibility is offered by the Deboo integrator,[4] which belongs to the class of KRC filters and is therefore amenable to CF realization. Its drawback is the need for tightly matched resistances, if lossless integration is desired. The alternative of Fig. 9 not only meets the given constraint, but also provides *active compensation*, a highly desirable feature to cope with Q-enhancement problems in dual-integrator-loop filters.[4] Using standard op amp analysis techniques, it is readily seen that the unity-gain frequency of this integrator is $f_0 = (R_2/R_1)/(2\pi RC)$.

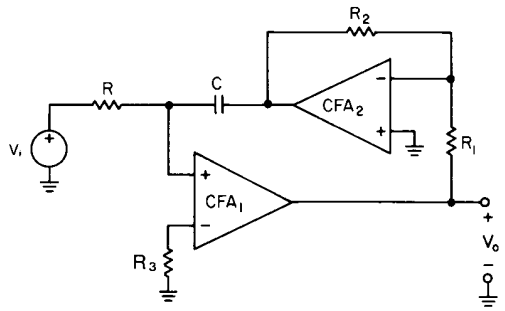

Fig. 9: Actively-compensated CF integrator.

Stray Input-Capacitance Compensation

Next, consider the effect of an *input capacitance* C_1 in parallel with R_1 in the basic circuit of Fig. 8a. Letting $Z = R_1 \| (1/sC_1)$, the noise gain is now $Z_2 = R_2[1 + R_0/(Z \| R_2)]$. After expanding, it is readily seen that the noise-gain curve has a zero at $f_z = 1/[2\pi(R_0 \| R_1 \| R_2)C_1]$, as shown in Fig. 8b, curve 3. If C_1 is sufficiently large, the phase of *T* at the crossover frequency will again approach −180°, bringing the circuit on the verge of instability. This is of particular concern in current-mode DAC output buffering, where C_1 is the output capacitance of the DAC, typically in the range of a few tens to a few hundreds of picofarads, depending on the DAC type.

Like a conventional op amp, the CF amp can be stabilized by using a feedback capacitance C_2 to introduce sufficient phase-lead to compensate for the phase-lag due to the input capacitance C_1. For a phase margin of 45°, choose the value of C_2 so that the noise-gain pole $f_p = 1/(2\pi R_2 C_2)$ coincides with the crossover frequency f_A, as shown in Fig. 10a. Using asymptotic Bode-plot reasoning,[4] it is easily seen that $f_A = [z_0 f_a f_z/(R_0 + R_2)]^{1/2}$, where $f_z = 1/[2\pi(R_0 \| R_2)C_1]$. Imposing $f_p = f_A$ yields

$$C_2 = \left(\frac{R_0}{2\pi R_2 z_0 f_a} C_1 \right)^{1/2} \qquad (21)$$

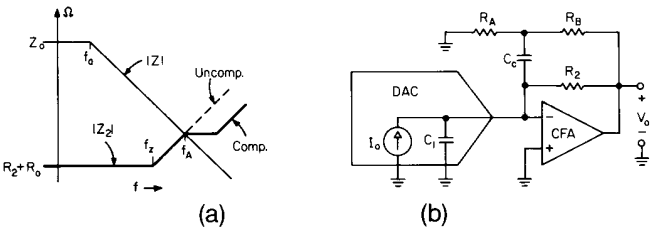

Fig. 10: DAC output capacitance compensation.

To cope with impractically low values of C_2, it is convenient to drive C_2 with a voltage divider as in Fig. 10b, since this will scale the value of C_2 to the more practical value

$$C_c = \left(1 + \frac{R_B}{R_A} \right) C_2 \qquad (22)$$

It can be shown that for this technique to be effective we must choose $R_B \ll R_2$. As an example, suppose a DAC having $C_1 = 100$ pF feeds the CF amp considered earlier. Then, Eq. (21) yields $C_2 = [50 \times 100 \times 10^{-12}/(2\pi \times 1.5 \times 10^3 \times 1.5 \times 10^{11})]^{1/2} = 1.88$ pF. To scale it to a more practical value, use [5] $R_A = 50\Omega$ and $R_B = 500\Omega$. Then, $C_c = (1 + 500/50)\,1.88 \simeq 21$ pF. This estimate may require some fine tuning to optimize the transient response.

Additional useful application hints can be found in Ref. [5].

References

1. P. Harold, *Current-Feedback Op Amps Ease High-Speed Circuit Design*, to be published in *EDN*, 1988.
2. *A New Approach to Op Amp Design*, Comlinear Corporation Application Note 300-1, March 1985.
3. *1988 Current-Feedback Seminar*, Comlinear Corp.
4. Sergio Franco, *Design with Operational Amplifiers and Analog ICs*, McGraw-Hill Book Company, 1988.
5. *Current-Feedback Op Amp Applications Circuit Guide*, Comlinear Corporation Application Note OA-07, 1988.

This page intentionally left blank.

Customer Design Applications Support

National Semiconductor is committed to design excellence. For sales, literature and technical support, call the National Semiconductor Customer Response Group at **1-800-272-9959** or fax **1-800-737-7018**.

Life Support Policy

National's products are not authorized for use as critical components in life support devices or systems without the express written approval of the president of National Semiconductor Corporation. As used herein:

1. Life support devices or systems are devices or systems which, a) are intended for surgical implant into the body, or b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.

2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

National Semiconductor Europe
Fax: (+49) 0-180-530 85 86
E-mail: europe.support@nsc.com
Deutsch Tel: (+49) 0-180-530 85 85
English Tel: (+49) 0-180-532 78 32
Francais Tel: (+49) 0-180-532 93 58
Italiano Tel: (+49) 0-180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block
Ocean Centre, 5 Canton Road
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2309
Fax: 81-043-299-2408